

SN55ALS160, SN75ALS160 OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

SLLS018D – JUNE 1986 – REVISED MAY 1995

SUITABLE FOR IEEE STANDARD 488-1978 (GPIB)[†]

- 8-Channel Bidirectional Transceivers
- High-Speed Advanced Low-Power Schottky (ALS) Circuitry
- Low Power Dissipation:
 - SN55ALS160 . . . 56 mW Max Per Channel
 - SN75ALS160 . . . 46 mW Max Per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis:
 - SN55ALS160 . . . 550 mV Typ
 - SN75ALS160 . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down ($V_{CC} = 0$)
- Power-Up/Power-Down Protection (Glitch Free)

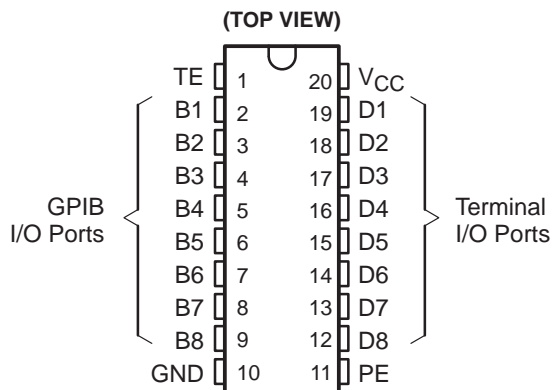
description

The SN55ALS160 and SN75ALS160 eight-channel general-purpose interface bus transceivers are monolithic, high-speed, advanced low-power Schottky (ALS) devices designed for two-way data communications over single-ended transmission lines. They are designed to meet the requirements of IEEE Standard 488-1978. The transceivers feature driver outputs that can be operated in either the passive-pullup or 3-state mode. If talk enable (TE) is high, these ports have the characteristics of passive-pullup outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

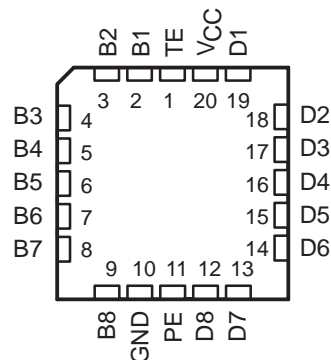
An active turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when $V_{CC} = 0$. When combined with the SN55ALS161, SN75ALS161, or SN75ALS162 bus management transceiver, the pair provides the complete 16-wire interface for the IEEE-488 bus.

The SN55ALS160 is characterized for operation from -55°C to 125°C . The SN75ALS160 is characterized for operation from 0°C to 70°C .

SN55ALS160 . . . J OR W PACKAGE
SN75ALS160 . . . DW OR N PACKAGE



SN55ALS160 . . . FK PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†] The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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Function Tables

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

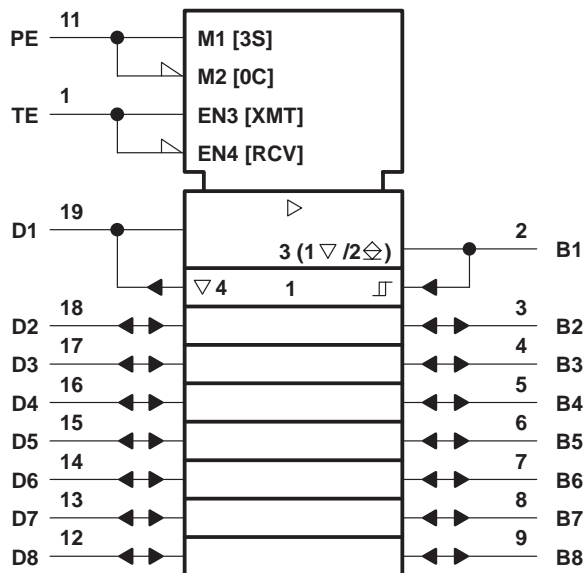
EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant,
Z = high-impedance state

† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and GND.

logic symbol†

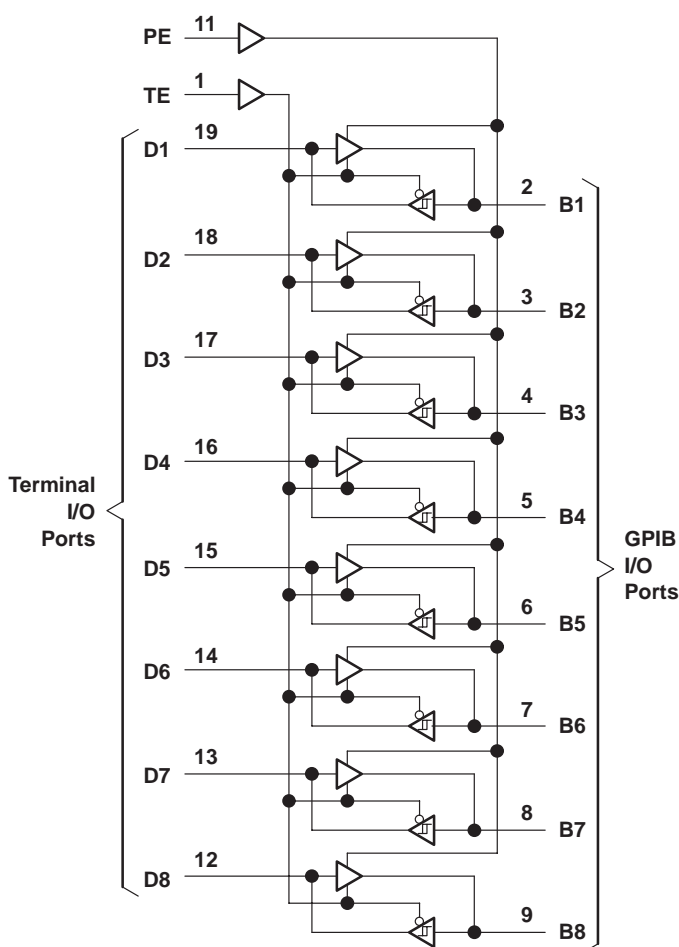


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

▽ Designates 3-state outputs

⊕ Designates open-collector outputs with passive pullup

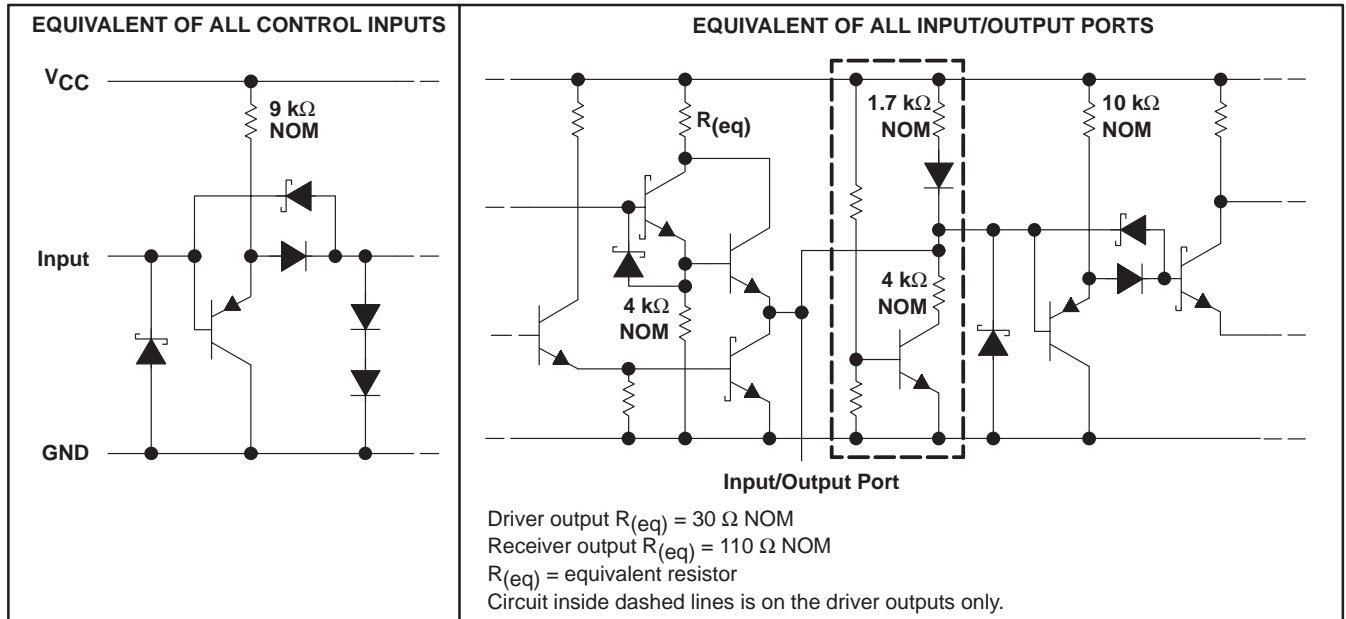
logic diagram (positive logic)



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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Low-level driver output current, I_{OL}	100 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN55ALS160	-55°C to 125°C
SN75ALS160	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J or W package	300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

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SN55ALS160 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	TE and PE at $T_A = -55^\circ\text{C}$ to 125°C	2			V
	Bus and terminal at $T_A = 25^\circ\text{C}$ to 125°C	2			
	Bus and terminal at $T_A = -55^\circ\text{C}$	2.1			
Low-level input voltage, V_{IL}	TE and PE at $T_A = -55^\circ\text{C}$ to 125°C	0.8			V
	Bus and terminal at $T_A = 25^\circ\text{C}$ to -55°C	0.8			
	Bus and terminal at $T_A = 125^\circ\text{C}$	0.7			
High-level output current, I_{OH}	Bus ports with pullups active ($V_{CC} = 5\text{ V}$)	-5.2			mA
	Terminal ports	-800			μA
Low-level output current, I_{OL}	Bus ports	48			mA
	Terminal ports	16			
Operating free-air temperature, T_A		-55		125	$^\circ\text{C}$

SN75ALS160 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}		0.8			V
High-level output current, I_{OH}	Bus ports with pullups active	-5.2			mA
	Terminal ports	-800			μA
Low-level output current, I_{OL}	Bus ports	48			mA
	Terminal ports	16			
Operating free-air temperature, T_A		0		70	$^\circ\text{C}$



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITION†		SN55ALS160			SN75ALS160			UNIT	
				MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IK}	Input clamp voltage	I _I = –18 mA, V _{CC} = MIN		–0.8	–1.5		–0.8	–1.5	V		
V _{hys}	Hysteresis voltage (V _{IT+} – V _{IT–})	Bus					0.4	0.65	V		
		Bus	V _{CC} = 5 V, T _A = –55°C and 25°C	0.4	0.55						
V _{OH} §	High-level output voltage	Terminal	I _{OH} = –800 µA, TE at 0.8 V, V _{CC} = MIN	2.7	3.5		2.7	3.5	V		
		Bus	I _{OH} = –5.2 mA, PE and TE at 2 V, V _{CC} = MIN	2.5	3.3		2.5	3.3			
V _{OL}	Low-level output voltage	Terminal	I _{OL} = 16 mA, TE at 0.8 V, V _{CC} = MIN		0.3	0.5		0.3	0.5	V	
		Bus	I _{OL} = 48 mA, TE at 2 V, V _{CC} = MIN		0.35	0.5		0.35	0.5		
I _I	Input current at maximum input voltage	Terminal	V _I = 5.5 V, V _{CC} = MAX		0.2	100		0.2	100	µA	
I _{IH}	High-level input current	Terminal,	V _I = 2.7 V, V _{CC} = MAX		0.1	20		0.1	20	µA	
I _{IL}	Low-level input current	PE, or TE	V _I = 0.5 V, V _{CC} = MAX		–30	–100		–10	–100	µA	
V _{I/O(bus)}	Voltage at bus port		Driver disabled, V _{CC} = 5 V (SN55 [†])	I _{I(bus)} = 0	2.5	3	3.7	2.5	3	3.7	V
				I _{I(bus)} = –12 mA			–1.5			–1.5	
I _{I/O(bus)}	Current into bus port	Power on	Driver disabled, V _{CC} = 5 V (SN55 [†])	V _{I(bus)} = –1.5 V to 0.4 V	–1.3			–1.3		mA	
				V _{I(bus)} = 0.4 V to 2.5 V	0	–3.2		0	–3.2		
				V _{I(bus)} = 2.5 V to 3.7 V			2.5		2.5		
				V _{I(bus)} = 3.7 V to 5 V	0	2.5		0	2.5		
				V _{I(bus)} = 5 V to 5.5 V	0.7	2.5		0.7	2.5		
		Power off	V _{CC} = 0	V _{I(bus)} = 0 to 2.5 V		40		40	µA		
I _{OS}	Short-circuit output current	Terminal	V _{CC} = MAX	–15	–35	–75	–15	–35	–75	mA	
		Bus	V _{CC} = MAX	–25	–50	–125	–25	–50	–125		
I _{CC}	Supply current		No load, V _{CC} = MAX	Terminal outputs low and enabled		42	56		42	65	mA
				Bus outputs low and enabled		52	85		52	80	
C _{I/O(bus)}	Bus-port capacitance	V _{CC} = 0 to 5 V, V _{I/O} = 0 to 2 V, f = 1 MHz			30			30	pF		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ V_{OH} applies to 3-state outputs only.

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switching characteristics at $V_{CC} = 4.75\text{ V}$, 5 V , and 5.25 V , $C_L = 50\text{ pF}$ (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A †	MIN	TYP‡	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	See Figure 1	25°C		10	17	ns
					Full range			20	
t _{PHL}	Propagation delay time, high- to low-level output				25°C		10	14	
					Full range			16	
t _{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	See Figure 2	25°C		8	15	ns
					Full range			18	
t _{PHL}	Propagation delay time, high- to low-level output				25°C		8	15	
					Full range			18	
t _{PZH}	Output enable time to high level	TE	Bus	See Figure 3	25°C		24	30	ns
					Full range			41	
t _{PHZ}	Output disable time from high level				25°C		9	14	
					Full range			16	
t _{PZL}	Output enable time to low level				25°C		16	28	
					Full range			34	
t _{PLZ}	Output disable time from low level				25°C		12	19	
					Full range			24	
t _{PZH}	Output enable time to high level	TE	Terminal	See Figure 4	25°C		24	36	ns
					Full range			50	
t _{PHZ}	Output disable time from high level				25°C		10	18	
					Full range			23	
t _{PZL}	Output enable time to low level				25°C		15	26	
					Full range			30	
t _{PLZ}	Output disable time from low level				25°C		15	24	
					Full range			31	
t _{en}	Output pullup enable time	PE	Bus	See Figure 5	25°C		16	24	ns
					Full range			25	
t _{dis}	Output pullup disable time				25°C		9	16	
					Full range			20	

† Full range is -55°C to 125°C .

‡ All typical values are at $V_{CC} = 5\text{ V}$.

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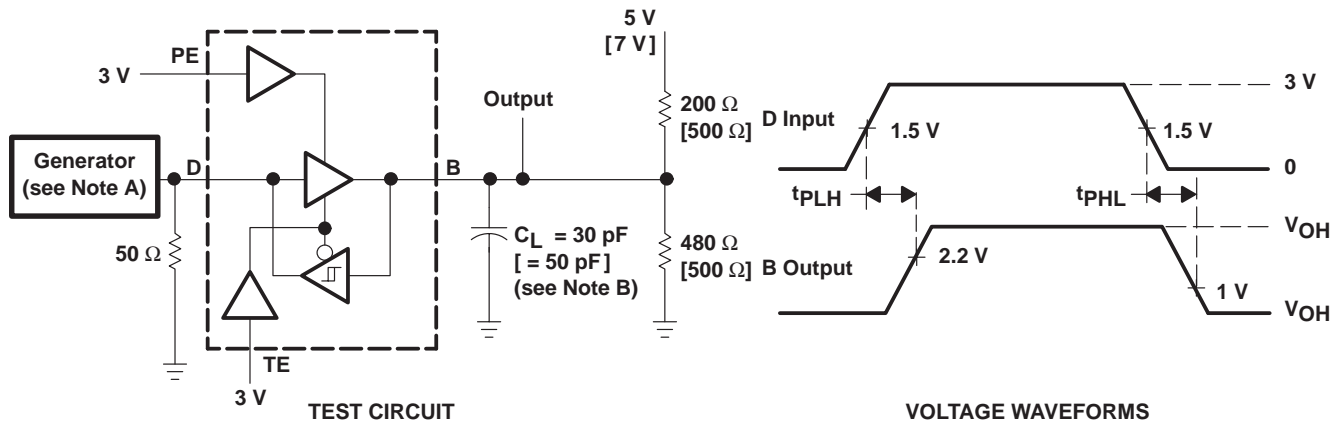
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switching characteristics over recommended range of operating free-air temperature, $V_{CC} = 5\text{ V}$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	$C_L = 30\text{ pF}$, See Figure 1	7	8	20	ns
t_{PHL}	Propagation delay time, high- to low-level output							
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	$C_L = 30\text{ pF}$, See Figure 2	7	9	14	ns
t_{PHL}	Propagation delay time, high- to low-level output							
t_{PZH}	Output enable time to high level	TE	Bus	$C_L = 15\text{ pF}$, See Figure 3	19	5	30	ns
t_{PHZ}	Output disable time from high level							
t_{PZL}	Output enable time to low level							
t_{PLZ}	Output disable time from low level							
t_{PZH}	Output enable time to high level	TE	Terminal	$C_L = 15\text{ pF}$, See Figure 4	13	12	20	ns
t_{PHZ}	Output disable time from high level							
t_{PZL}	Output enable time to low level							
t_{PLZ}	Output disable time from low level							
t_{en}	Output pullup enable time	PE	Bus	$C_L = 15\text{ pF}$, See Figure 5	11	6	22	ns
t_{dis}	Output pullup disable time							

† Typical values are at $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



[] denotes the SN55ALS160 military test conditions.

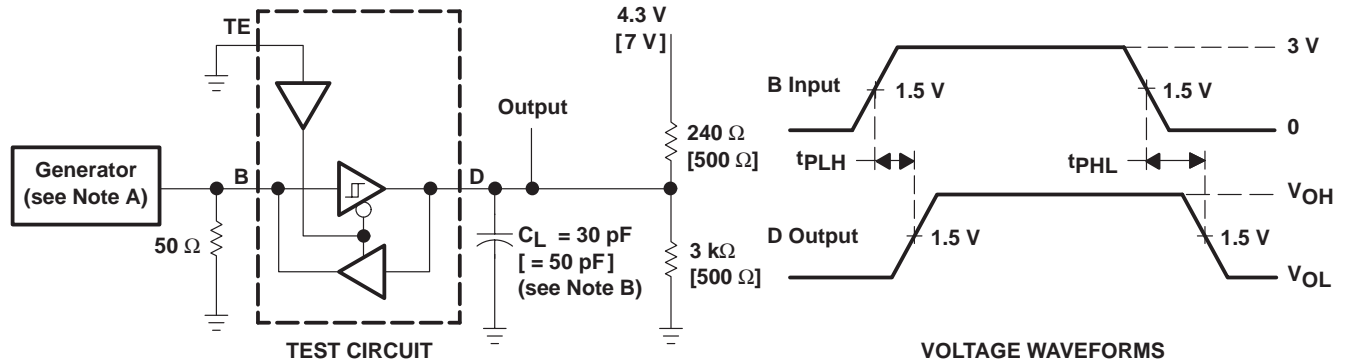
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$, $Z_0 = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

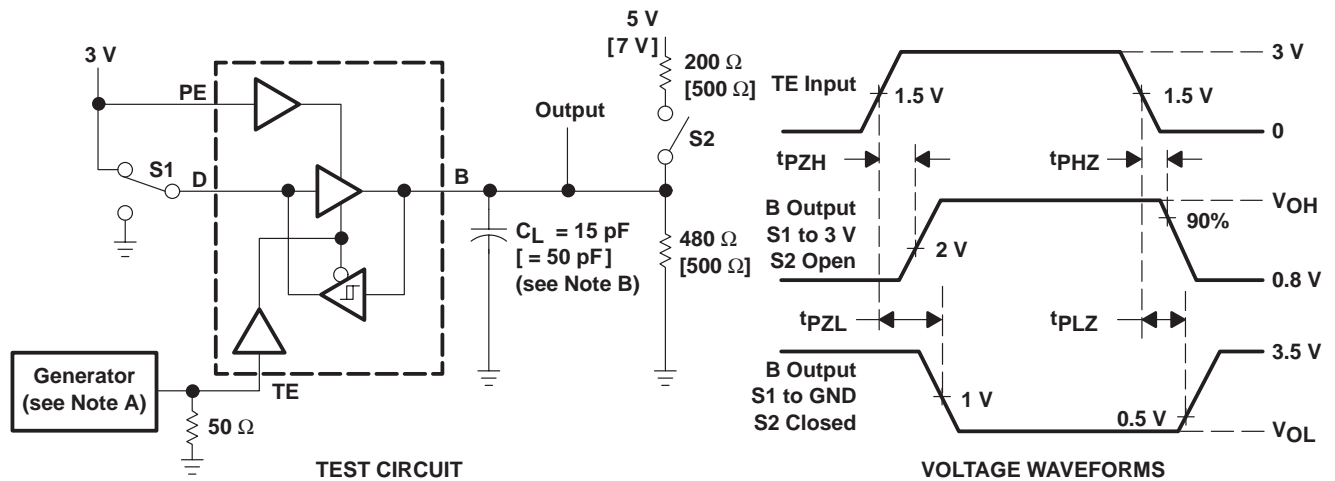


[] denotes the SN55ALS160 military test conditions.

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

B. C_L includes probe and jig capacitance.

Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms



[] denotes the SN55ALS160 military test conditions.

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

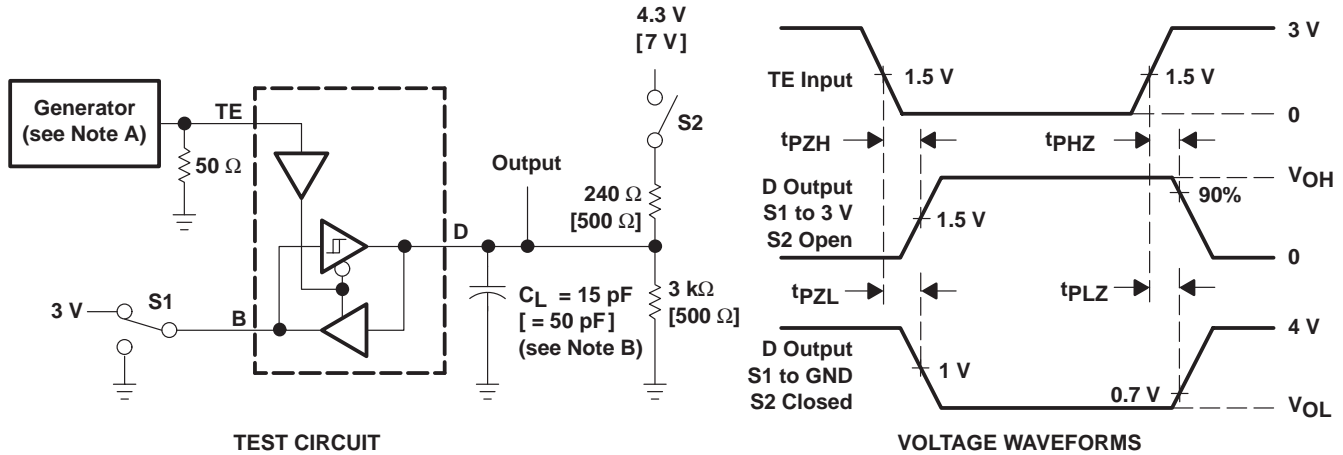
B. C_L includes probe and jig capacitance.

Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

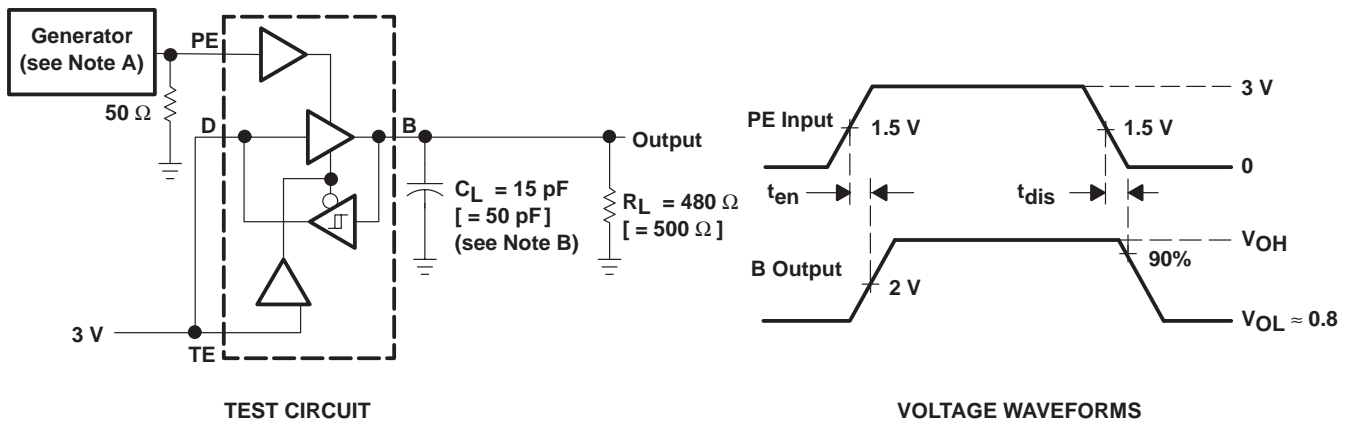


[] denotes the SN55ALS160 military test conditions.

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

B. C_L includes probe and jig capacitance.

Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms



[] denotes the SN55ALS160 military test conditions.

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

B. C_L includes probe and jig capacitance.

Figure 5. PE-to-Bus Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

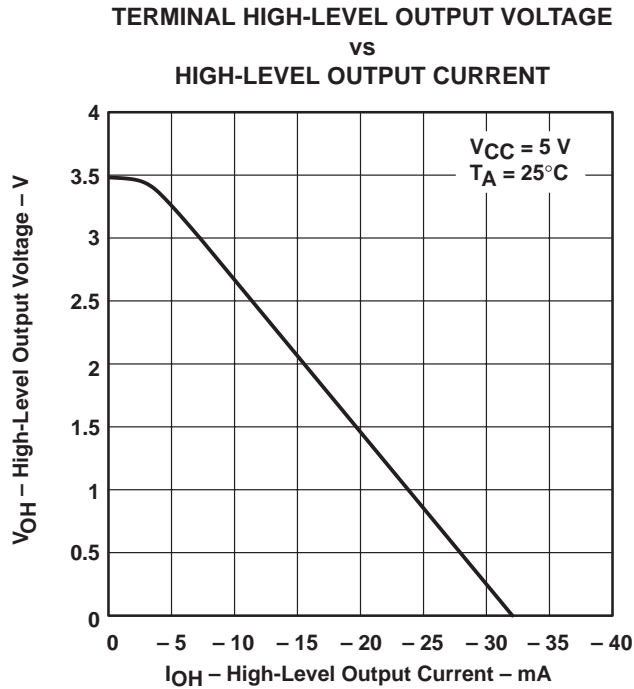


Figure 6

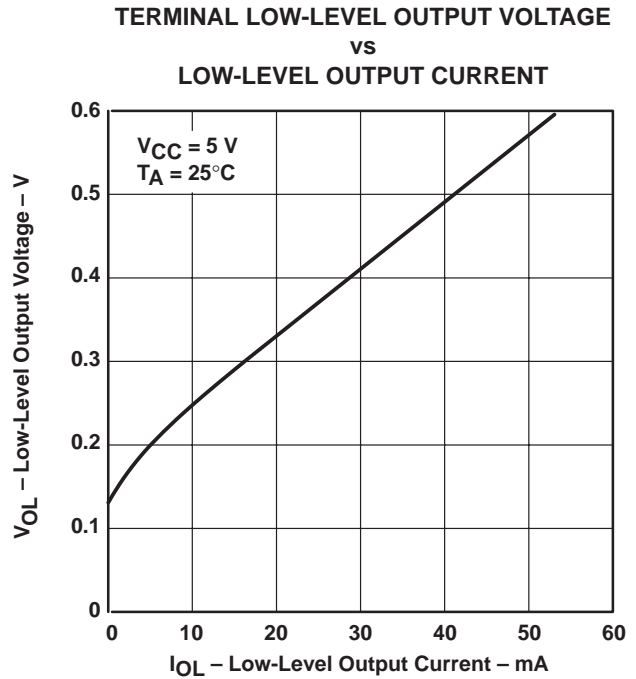


Figure 7

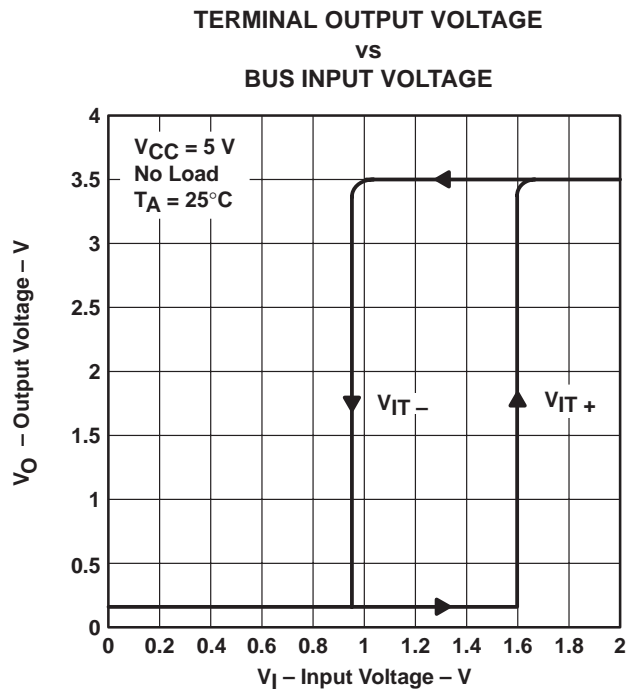
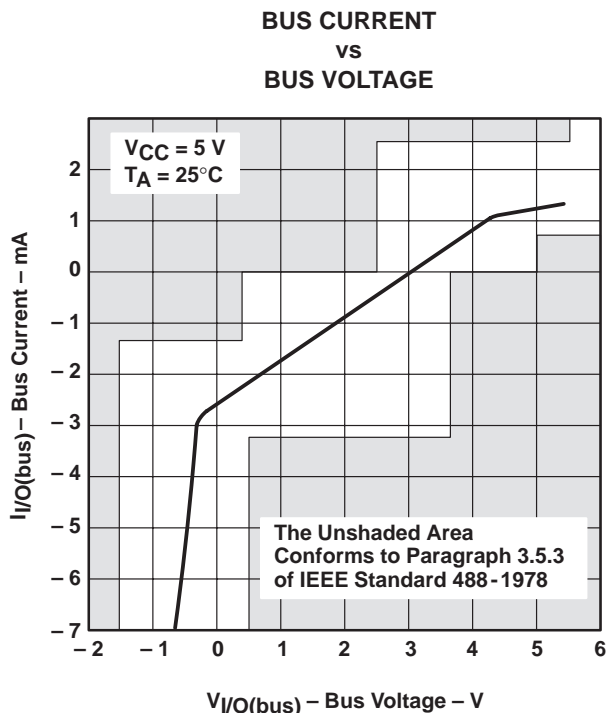
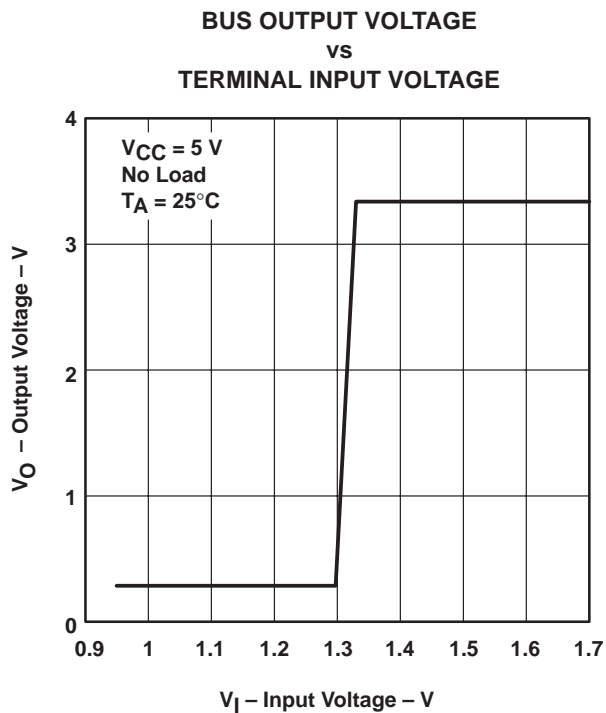
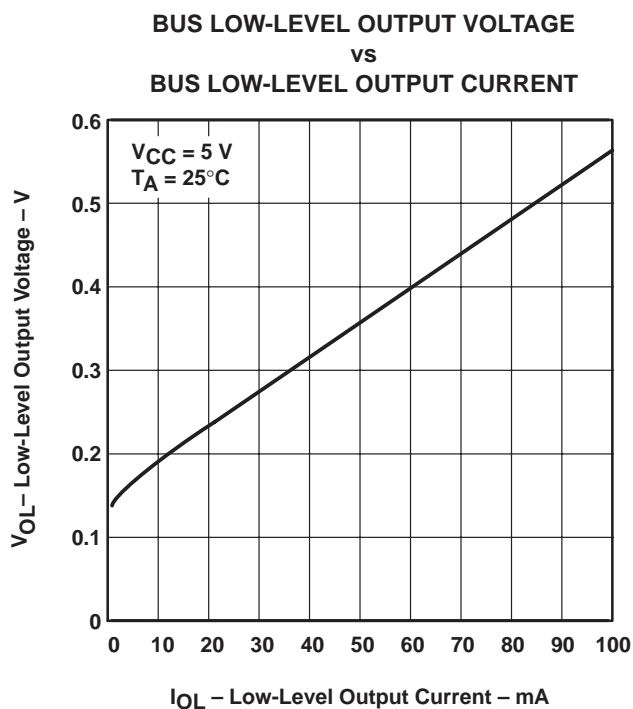
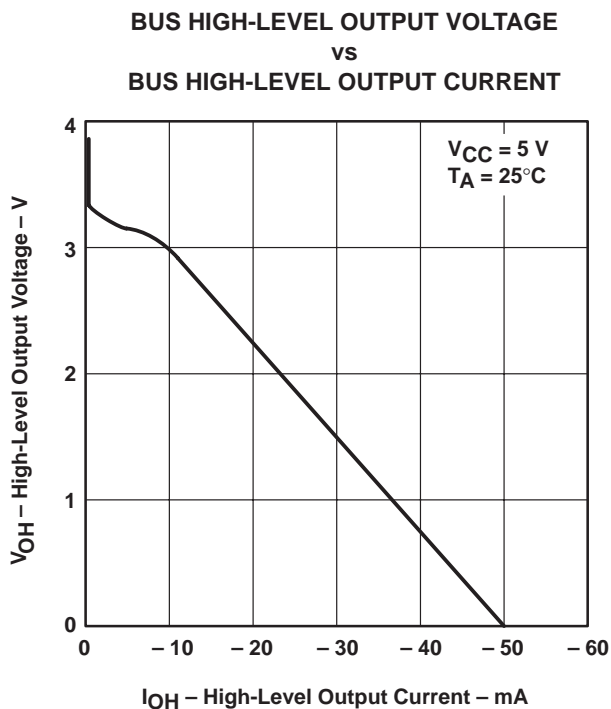


Figure 8

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TYPICAL CHARACTERISTICS



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