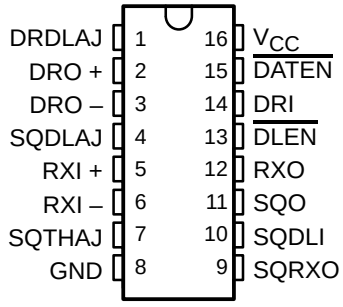
- **IEEE 802.3 1BASE5 Driver and Receiver**
- **On-Chip Receiver Squelch With Adjustable Threshold**
- **Adjustable Squelch Delay**
- **Direct TTL-Level Squelch Output**
- **Squelch Circuit Allows for External Noise Filtering**
- **Two Driver-Enable Options**
- **On-Chip Start-of-Idle Detection and Disable**
- **Driver Provides 2-V Minimum into a 50-Ω Differential Load Allowing for Use With Doubly-Terminated Lines and Multipoint Architectures**
- **On-Chip Driver Slew-Rate Control for Very Closely Matched Output Rise and Fall Times**

N PACKAGE
(TOP VIEW)



Function Tables

DRIVER

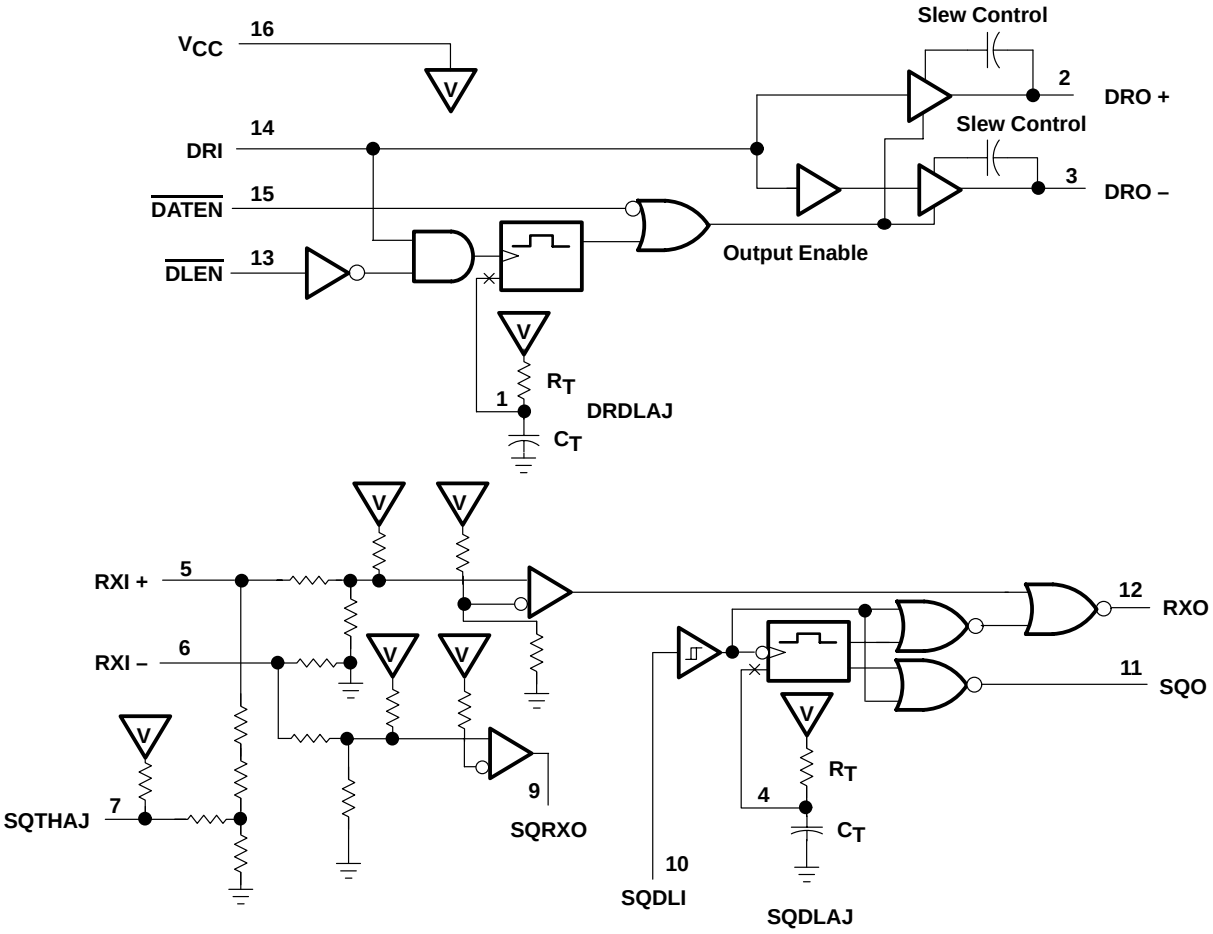
INPUTS			OUTPUTS	
DRI	$\overline{\text{DATEN}}$	$\overline{\text{DLEN}}$	DRO +	DRO –
L	L	X	L	H
H	L	X	H	L
X	H	H	Z	Z
H	H	L	H †	L †
L	H	L	L ‡	H ‡

RECEIVER§

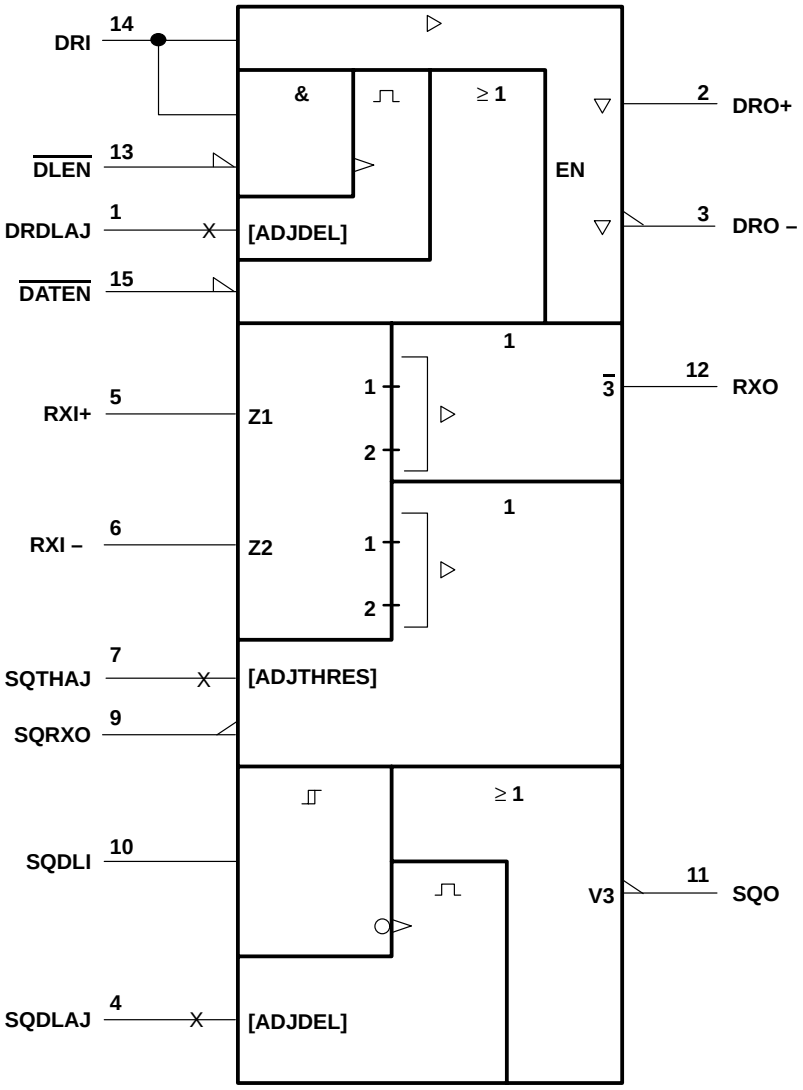
CONDITION	INPUTS		OUTPUTS	
	RXI +	RXI –	RXO	SQO
No active signal ¶	X	X	H	H
Active signal ¶	L	H	L	L
	H	L	H	L

† This condition is valid during the time period set by DRDLAJ following a rising transition on DRI. Following this, when a subsequent positive transition does not occur on DRI, the outputs go to the high-impedance state.
‡ This condition is valid when it occurs within the enable time set by DRDLAJ after a rising transition on DRI. Otherwise, the outputs are in the high-impedance state.
§ Pins 9 and 10 are tied together.
¶ An active signal is one that has an amplitude greater than the threshold level set by SQTHAJ.

logic diagram (positive logic)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN75061 is a single-channel driver/receiver pair designed for use in IEEE 802.3, 1BASE5 applications as well as other general data communications circuits. The SN75061 offers both a driver and a receiver that are easily configured for use with a variety of controllers and data encoder/decoders.

The receiver features a full analog squelch circuit with an adjustable threshold and a programmable squelch delay. Internal nodes of the squelch circuitry are brought out to external connections to allow for the insertion of noise-filtering circuitry of the designer's choice.

As with the receiver, the driver offers a variety of implementation options. Driver enabling may be directly controlled by an external logic input or by use of an on-chip one-shot that is retriggered as long as data is being sent to the driver. The driver then automatically goes to the high-impedance state when end-of-packet common phrase occurs. The driver features internal slew-rate control for optimal matching of rise and fall times allowing for reduction of driver-induced jitter.

receiver

The SN75061 receiver implements full analog squelch functions by integrating both a separate, parallel squelch receiver with an externally programmable threshold, and a programmable one-shot. The output of the squelch receiver and the input to the high-level, dc-triggered one-shot are brought out to external connections. These pins can be shorted for direct implementation or used for the insertion of noise-filtering circuitry of the implementer's design. The receiver one-shot can be effectively bypassed by applying a high logic level to SQDLI. The squelch threshold may be set externally by applying an external voltage set to a level that is –2 times the desired threshold voltage. When SQTHAJ is left open, the squelch receiver defaults to its internal preset value of –600 mV. The receiver also outputs a high logic squelch signal when there is not any active data present at the receiver inputs. When data is not present on the transmission line, the receiver output assumes a high level. The unsquelch duration is set externally with an R-C combination at SQDLAJ.

driver

The driver offers a variety of implementation options. Driver enabling may be controlled directly by an active-low, external logic input on $\overline{\text{DATEN}}$ or by use of another on-chip one-shot that retriggers with positive-going transitions on the driver input line. When positive transition does not occur within the pulse duration set by an external R-C combination, the one-shot times out and the driver is automatically put into a high-impedance state. When operating in the delay-enable mode, the 2-bit-time, high-level, start-of-idle pulse prescribed by IEEE 802.3 1BASE5 causes the one-shot to time out and automatically place the driver outputs in the high-impedance state. This delay time is also adjustable for use in other applications. The driver implements an output slew-rate control that is internally set for nominally 40 mV/ns. (This is roughly a 100-ns peak-to-peak differential transition time.) The driver outputs are capable of driving a 50-Ω differential load with a minimum output level of 2 V. Short-circuit output current is greater than 100 mA.

Terminal Functions

PIN NAME	PIN NO.	DESCRIPTION
$\overline{\text{DATEN}}$	15	Driver data enable. When this sign is low, driver outputs are in an active state. When the signal is high, the driver outputs are in a high-impedance state when $\overline{\text{DLEN}}$ is also high.
$\overline{\text{DLEN}}$	13	Driver delay enable. When this signal is low and $\overline{\text{DATEN}}$ is high, the driver outputs are active for a period of time set by DRDLAJ after a positive-going transition on DRI. When there is not any active data on DRI, the outputs are in a high-impedance state.
DRDLAJ	1	Driver delay adjust is a connection for the external R-C combination that determines the duration of the driver output active state after a positive transition on DRI when $\overline{\text{DLEN}}$ is low and $\overline{\text{DATEN}}$ is high.
DRI	14	Driver data input
DRO+	2	Noninverting driver output
DRO–	3	Inverting driver output
GND	8	Ground. Common for all voltages
RXI+	5	Noninverting receiver input
RXI–	6	Inverting receiver input
RXO	12	Main receiver input
SQDLAJ	4	Squelch delay adjust is a connection for an external R-C combination that determines the duration of the receiver unsquelch after a negative-going transition on SQDLI.
SQDLI	10	Squelch delay input is the input to the one-shot that controls the duration of the receiver unsquelch period. The main receiver output remains unsquelched as long as SQDLI is held high. Timing of the unsquelch period begins on the high-to-low transition of SQDLI.
SQO	11	Squelch output is high while the receiver is squelched.
SQRXO	9	Squelch receiver output is high only when the differential receiver input exceeds the threshold set by SQTHAJ.
SQTHAJ	7	Squelch receiver threshold adjust. The voltage at this input determines the threshold of the squelch receiver in a ratio of –2, SQTHAJ to threshold. When the receiver is left open, the squelch receiver threshold defaults to –600 mV.
V_{CC}	16	Supply-voltage input

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I (any logic input) . . . . . 7 V
Receiver differential input voltage . . . . . ±25 V
Receiver input voltage . . . . . ±15 V
Driver output voltage . . . . . –0.5 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 1150 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: For operation above 25°C free-air temperature, derate to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Driver high-level input voltage, V_{IH}	2			V
Driver low-level input voltage, V_{IL}			0.8	V
Receiver common-mode input voltage, V_{IC} (see Note 2)	–2.5		5	V
Driver high-level output current, I_{OH}			–150	mA
Driver low-level output current, I_{OL}			150	mA
External timing resistance, R_{ext}	5		260	kΩ
External timing capacitance, C_{ext}		No restriction		
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, in which the less-positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage V_{IC} and threshold levels V_{IT+} and $V_{IT–}$.

electrical characteristics over recommended operating free-air temperature and supply voltage ranges (unless otherwise noted)

driver

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_{OD}	Differential output voltage	R_L = 50 Ω		2	2.4	3.3	V
		R_L = 115 Ω				3.65	
ΔV_{OD}	Change in differential output voltage for a change in logic input state					50	mV
I_{IH}	High-level input current	V_I = 2 4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V		±100		–35	μA
I_{OS}	Short-circuit output current	V_O = 0 or 6 V,	V_I = 0.8 V or 2.5 V			±300	mA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V	V_{OC} = 10 V			100	μA
			V_{OC} = 0			–100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature and supply voltage ranges (unless otherwise noted) (continued)

receiver

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage, squelch delay		I_I = –18 mA				–1.5	V
V_{IT+}	Positive-going input threshold voltage		V_O = 2.7 V,	I_O = –0.4 mA			50	mV
V_{IT-}	Negative-going input threshold voltage		V_O = 0.5 V,	I_O = 16 mA	–50‡			mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					50		mV
V_{IC}	Common-mode input voltage						5	V
V_{OH}	High-level output voltage	RXO	V_{CC} = 4.75 V, SQDLAJ at 0.8 V	I_{OH} = –400 μA,	2.7			V
		SQO			2.7	3.5		
		SQRXO	V_{CC} = 4.75 V, $V_{ID(RXI)}$ = –0.7 V,	I_{OH} = –20 μA, SQDLAJ open	2.7	4.65		
V_{OL}	Low-level output voltage	RXO	V_{CC} = 4.75 V, SQDLAJ at 2 V	I_{OL} = 8 mA			0.45	V
		SQO		I_{OL} = 16 mA			0.5	
				I_{OL} = 8 mA		0.35	0.5	
		SQRXO	V_{CC} = 4.75 V, $V_{ID(RXI)}$ = 50 mV	I_{OL} = 8 mA			0.45	
				I_{OL} = 16 mA			0.5	
I_{IH}	High-level input current	SQDLI	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current		V_I = 0.5 V				–35	μA
I_{OS}	Short-circuit output current	RXO	V_{CC} = 5.25 V,	V_O = 0	–15		–85	mA
		SQO			–15		–100	
		SQRXO	V_{CC} = 5 V,	V_O = 0	–0.8	–1	–1.2	
r_i	Input resistance					10		kΩ
$V_{IT-(sq)}$	Squelch preset input threshold voltage		V_{CC} = 5 V, SQTHAJ open	V_{IC} = 1.5 V to 3.5 V	–525	–600	–675	mV
				V_{IC} = –2.5 V to 1.5 V or 3.5 V to 5 V	–500		–700	mV
	Ratio of SQTHAJ input voltage to actual squelch threshold voltage		SQTHAJ at 200 mV to 4 V		–1.9		–2.1	

driver and receiver

I_{CC}	Supply current	V_{CC} = 5.25 V, No load	Driver outputs disabled,		70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage V_{IC} and threshold levels V_{IT+} and V_{IT-}.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

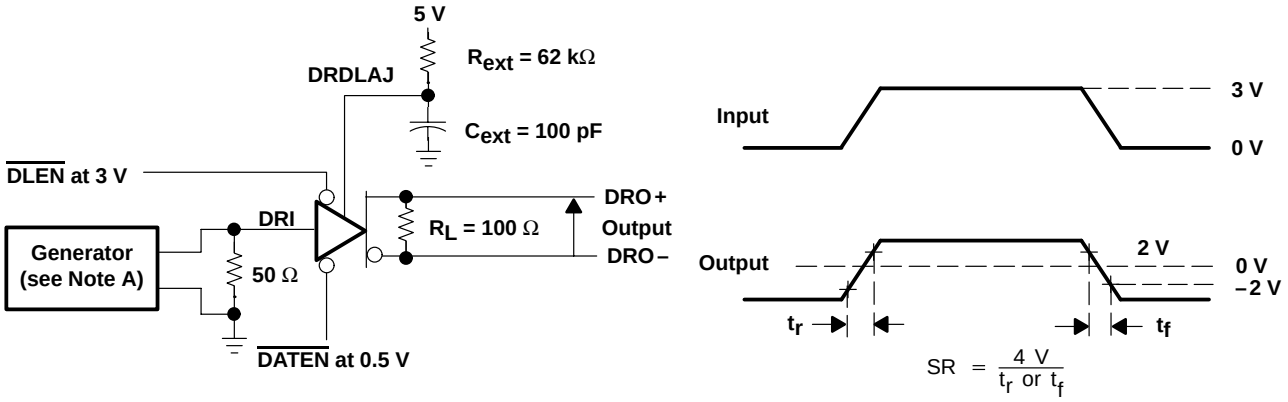
driver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Differential-output slew rate	V_O = –2 V to 2 V, R_L =100 Ω (differential), See Figure 1	28	40	52	mV/ns
$t_{d(OD)}$	Differential-output delay time ($t_{d(OD)+}$ and $t_{d(OD)-}$)	C_L= 15 pF, R_L =100 Ω (differential), See Figure 2			160	ns
	Differential-output delay time difference ($t_{d(OD)+} - t_{d(OD)-}$)	R_L =100 Ω (differential), See Figure 2			5	ns
t_{PHZ}	Disable time from $\overline{\text{DATEN}}$	See Figure 3, 4, and 5			220	ns
t_{PLZ}					300	ns
t_{PZH}	Enable time from $\overline{\text{DATEN}}$				220	ns
t_{PZL}					290	ns
t_{PZH}	Enable time from $\overline{\text{DLEN}}$				250	ns
$t_{w(en)}$	Enable pulse duration time (with DLEN low)	C_{ext} = 100 pF, R_{ext} = 62 kΩ, See Figure 6	2	2.5	3	µs

receiver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{en(RX)}$	Receiver enable time	Squelch off, See Figure 7		117		ns
t_{PLH}	Propagation delay time, low- to high level output	Squelch off, See Figure 8		20	35	ns
t_{PHL}	Propagation delay time, high- to low level output	Squelch off, See Figure 8		22	35	ns
$t_{d(unsq)}$	Unsquelch delay time	C_{ext} = 50 pF, R_{ext} = 51 kΩ, See Figure 9	1	1.2	1.45	µs
		C_{ext} = 15 pF, R_{ext} = 6.8 kΩ, See Figure 9			180	ns

PARAMETER MEASUREMENT INFORMATION

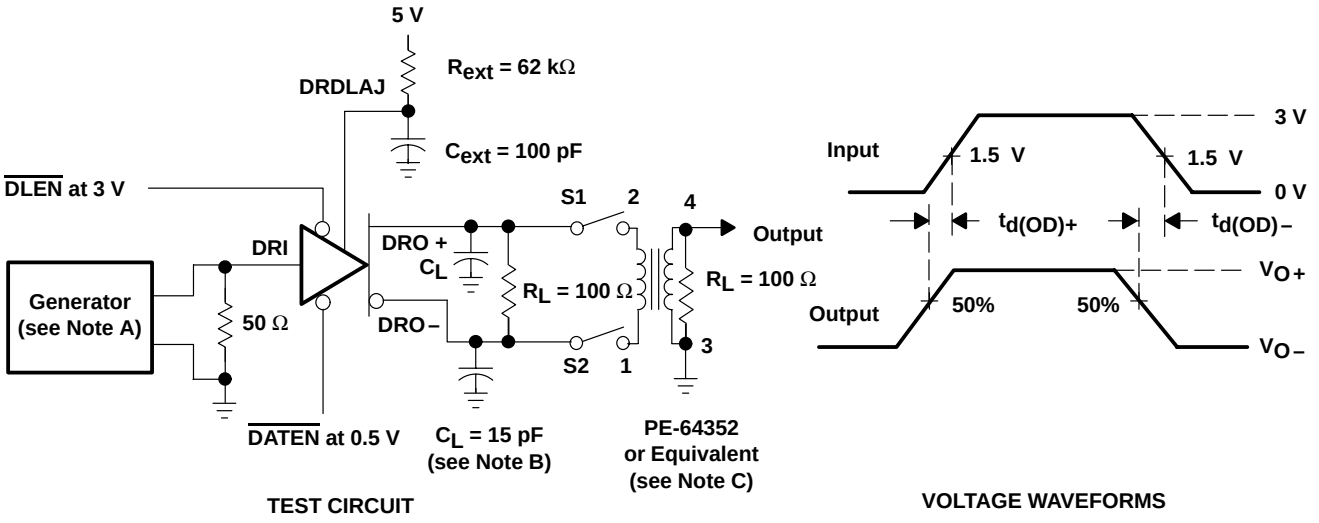


TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

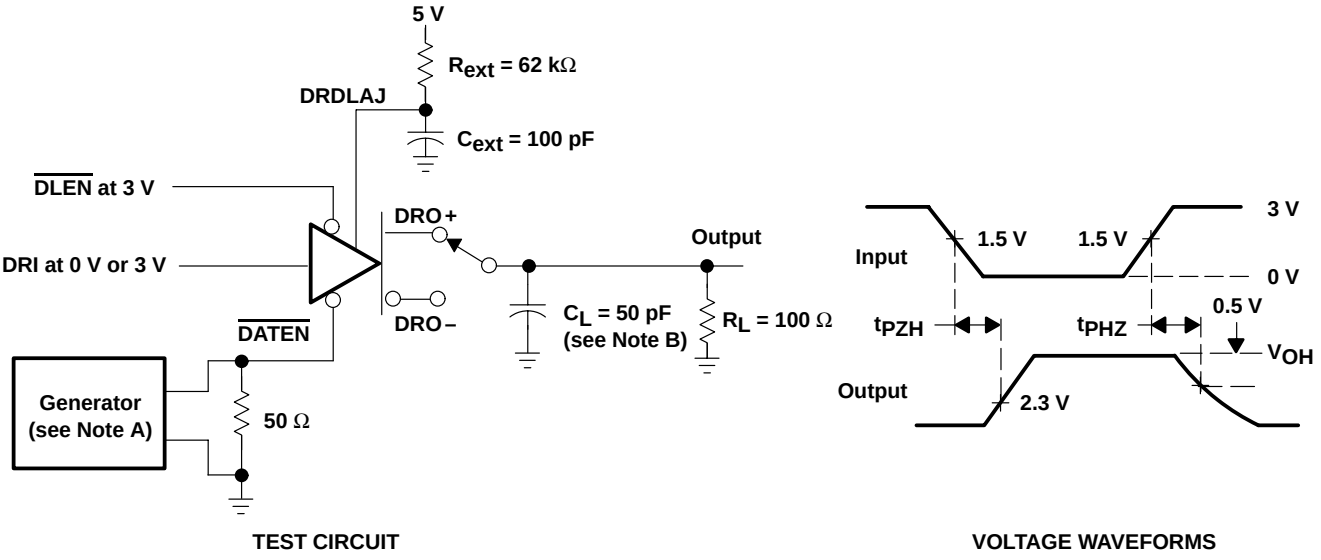
Figure 1. Test Circuit and Voltage Waveforms for Driver Slew Rate

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. When measuring differential-output delay time difference, switches S1 and S2 are closed (Isolation transformer from Pulse Engineering P/N PE-64352).

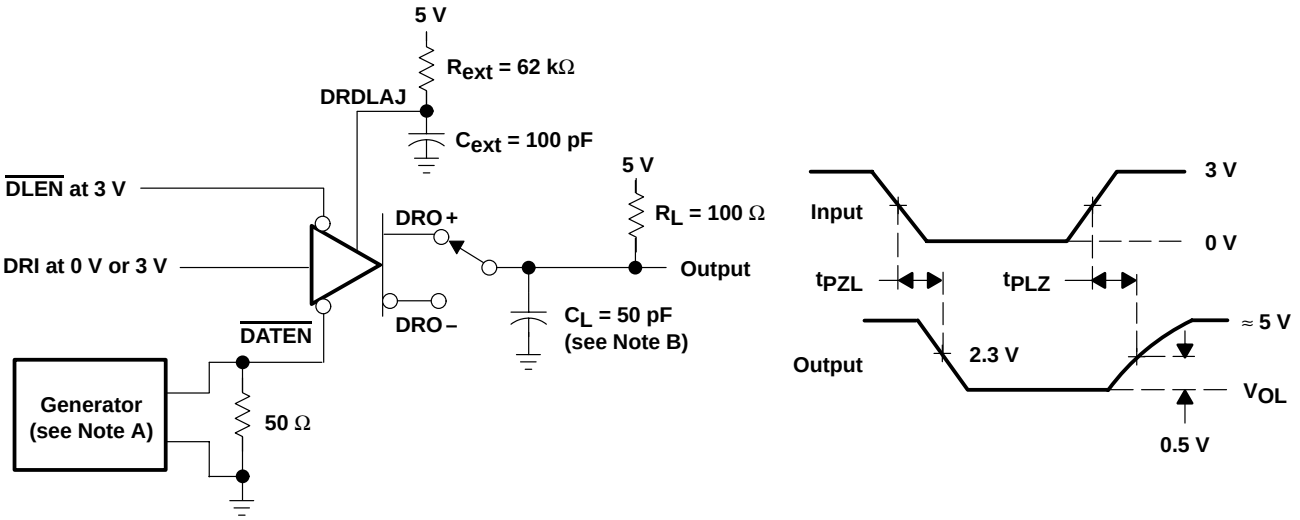
Figure 2. Test Circuit and Voltage Waveforms for Driver Differential Delay Time



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Voltage Waveforms for Driver Enable and Disable Time

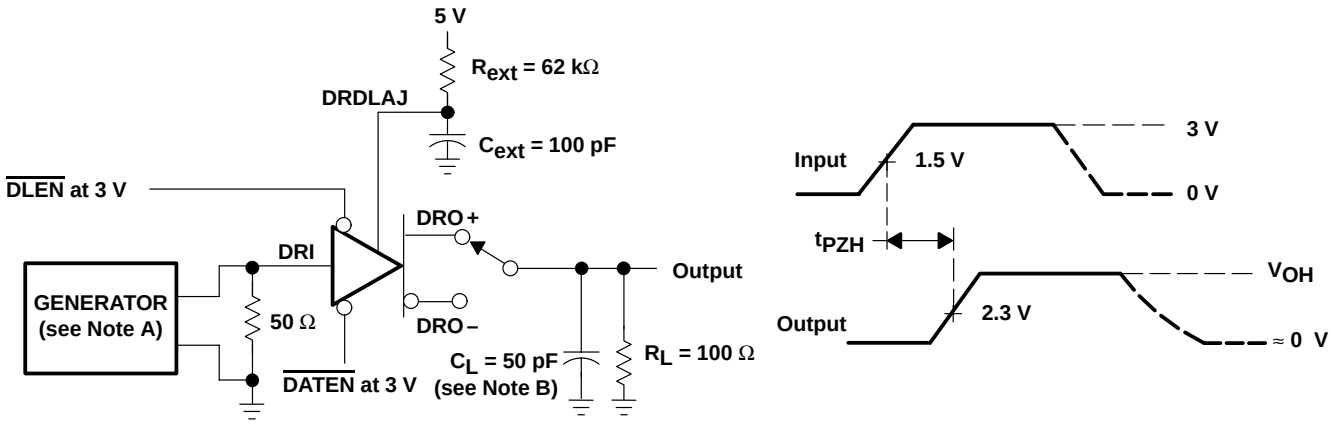
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 200 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. Test Circuit and Voltage Waveforms for Driver Enable and Disable Time

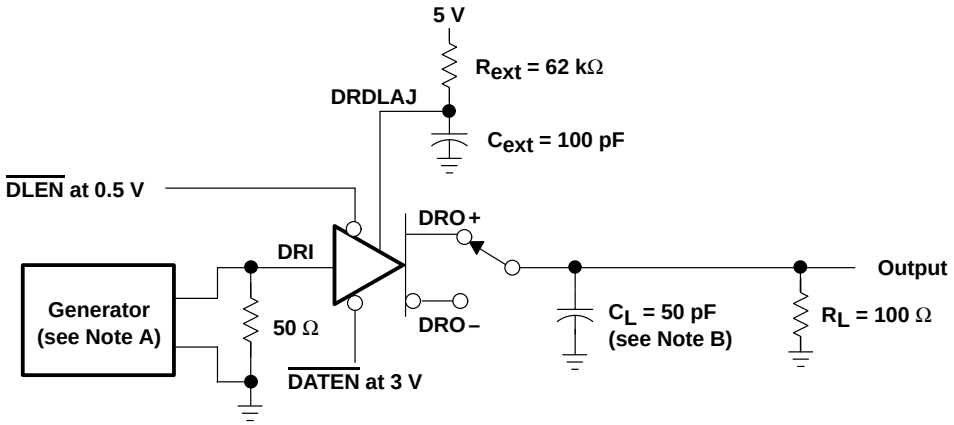


TEST CIRCUIT VOLTAGE WAVEFORMS

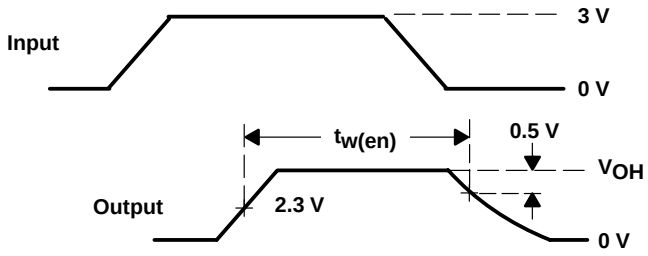
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 5. Test Circuit and Voltage Waveforms for Enable Time From Delay Enable

PARAMETER MEASUREMENT INFORMATION



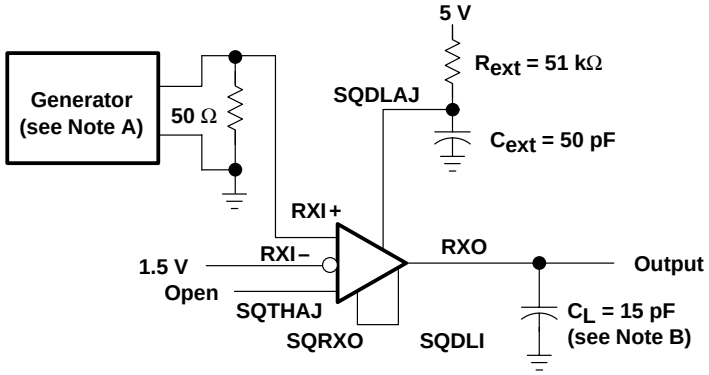
TEST CIRCUIT



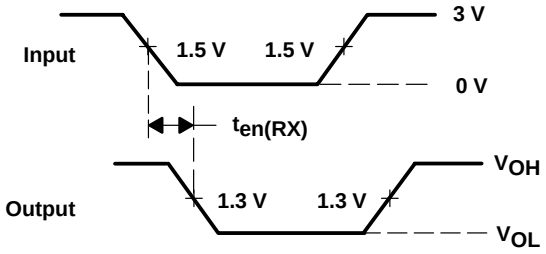
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 200 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 6. Test Circuit and Voltage Waveforms for Enable Pulse Duration With Delay Enable Low



TEST CIRCUIT

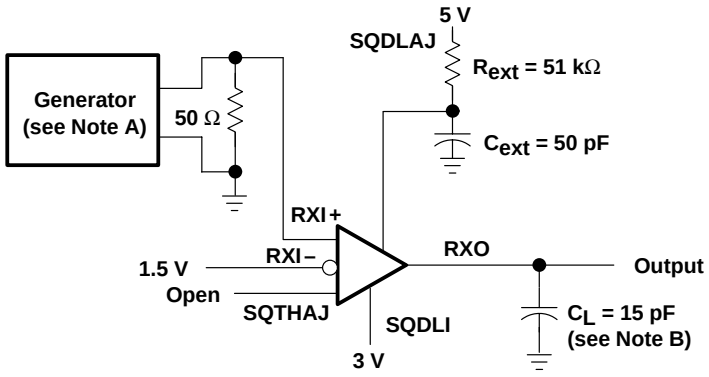


VOLTAGE WAVEFORMS

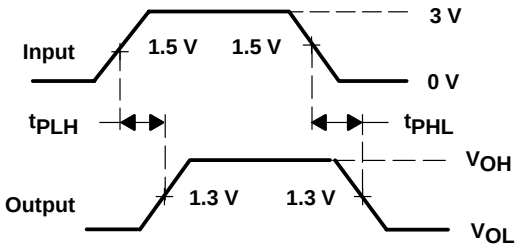
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Test Circuit and Voltage Waveforms for Receiver Enable (Unsquelch) Time

PARAMETER MEASUREMENT INFORMATION



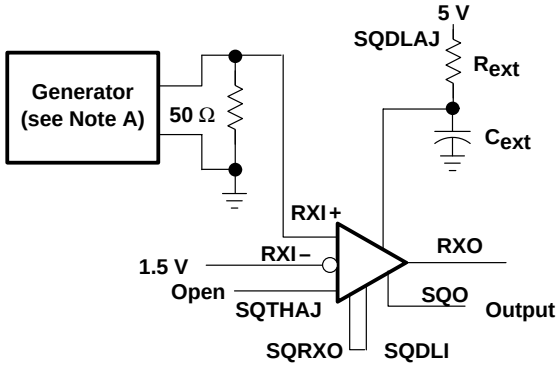
TEST CIRCUIT



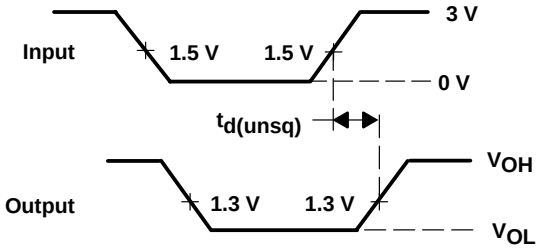
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 8. Test Circuit and Voltage Waveforms for Receiver Propagation Delay Time



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 9. Test Circuit and Voltage Waveforms for Unsquelch Duration Time

NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 100 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.