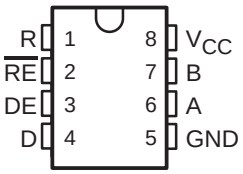
SLLS040E – AUGUST 1987 – REVISED MAY 1995

- **Meet or Exceed the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendations V.11 and X.27**
- **Designed and Tested to Operate at Data Rates up to 35 MBaud**
- **SN65ALS176 Operating Temperature –40°C to 85°C**
- **Three Skew Limits Available:**
  - **′ALS176 . . . 10 ns**
  - **′ALS176A . . . 7.5 ns**
  - **′ALS176B . . . 5 ns**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirements 30 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Thermal Shutdown Protection**
- **Driver Positive- and Negative-Current Limiting**
- **Receiver Input Hysteresis**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Receiver Open-Circuit Fail-Safe Design**

D OR P PACKAGE
(TOP VIEW)



description

The SN65ALS176 and SN75ALS176 series differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendations V.11 and X.27.

The SN65ALS176 and SN75ALS176 series combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN65ALS176 is characterized for operation from –40°C to 85°C, and the SN75ALS176 series is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	$t_{sk(LIM)}$†	PACKAGE	
		SMALL OUTLINE (D)‡	PLASTIC DIP (P)
0°C to 70°C	10 7.5 5	SN75ALS176D SN75ALS176AD SN75ALS176BD	SN75ALS176P SN75ALS176AP SN75ALS176BP
–40°C to 85°C	15	SN65ALS176D	SN65ALS176P

† $t_{sk(LIM)}$ This is the maximum range that the driver or receiver delay times vary over temperature, V_{CC}, and process (device to device).

‡ The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN75ALS176DR).

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

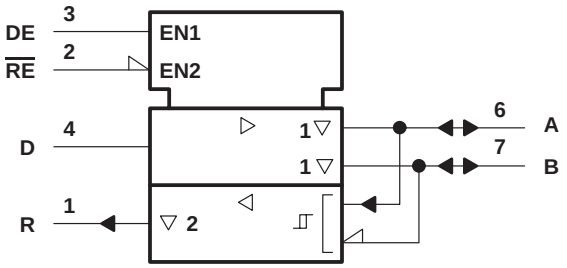
H = high level, L = low level, X = irrelevant,
Z = high impedance

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs open	L	H

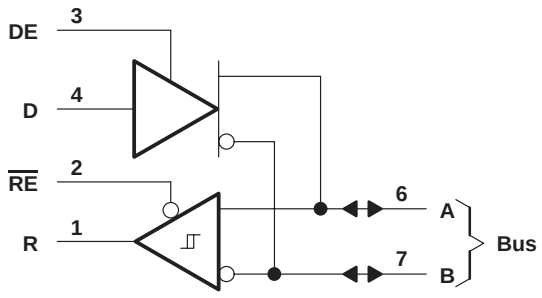
H = high level, L = low level, X = irrelevant,
Z = high impedance

logic symbol§

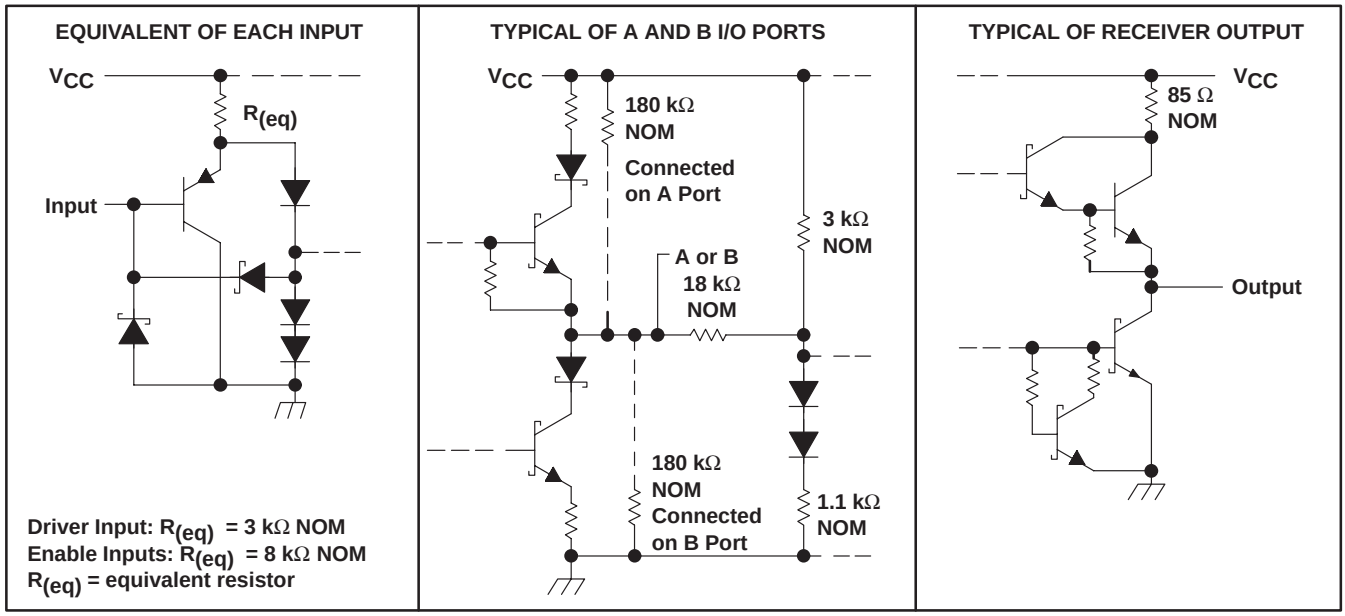


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage range at any bus terminal . . . . . –7 V to 12 V
Enable input voltage, V_I . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65ALS176 . . . . . –40°C to 85°C
SN75ALS176 series . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65ALS176	−40		85	°C
	SN75ALS176	0		70	

NOTE 2: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1} or 2§			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = –7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage¶	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3 –1	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage¶					±0.2	V
I_O	Output current	Outputs disabled, See Note 3	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current	V_O = –4 V	SN65ALS176			–250	mA
		V_O = –6 V	SN75ALS176				
		V_O = 0				–150	
		V_O = V_{CC}				250	
		V_O = 8 V					
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
¶ $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.

NOTE 3: This applies for both power on and power off; refer to ANSI standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω, C_L = 50 pF, See Figure 3			15	ns
$t_{sk(p)}$	Pulse skew‡			0	2	ns
$t_{t(OD)}$	Differential output transition time			8		ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, C_L = 50 pF, See Figure 4			80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, C_L = 50 pF, See Figure 5			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, C_L = 50 pF, See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, C_L = 50 pF, See Figure 5			30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	’ALS176	R_L = 54 Ω, C_L = 50 pF, See Figure 3	3	8	13	ns
		’ALS176A		4	7	11.5	
		’ALS176B		5	8	10	
$t_{sk(p)}$	Pulse skew‡		R_L = 54 Ω, C_L = 50 pF, See Figure 3		0	2	ns
$t_{sk(lim)}$	Skew limit§	’ALS176	R_L = 54 Ω, C_L = 50 pF, See Figure 3			10	ns
		’ALS176A				7.5	
		’ALS176B				5	
$t_{t(OD)}$	Differential output transition time		R_L = 54 Ω, C_L = 50 pF, See Figure 3		8		ns
t_{PZH}	Output enable time to high level		R_L = 110 Ω, C_L = 50 pF, See Figure 4		23	50	ns
t_{PZL}	Output enable time to low level		R_L = 110 Ω, C_L = 50 pF, See Figure 5		14	20	ns
t_{PHZ}	Output disable time from high level		R_L = 110 Ω, C_L = 50 pF, See Figure 4		20	35	ns
t_{PLZ}	Output disable time from low level		R_L = 110 Ω, C_L = 50 pF, See Figure 5		8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.
§ Skew limit is the maximum difference in propagation delay times between any two channels of one device.

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$	None	V_t (test termination measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	None
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	–0.2‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OH} = –400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, See Figure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
V_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = –7 V			–0.8	
I_{IH}	High-level-enable input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level-enable input current	V_{IL} = 0.4 V				–100	μA
r_I	Input resistance			12	20		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	–15		–85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 4: This applies for both power on and power off. Refer to ANSI Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{pd}	Propagation time		V_{ID} = –1.5 V to 1.5 V, See Figure 7	C_L = 15 pF,			25	ns
$t_{sk(p)}$	Pulse skew§					0	2	ns
$t_{sk(lim)}$	Skew limit¶	'ALS176	R_L = 54 Ω, See Figure 3	C_L = 50 pF,			10	ns
		'ALS176A					7.5	
		'ALS176B					5	
t_{PZH}	Output enable time to high level		C_L = 15 pF,	See Figure 8		11	18	ns
t_{PZL}	Output enable time to low level					11	18	ns
t_{PHZ}	Output disable time from high level						50	ns
t_{PLZ}	Output disable time from low level						30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.
¶ Skew limit is the maximum difference in propagation delay times between any two channels of one device.

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{pd}	Propagation time	'ALS176	V_{ID} = –1.5 V to 1.5 V, See Figure 7	C_L = 15 pF,	9	14	19	ns
		'ALS176A			10.5	14	18	
		'ALS176B			11.5	13	16.5	
$t_{sk(p)}$	Pulse skew‡					0	2	ns
t_{PZH}	Output enable time to high level		C_L = 15 pF,	See Figure 8		7	14	ns
t_{PZL}	Output enable time to low level					20	35	ns
t_{PHZ}	Output disable time from high level					20	35	ns
t_{PLZ}	Output disable time from low level					8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.

PARAMETER MEASUREMENT INFORMATION

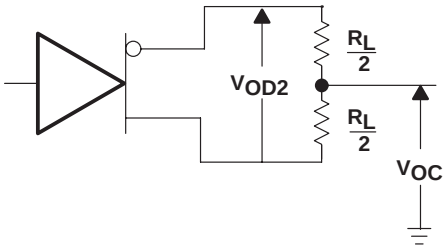


Figure 1. Driver V_{OD2} and V_{OC}

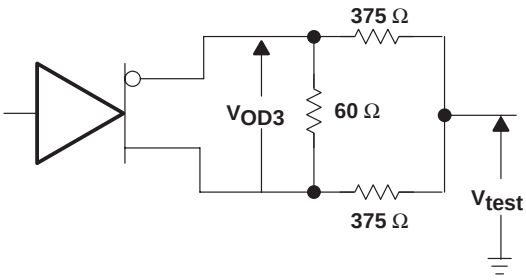
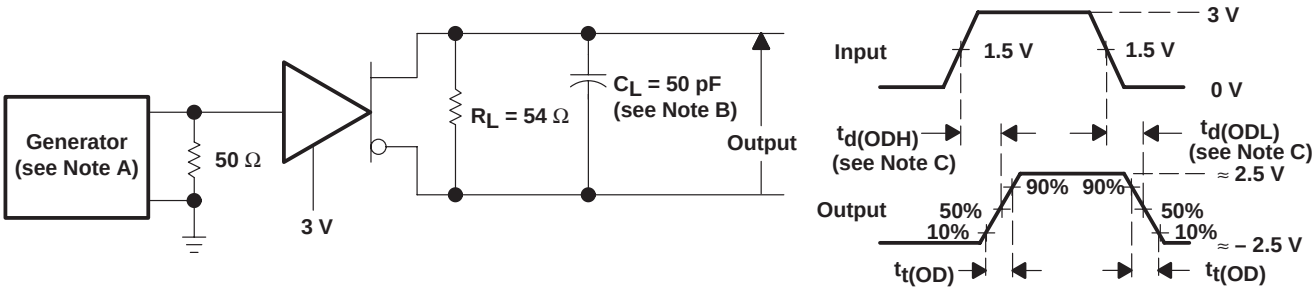


Figure 2. Driver V_{OD3}

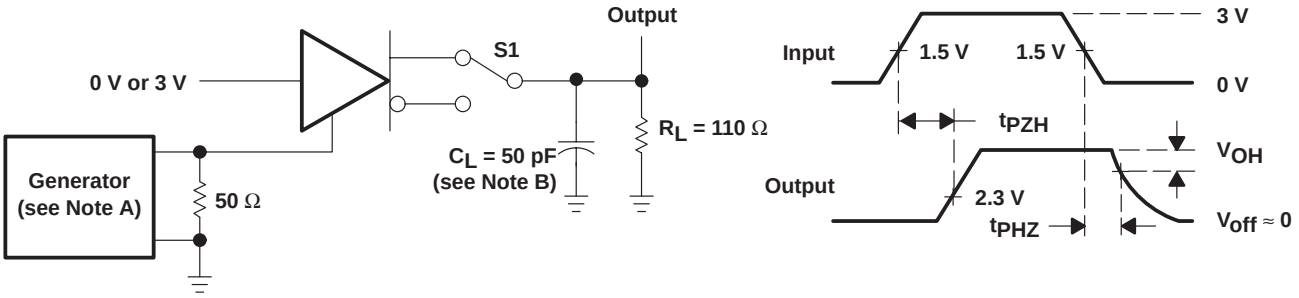
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. $t_{d(OD)} = t_{d(ODH)}$ or $t_{d(ODL)}$

Figure 3. Driver Test Circuit and Voltage Waveforms

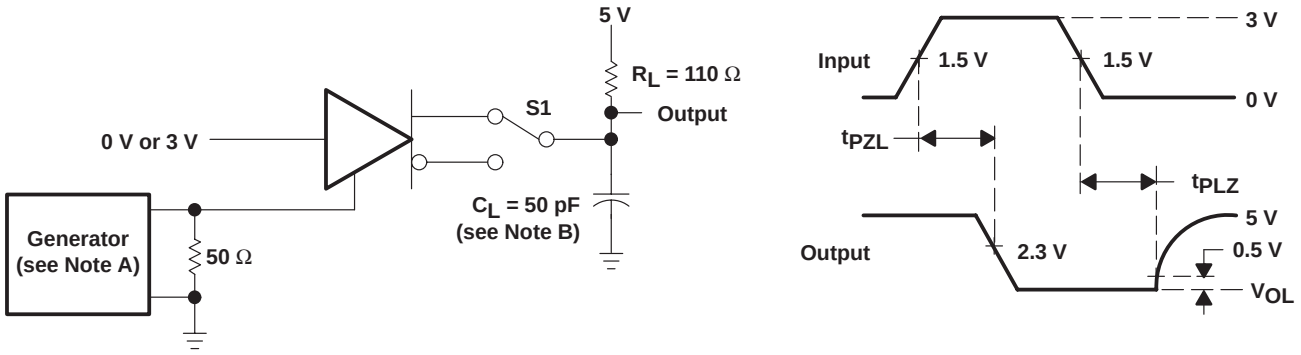


TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waeforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms

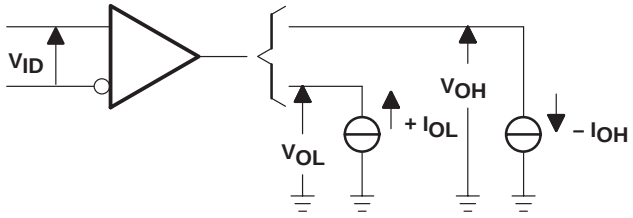
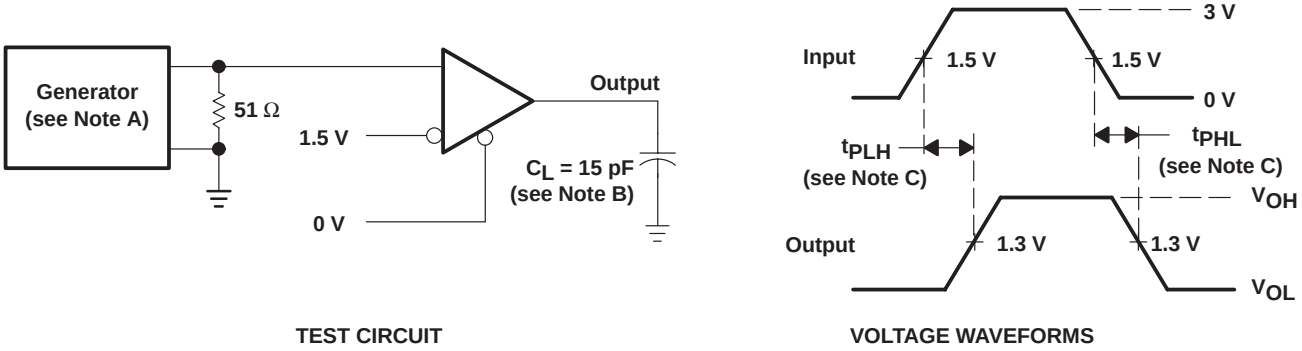


Figure 6. Receiver V_{OH} and V_{OL} Test Circuit

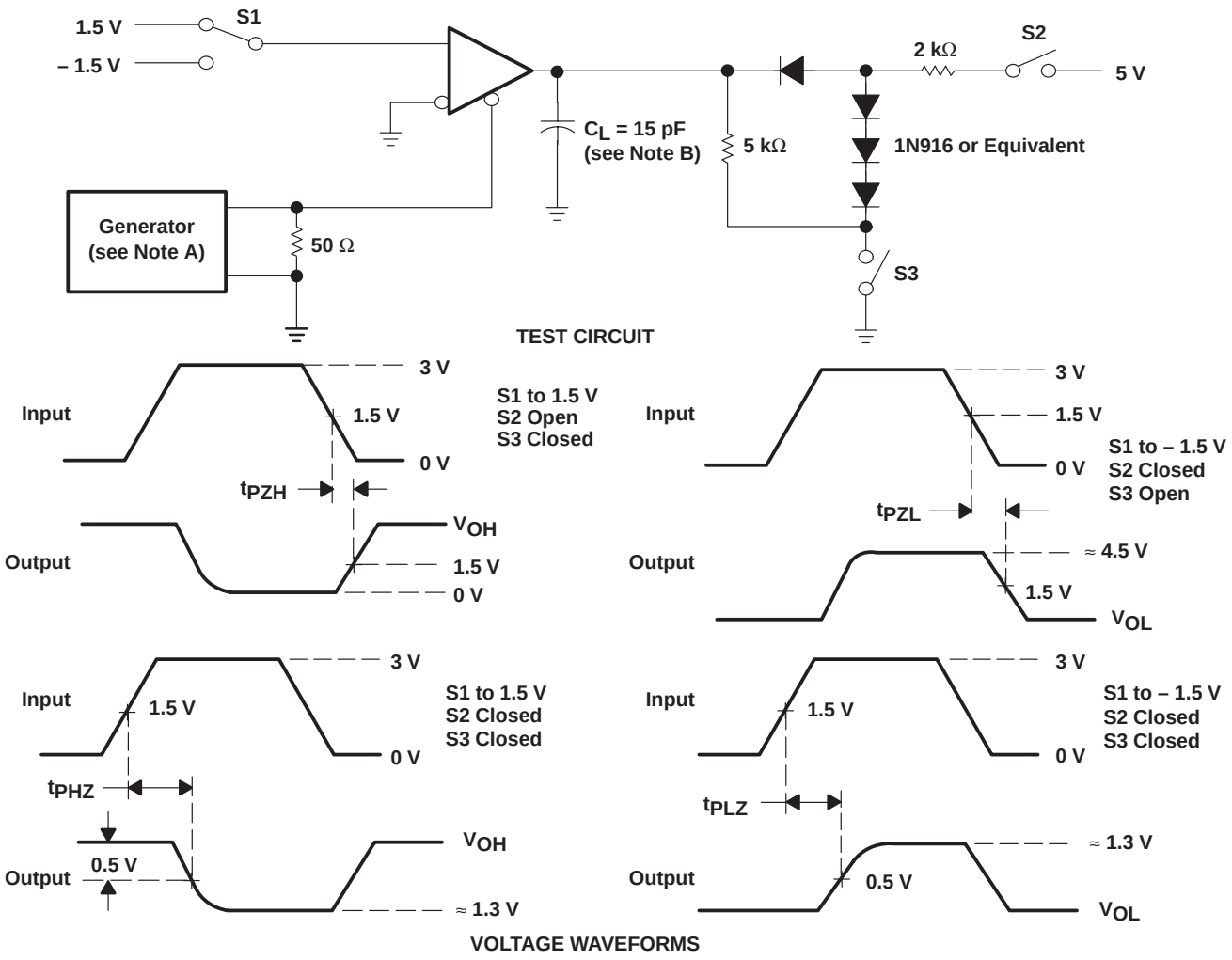


TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. t_{pd} = t_{PLH} or t_{PHL}

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 8. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

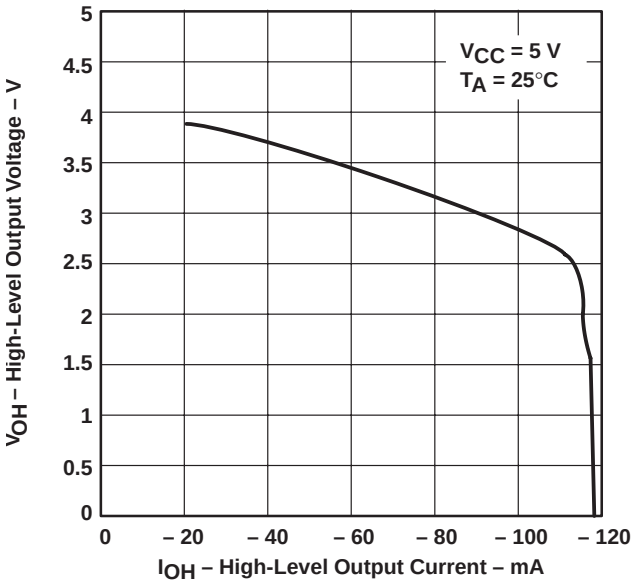


Figure 9

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

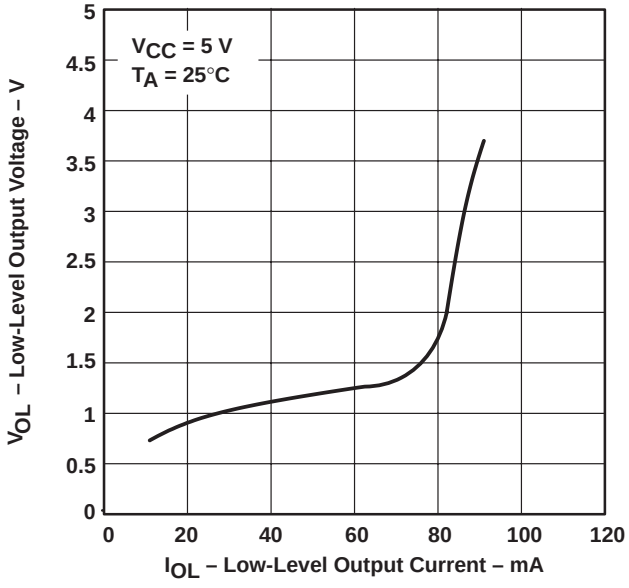


Figure 10

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

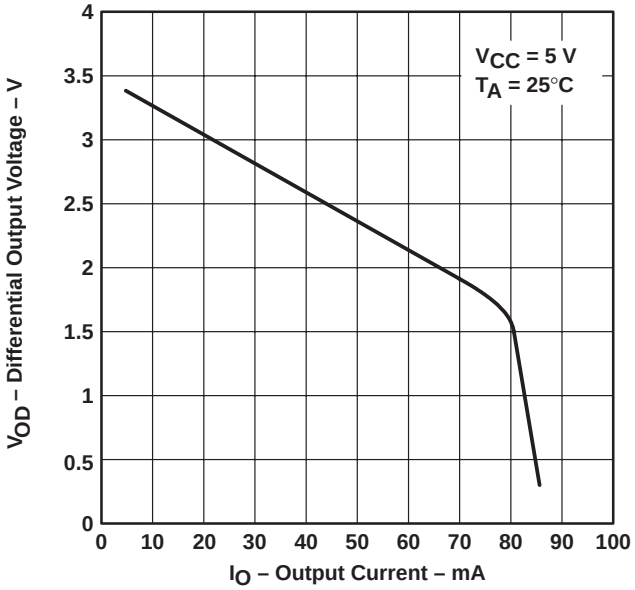


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

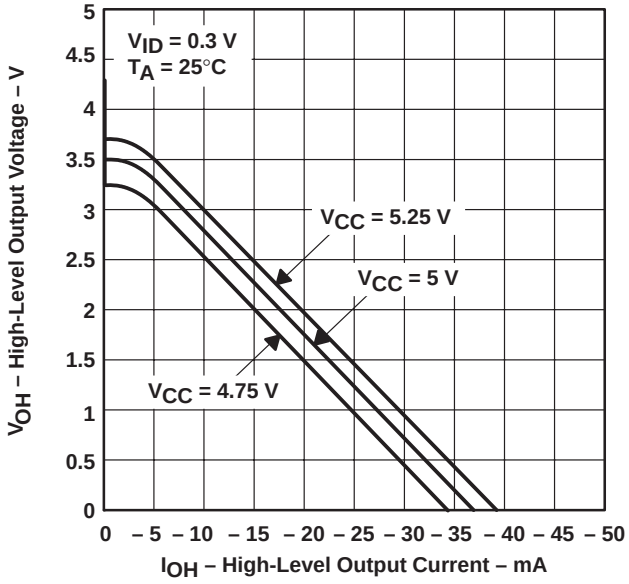


Figure 12

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

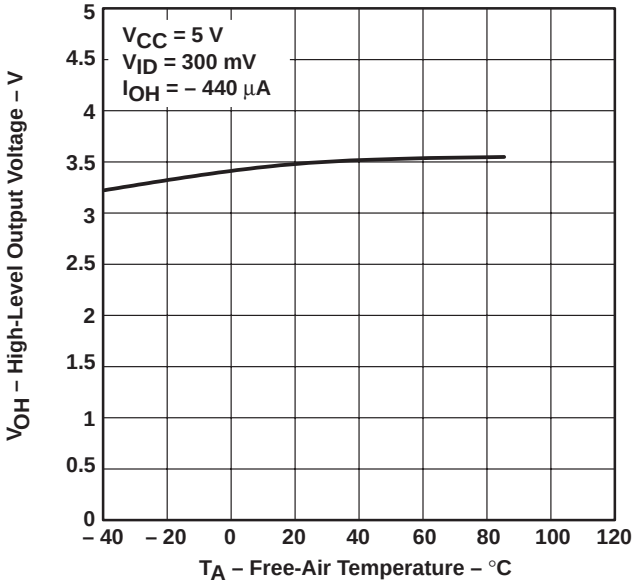


Figure 13

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

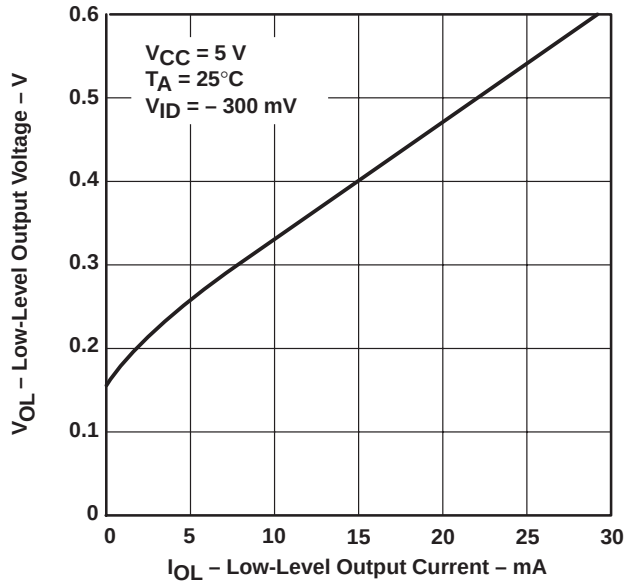


Figure 14

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

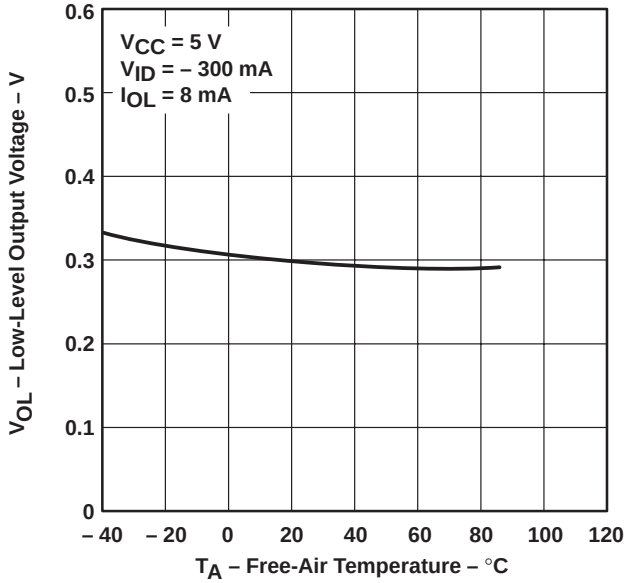


Figure 15

TYPICAL CHARACTERISTICS

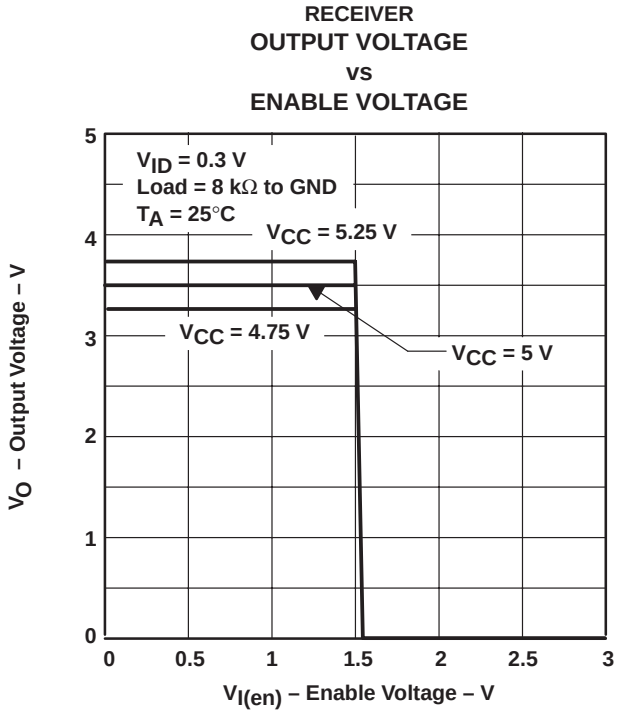


Figure 16

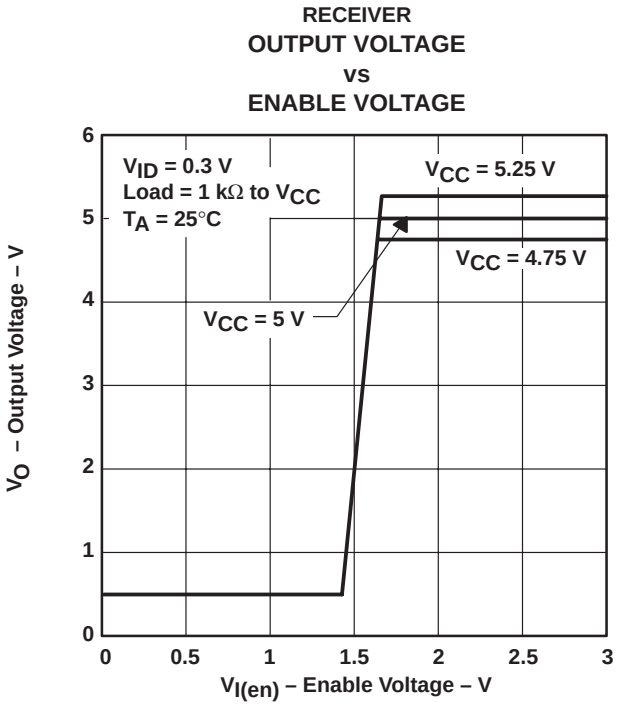
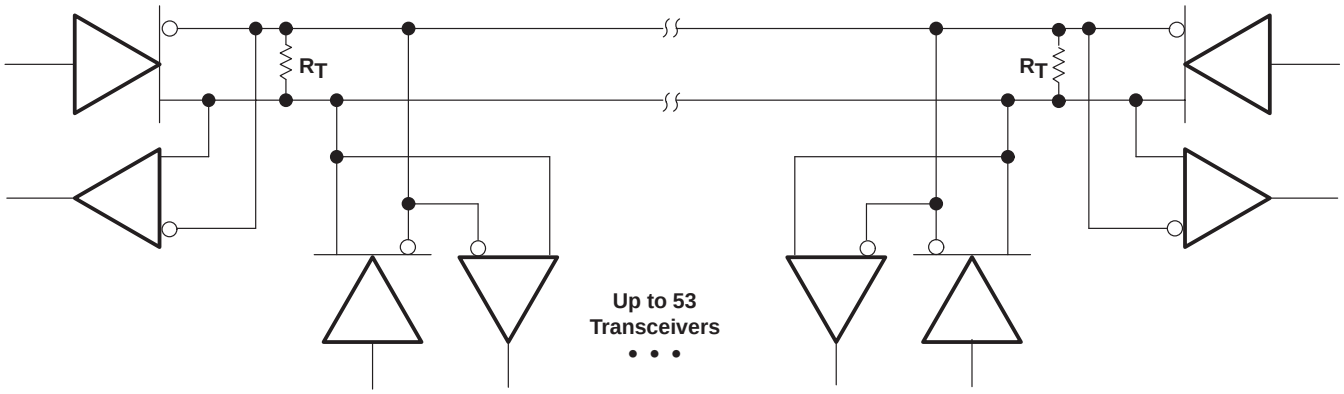


Figure 17

APPLICATION INFORMATION



NOTE A: The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.