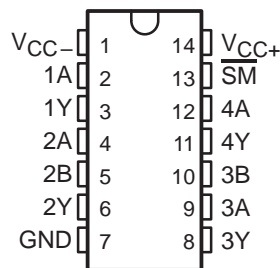


SN75C198 QUADRUPLE LOW-POWER LINE DRIVERS

SLLS051C – JULY 1990 – REVISED MARCH 1997

- Meets ANSI EIA/TIA-232-E and ITU Recommendation V.28
- Very Low Supply Current
- Sleep Mode:
3-State Outputs in High-Impedance State
Ultra-Low Supply Current . . . 17 μ A Typ
- Improved Functional Replacement for:
SN75188,
Motorola MC1488,
National Semiconductor DS14C88, and
DS1488
- CMOS- and TTL-Compatible Data Inputs
- On-Chip Slew-Rate Limit . . . 30 V/ μ s
- Output Current Limit . . . 10 mA Typ
- Wide Supply Voltage Range . . . ± 4.5 V
to ± 15 V

D OR N PACKAGE
(TOP VIEW)



NOT RECOMMENDED FOR NEW DESIGNS

description

The SN75C198 is a monolithic low-power BI-MOS device containing four low-power line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE) in conformance with the specifications of ANSI EIA/TIA-232-E. The drivers of the SN75C198 are similar to those of the SN75C188 quadruple driver. The drivers have a controlled-output slew rate that is limited to a maximum of 30 V/ μ s. This feature eliminates the need for external components.

The sleep-mode input, \overline{SM} , can switch the outputs to high impedance, which avoids the transmission of corrupted data during power-up and allows significant system power savings during data-off periods.

The SN75C198 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

| INPUTS | | | OUTPUT Y |
|-----------------|---|---|-------------|
| \overline{SM} | A | B | |
| H | H | H | L |
| H | L | X | H |
| H | X | L | H |
| L | X | X | Z |

H = high level, L = low level,
X = irrelevant, Z = high impedance



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

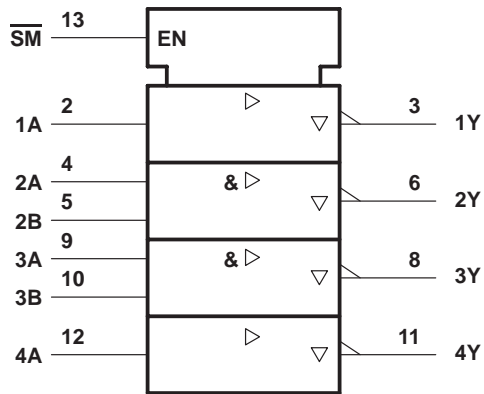
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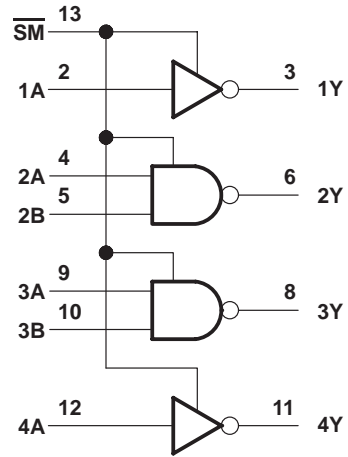
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logic symbol†

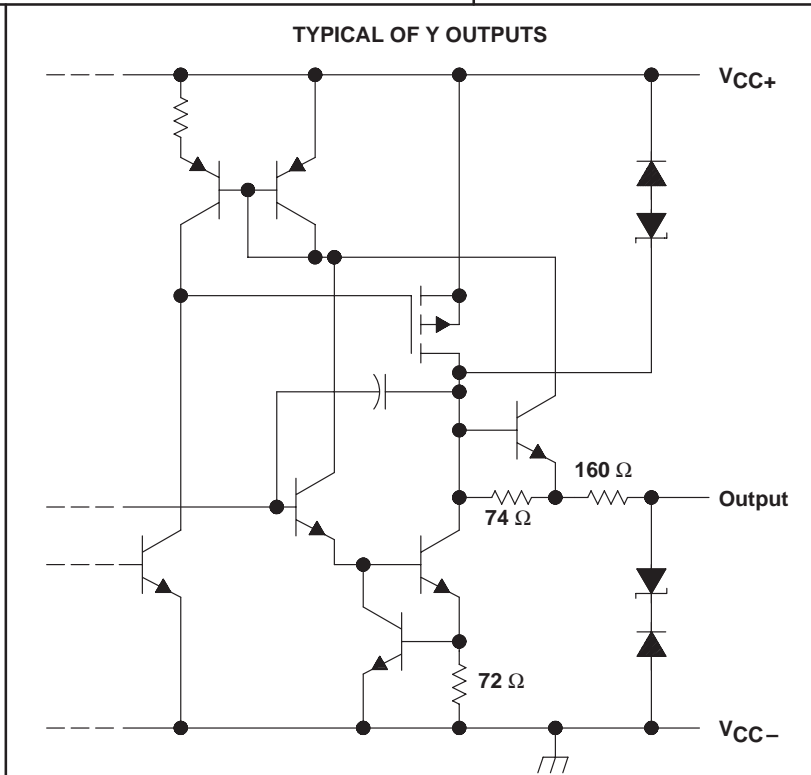
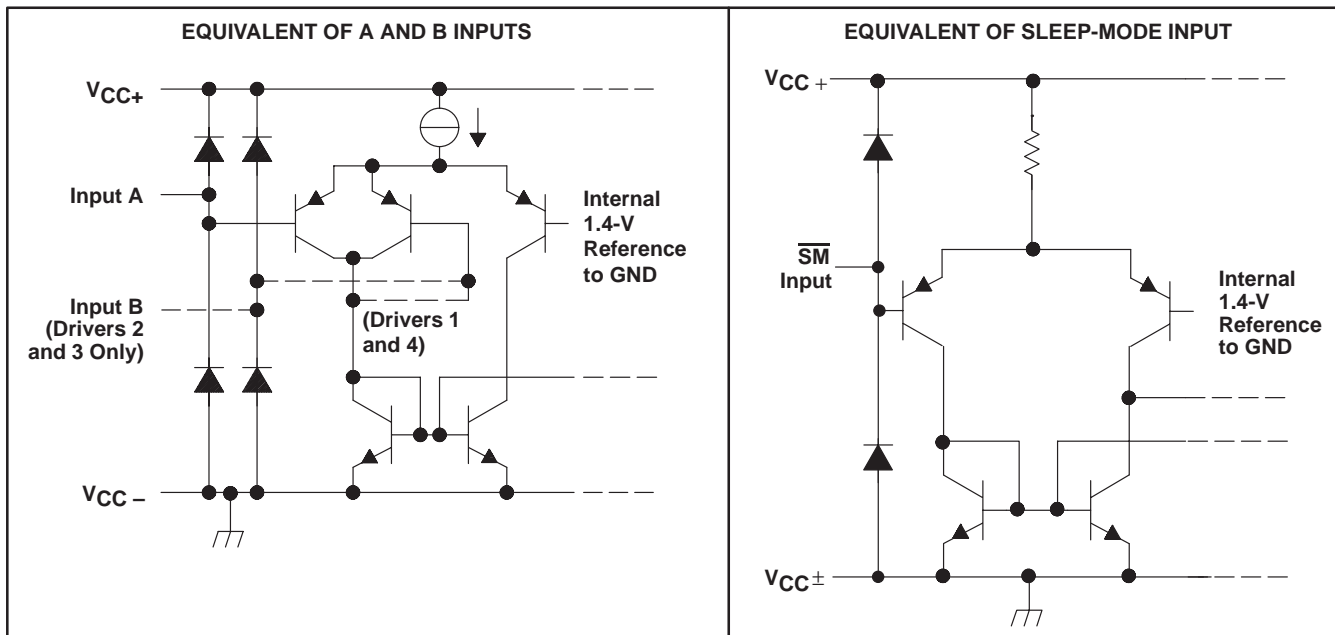


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



All resistor values shown are nominal.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--------------------------------------------------------------|------------------------------------|
| Supply voltage, V_{CC+} (see Note 1) | 15 V |
| Supply voltage, V_{CC-} | -15 V |
| Input voltage range, V_I | -15 V to 15 V |
| Output voltage range, V_O | $V_{CC-} - 6 V$ to $V_{CC+} + 6 V$ |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A : SN75C198 | 0°C to 70°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING |
|---------|---------------------------------------------|---------------------------------------------------|------------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| N | 1150 mW | 9.2 mW/°C | 730 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---------------------------------------|----------------|-----|-----------|------|
| Supply voltage, V_{CC+} | 4.5 | 12 | 15 | V |
| Supply voltage, V_{CC-} | -4.5 | -12 | -15 | V |
| Input voltage, V_I (see Figure 2) | $V_{CC-} + 2$ | | V_{CC+} | V |
| High-level input voltage, V_{IH} | 2 | | | V |
| Low-level input voltage, V_{IL} | A and B inputs | | 0.8 | V |
| | SM input | | 0.6 | |
| Operating free-air temperature, T_A | 0 | | 70 | °C |



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electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm} = \pm 12\text{ V}$, \overline{SM} at 2 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT | |
|--------------------|------------------------------------------|---------------------------------------------------------------------------------|--------------------------------------------------|------|------|-------|------|--|
| V _{OH} | High-level output voltage | V _{IH} = 0.8 V, R _L = 3 kΩ | V _{CC±} = ±5 V | 4 | | | V | |
| | | | V _{CC±} = ±12 V | 10 | | | | |
| V _{OL} | Low-level output voltage (see Note 2) | V _{IH} = 2 V, R _L = 3 kΩ | V _{CC±} = ±5 V | | | -4 | V | |
| | | | V _{CC±} = ±12 V | | | -10 | | |
| I _{IH} | High-level input current | V _I = 5 V | | | | 10 | μA | |
| I _{IL} | Low-level input current | V _I = 0 V | | | | -10 | μA | |
| I _{OZ} | High-impedance-state output current | \overline{SM} at 0.6 V | V _O = 12 V, V _{CC±} = ±12 V | | | 100 | μA | |
| | | | V _O = -12 V, V _{CC±} = ±12 V | | | -100 | | |
| I _{OS(H)} | High-level short-circuit output current‡ | V _I = 0.8 V, V _O = 0 or V _{CC-} | | -4.5 | -10 | -19.5 | mA | |
| I _{OS(L)} | Low-level short-circuit output current‡ | V _I = 2 V, V _O = 0 or V _{CC+} | | 4.5 | 10 | 19.5 | mA | |
| r _o | Output resistance | V _{CC±} = 0, V _O = -2 V to 2 V | | 300 | | | Ω | |
| I _{CC+} | Supply current from V _{CC+} | A and B inputs at 0.8 V or 2 V, No load | V _{CC±} = ±5 V | | 90 | 160 | μA | |
| | | | V _{CC±} = ±12 V | | 95 | 160 | | |
| | | A and B inputs at 0.8 V or 2 V, R _L = 3 kΩ, \overline{SM} at 0.6 V | V _{CC±} = ±5 V | | 40 | | | |
| | | | V _{CC±} = ±12 V | | 40 | | | |
| I _{CC-} | Supply current from V _{CC-} | A and B inputs at 0.8 V or 2 V, No load | V _{CC±} = ±5 V | | -90 | -160 | μA | |
| | | | V _{CC±} = ±12 V | | -95 | -160 | | |
| | | A and B inputs at 0.8 V or 2 V, R _L = 3 kΩ, \overline{SM} at 0.6 V | V _{CC±} = ±5 V | | -40 | | | |
| | | | V _{CC±} = ±12 V | | -40 | | | |

† All typical values are at T_A = 25°C.

‡ Not more than one output should be shorted at a time.

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10 V is a maximum, the typical value is a more negative voltage.

switching characteristics over recommended operating free-air temperature range, $V_{CC\pm} = \pm 12\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|------------------|----------------------------------------------------|-----------------------------------------------------------------------|---|------|------|-----|------|
| t _{PLH} | Propagation delay time, low- to high-level output§ | R _L = 3 kΩ to 7 kΩ, C _L = 15 pF, See Figure 1 | | | | 3 | μs |
| t _{PHL} | Propagation delay time, high- to low-level output§ | | | | | 3.5 | μs |
| t _{TLH} | Transition time, low- to high-level output¶ | | | 0.53 | 1 | 3.2 | μs |
| t _{THL} | Transition time, high- to low-level output¶ | | | 0.53 | 1 | 3.2 | μs |
| t _{TLH} | Transition time, low- to high-level output# | R _L = 3 kΩ to 7 kΩ, C _L = 2500 pF, See Figure 2 | | | | 1.5 | μs |
| t _{THL} | Transition time, high- to low-level output# | | | | | 1.5 | μs |
| t _{PZH} | Output enable time to high level | R _L = 3 kΩ to 7 kΩ, C _L = 15 pF, See Figure 3 | | | | 50 | μs |
| t _{PHZ} | Output disable time from high level | | | | | 10 | μs |
| t _{PZL} | Output enable time to low level | R _L = 3 kΩ to 7 kΩ, C _L = 15 pF, See Figure 4 | | | | 15 | μs |
| t _{PLZ} | Output disable time from low level | | | | | 10 | μs |
| SR | Output slew rate# | R _L = 3 kΩ to 7 kΩ, C _L = 15 pF | 6 | 15 | 30 | | V/μs |

† All typical values are at T_A = 25°C.

§ t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.

¶ Measured between 10% and 90% points of output waveform

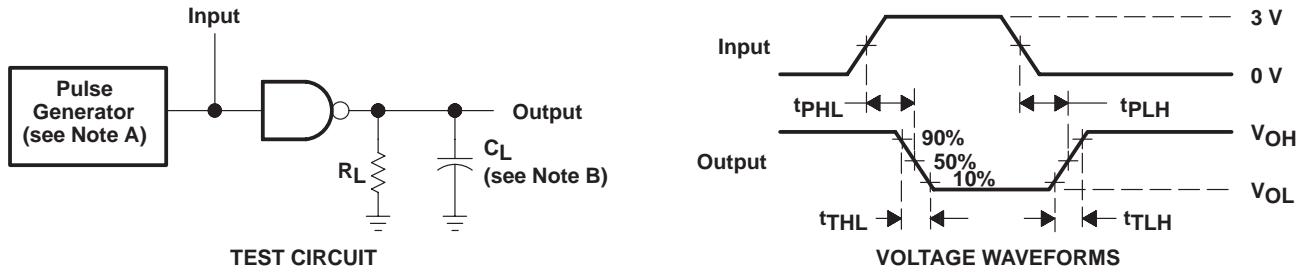
Measured between 3-V and -3-V points of output waveform



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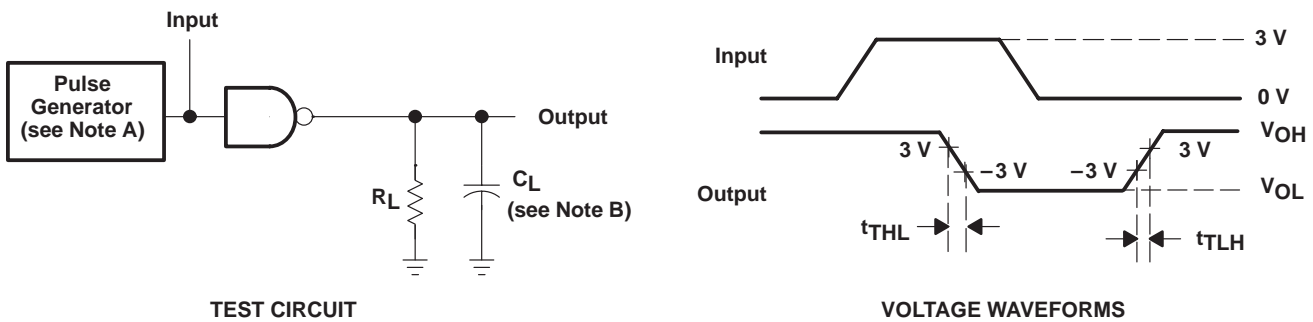
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PARAMETER MEASUREMENT INFORMATION



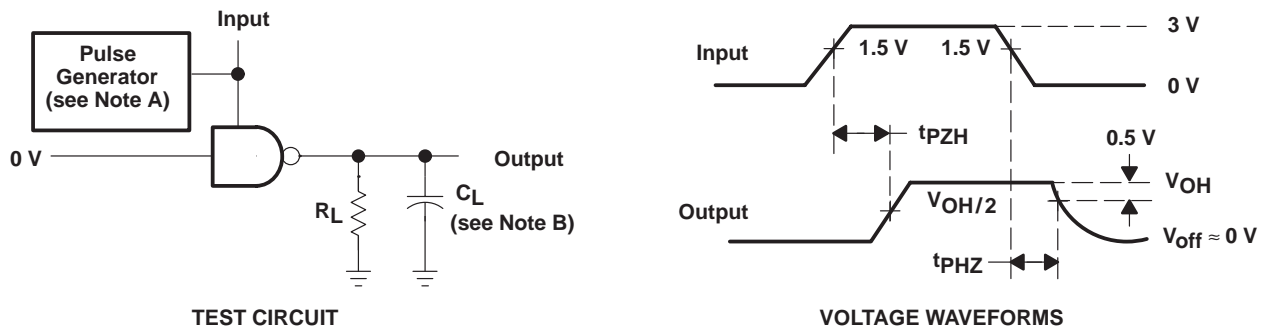
NOTES: A. The pulse generator has the following characteristics: $t_w = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f \leq 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Propagation and Transition Times



NOTES: A. The pulse generator has the following characteristics: $t_w = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f \leq 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

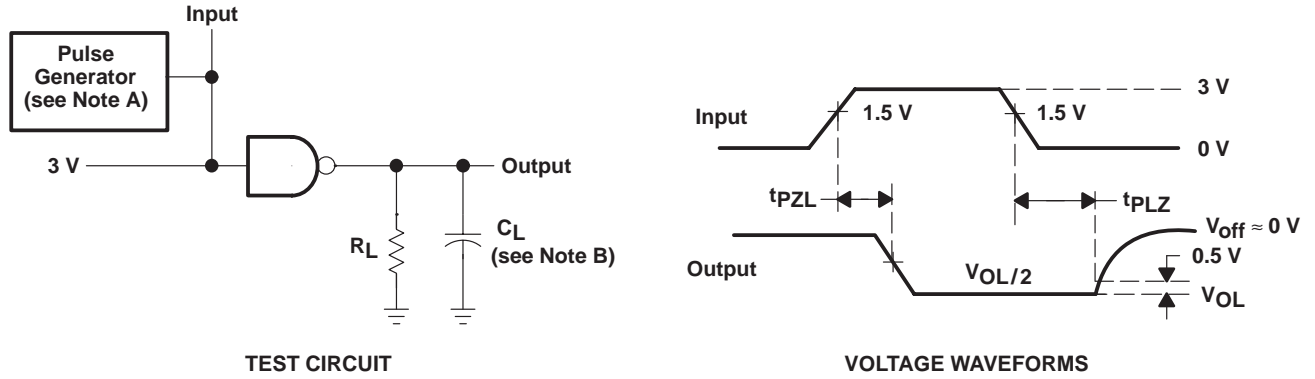
Figure 2. Test Circuit and Voltage Waveforms, Transition Times



NOTES: A. The pulse generator has the following characteristics: $t_w = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f \leq 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: $t_W = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f \leq 50 \text{ ns}$.
 B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

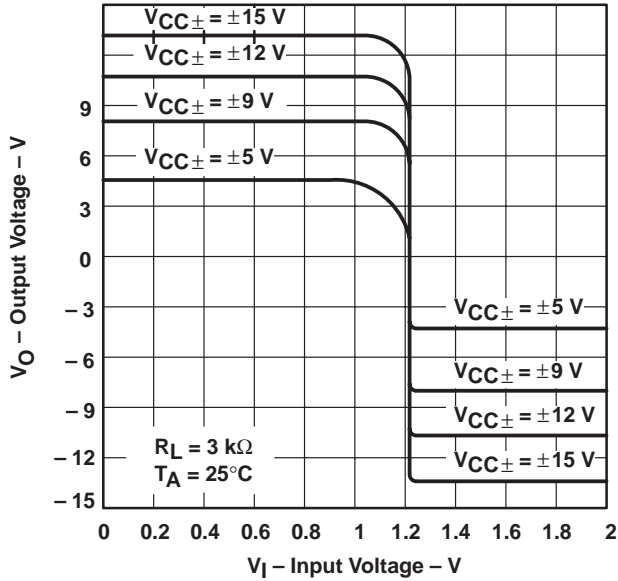


Figure 5

OUTPUT CURRENT vs OUTPUT VOLTAGE

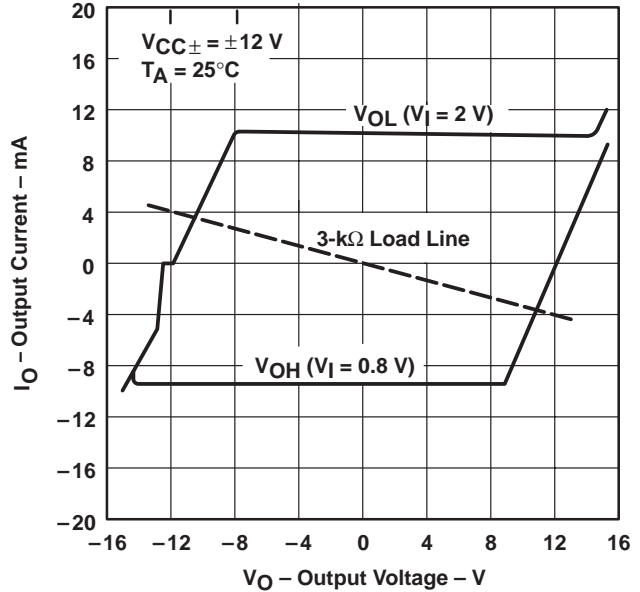


Figure 6

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

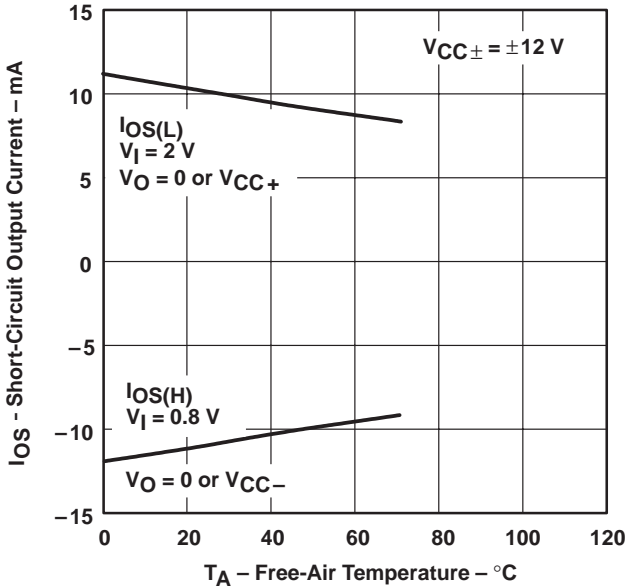


Figure 7

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

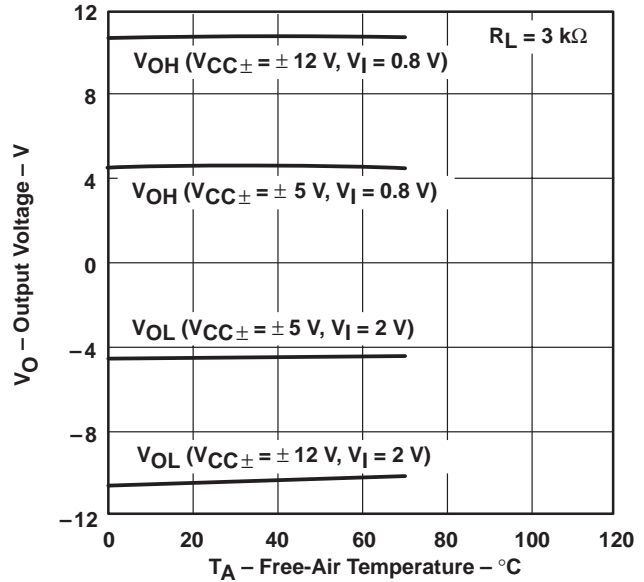
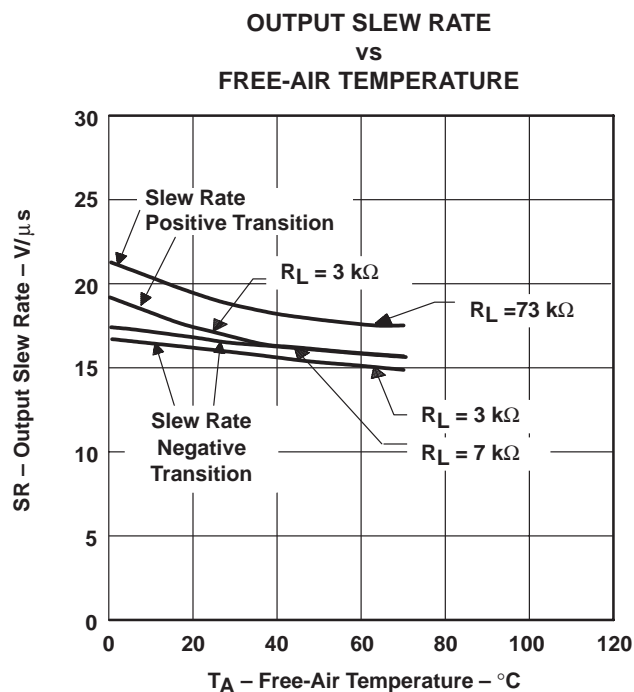
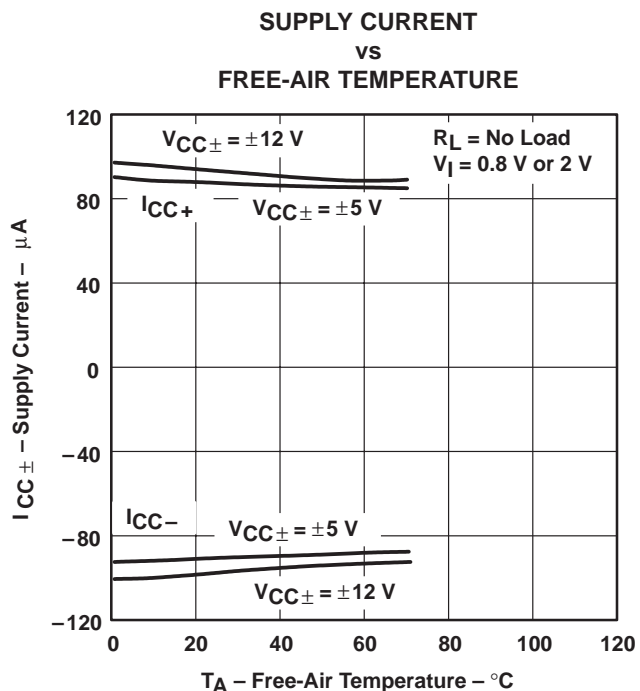
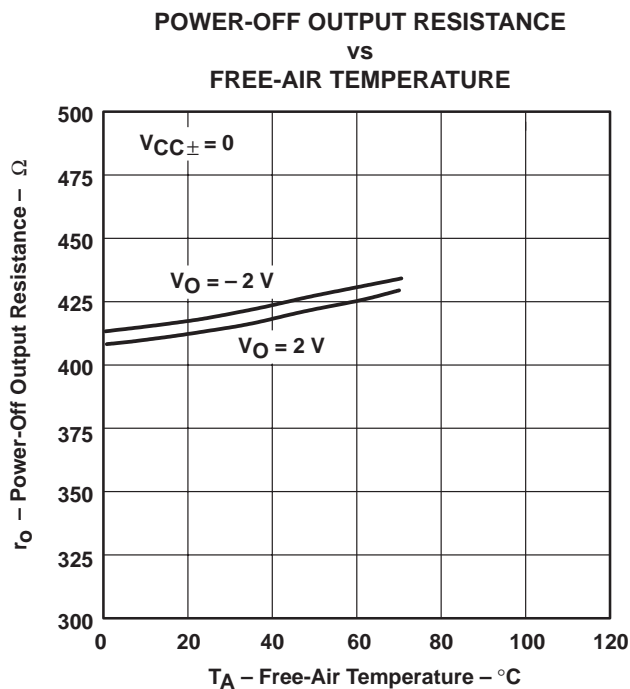
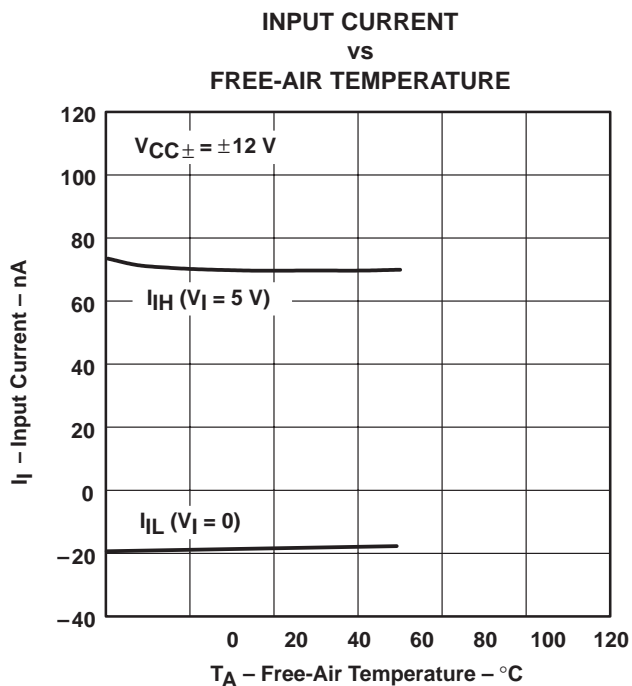


Figure 8

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

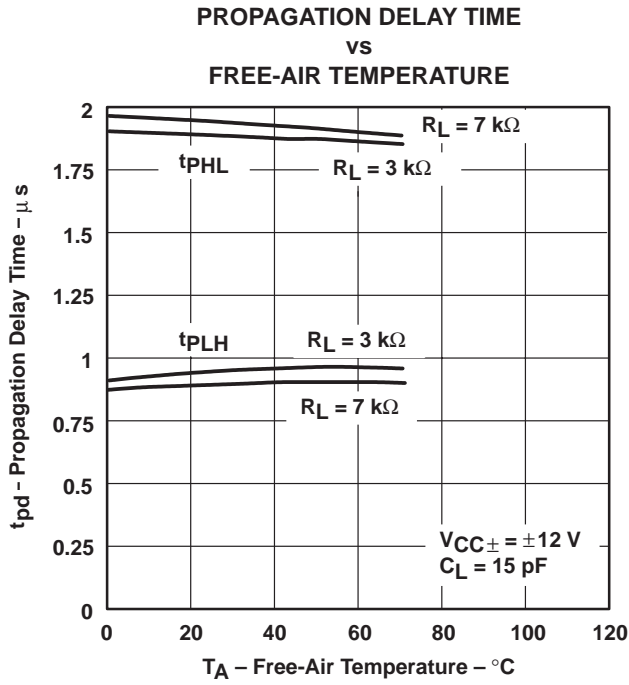


Figure 13

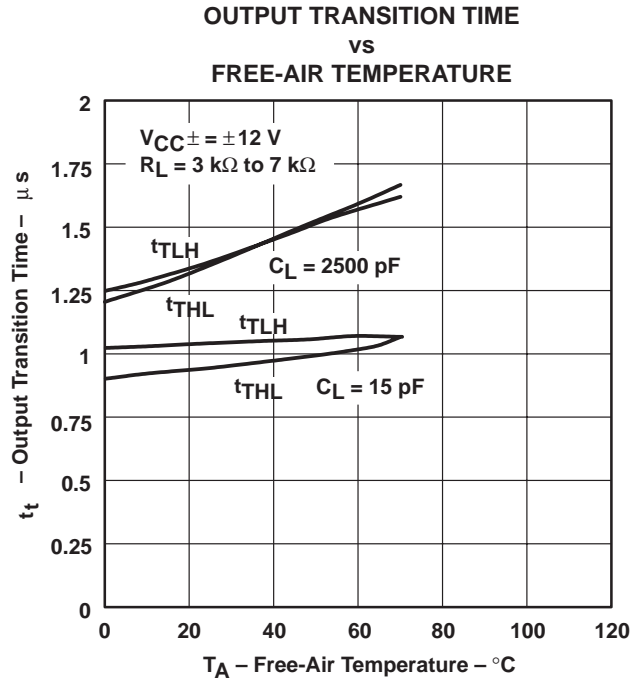


Figure 14

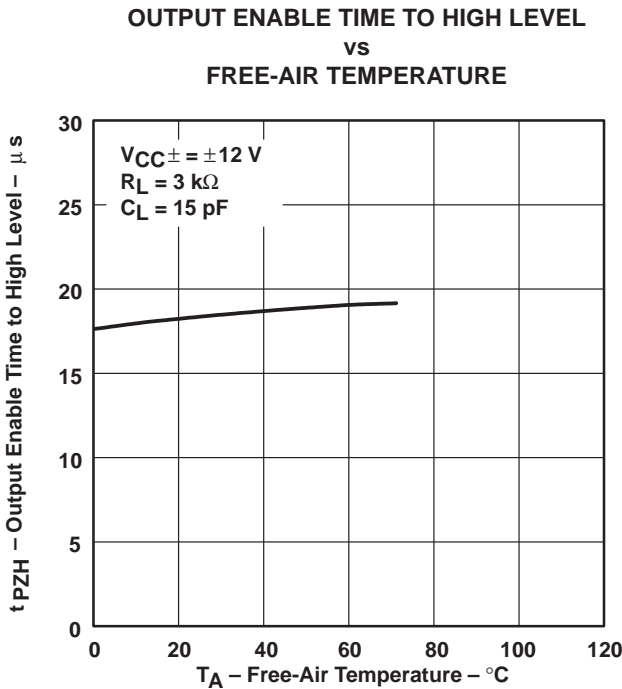


Figure 15

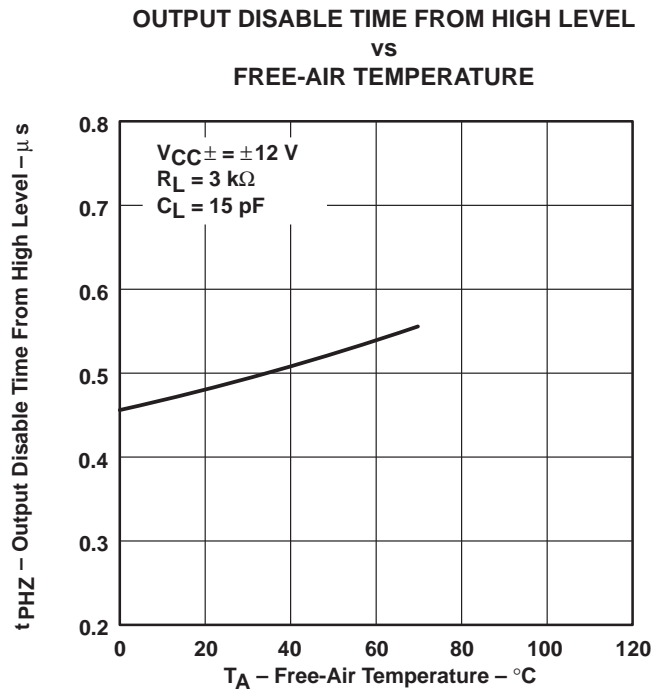


Figure 16

TYPICAL CHARACTERISTICS

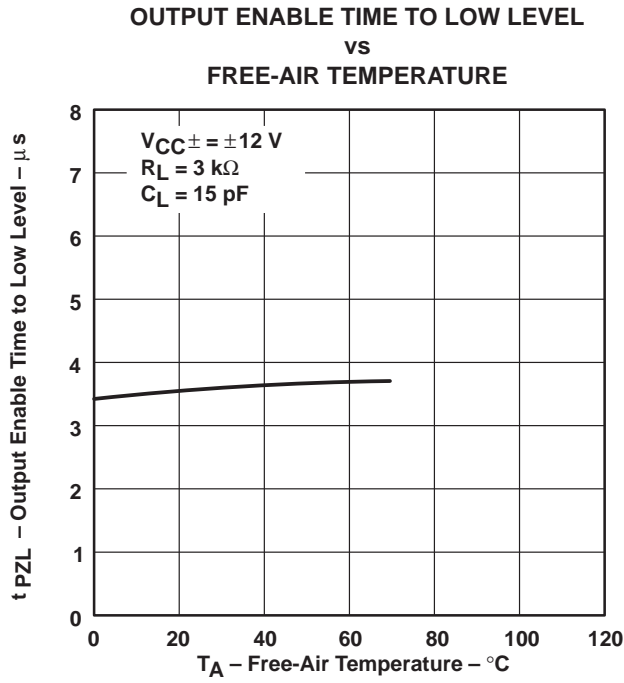


Figure 17

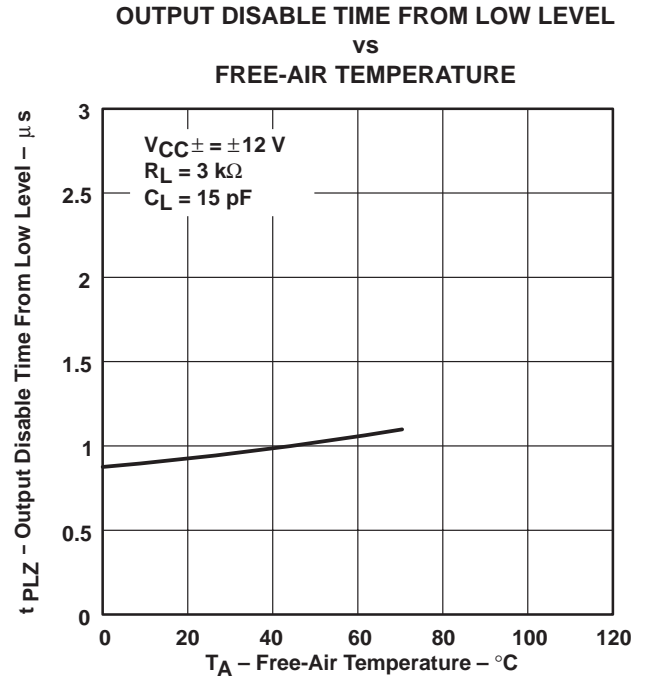


Figure 18

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