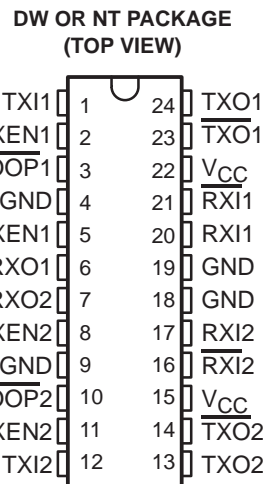


- **Meets or Exceeds the Requirements of IOS 8802.3:1989 and ANSI/IEEE Std 802.3-1988**
- **Interdevice Loop-Back Paths for System Testing**
- **Squelch Function Implemented on the Receiver Inputs**
- **Drivers Will Drive a Balanced 78-Ω Load**
- **Transformer Coupling Not Required in System**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **Isolated Ground Pins for Reduced Noise Coupling**
- **Fault-Condition Protection Built into the Device**
- **Driver Inputs Are Level-Shifted ECL Compatible**



description

The SN75ALS085 is a monolithic, high-speed, advanced low-power Schottky, dual-channel driver/receiver device designed for use in the AUI of ANSI/IEEE Std 802.3-1988. The two drivers on the device drive a 78-Ω balanced, terminated twisted-pair transmission line up to a maximum length of 50 meters. In the off (idle) state, the drivers maintain minimal differential output voltage on the twisted-pair line and, at the same time, remain within the required output common-mode range.

With the driver enable (TXEN) high, upon receiving the first falling edge into the driver input, the differential outputs will rise to full-amplitude output levels within 25 ns. The output amplitude is maintained for the remainder of the packet. After the last positive packet edge is transmitted into the driver, the driver will maintain a minimum of 70% full differential output for a minimum of 200 ns, then decay to a minimum level for the reset (idle) condition within 8 μs. Disabling the driver by taking the driver enable low will also force the output into the idle condition after the normal 8-μs timeout. While operating, the drivers are able to withstand a set of fault conditions and not suffer damage due to the faults being applied. The drivers power up in the idle state to ensure that no activity is placed on the twisted-pair cable that could be interpreted as network traffic.

The line receiver squelch function interfaces to a differential twisted-pair line terminated external to the device. The receiver squelch circuit allows differential receive signals to pass through as long as the input amplitude and pulse duration are greater than the minimum squelch threshold. This ensures a good signal-to-noise ratio while the data path is active and prevents system noise from causing false data transitions during line shutdown and line-idle conditions. The RXO outputs default to a high level and the RXEN outputs default to a low level while the squelch function is blocking the data path through the receiver (idle). The line receiver squelch will become active within 50 ns when the input squelch threshold is exceeded. RXEN will be driven high when the squelch circuit is allowing data to pass through the receiver. The receiver squelch circuit can also withstand a set of fault conditions while operating without causing permanent damage to the device.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated

SN75ALS085

LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

SLLS054B – APRIL 1989 – REVISED MAY 1995

description (continued)

The purpose of the loop functions is to provide a means by which system data path verification can be done to isolate faulty interfaces and assist in network diagnosis. The LOOP pins are TTL compatible and must be held high for normal operation. When $\overline{\text{LOOP1}}$ is taken low, the output of driver 1 (TXO1) immediately goes into the idle state. Also, the input to receiver 1 is ignored and a path from TXI1 to RXO1 is established. When $\overline{\text{LOOP1}}$ is taken back high, driver 1 and receiver 1 revert back to their normal operation. When $\overline{\text{LOOP2}}$ is taken low, a similar data path is established between TXI1 and RXO2. TXEN1 must be high for the loop functions to operate and TXEN1 can be used to gate the loop function if desired. During loop operation, the respective receiver enable output (RXEN) will reflect the status of TXEN1.

Function Tables

RECEIVER – $\overline{\text{LOOP}} = \text{H}$

RXI		PREVIOUS RXEN	OUTPUTS	
			RXEN	RXO
$V_{ID} = 1315 \text{ mV to } -175 \text{ mV},$	$t_w < 25 \text{ ns}$	L	L	H
$V_{ID} = -275 \text{ mV to } -1315 \text{ mV},$	$t_w > 50 \text{ ns}$	X	H	L
$V_{ID} = 318 \text{ mV to } 1315 \text{ mV},$	$t_w < 142 \text{ ns}$	H	H	H
$V_{ID} = 318 \text{ mV to } 1315 \text{ mV},$	$t_w > 187 \text{ ns}$	X	L	H

H = high level, L = low level, X = don't care

DRIVER – $\overline{\text{LOOP}} = \text{H}$

TXI	TXEN	PREVIOUS TXO	OUTPUT TXO
L	L	Idle	Idle
H	L	Idle	Idle
↓	H	Idle	L
L	H	Active	L
$H < 260 \mu\text{s}$	H	Active	H
$H > 8 \mu\text{s}$	H	Active	Idle
L	$L > 8 \mu\text{s}$	Active	Idle
$H < 260 \text{ ns}$	$L > 8 \mu\text{s}$	Active	Idle
$H < 260 \text{ ns}$	$L < 260 \text{ ns}$	Active	H
$H > 8 \mu\text{s}$	$L < 260 \text{ ns}$	Active	Idle
L	$L < 260 \text{ ns}$	Active	L

$H = V_I \geq V_T \text{ max}, L = V_I \leq V_T \text{ min}$



SN75ALS085
LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

SLLS054B – APRIL 1989 – REVISED MAY 1995

Function Tables (continued)

LOOP										
INPUTS						OUTPUTS				
LOOP1	LOOP2	TX1	TXEN1	RX1	RX2	RXO1	RXO2	RXEN1	RXEN2	TXO1
L	L	L	H	X	X	L	L	H	H	Idle
L	L	H	H	X	X	H	H	H	H	Idle
L	L	X	L	X	X	H	H	L	L	Idle
L	H	L	H	X	Normal	L	Normal	H	Normal	Idle
L	H	H	H	X	Normal	H	Normal	H	Normal	Idle
L	H	X	L	X	Normal	H	Normal	L	Normal	Idle
H	L	L	H	Normal	X	Normal	L	Normal	H	Idle
H	L	H	H	Normal	X	Normal	H	Normal	H	Idle
H	L	X	L	Normal	X	Normal	H	Normal	L	Idle
H	H	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

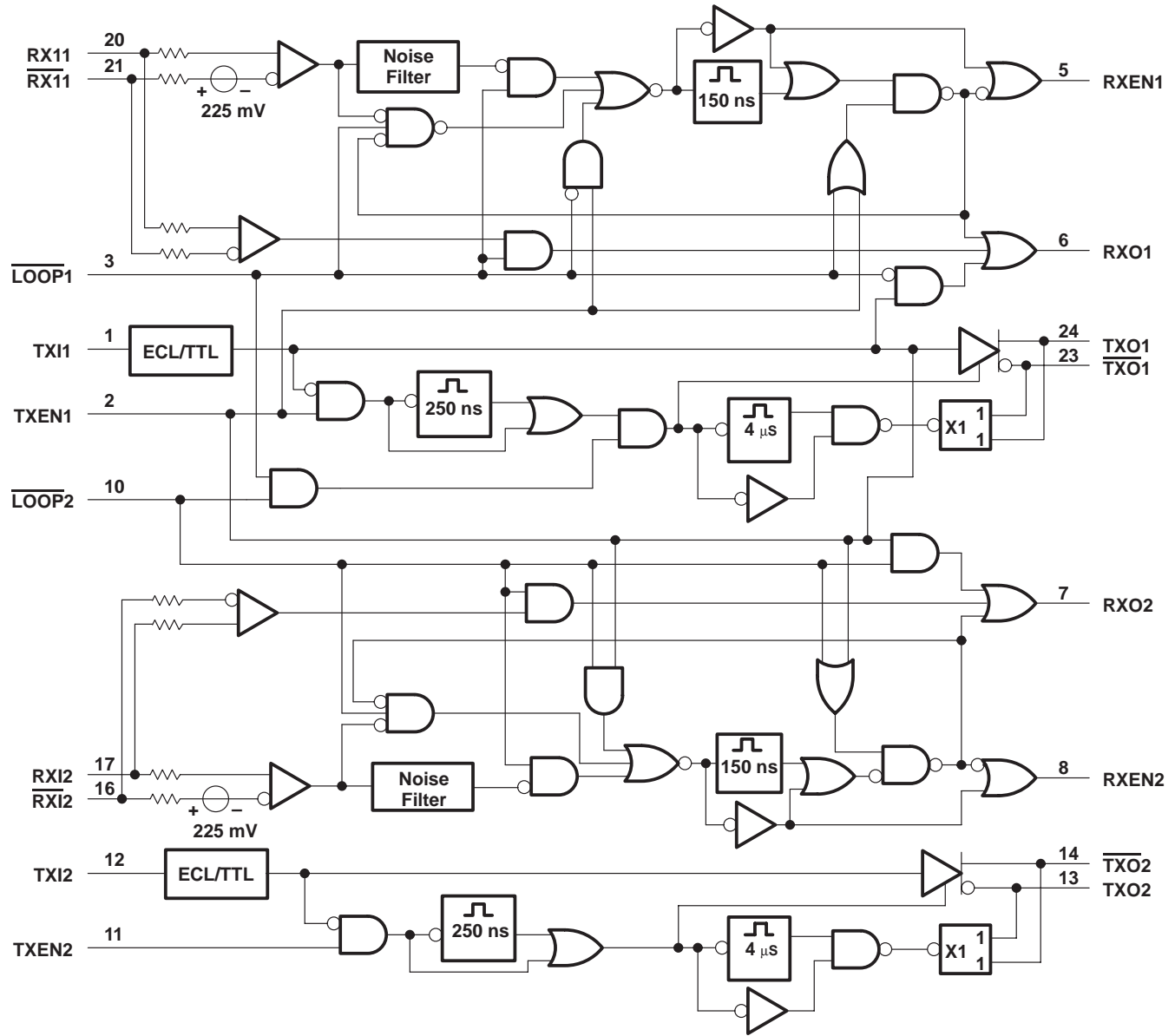
H = high level, L = low level, X = don't care



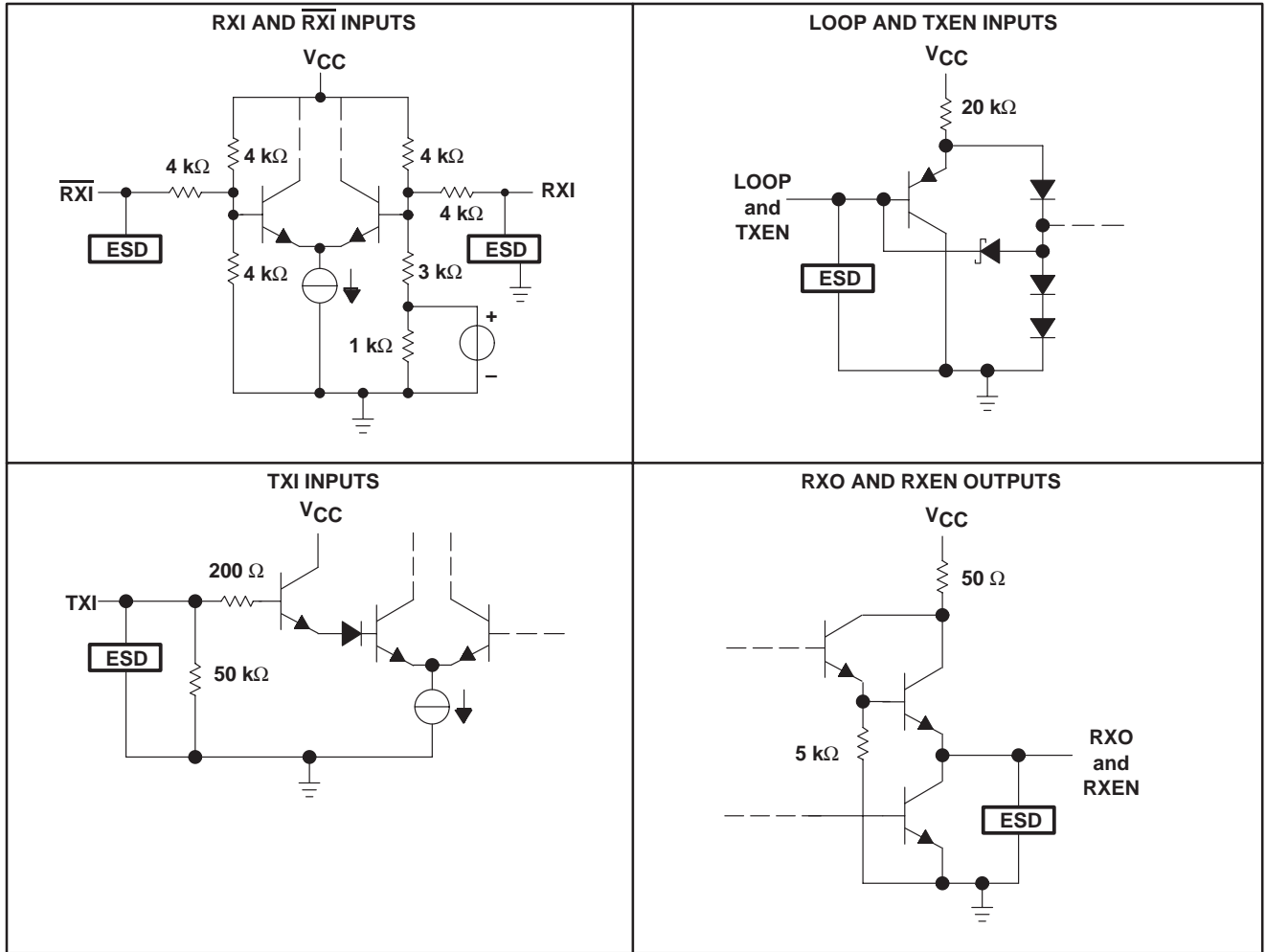
SN75ALS085 LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

SLLS054B – APRIL 1989 – REVISED MAY 1995

logic diagram (positive logic)



schematics of inputs and outputs



SN75ALS085

LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

SLLS054B – APRIL 1989 – REVISED MAY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	6 V
TXI and \overline{LOOP} input voltage, V_I	5.5 V
TXO and \overline{TXO} output voltage, V_O	16 V
RXI and \overline{RXI} input voltage, V_I	16 V
RXO and RXEN output voltage, V_O	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW
NT	1250 mW	10.0 mW/°C	800 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode voltage at RXI inputs, V_{IC}	1		4.2	V
Differential voltage between RXI inputs, V_{ID}	± 318		± 1315	mV
High-level input voltage, \overline{LOOP} and TXEN, V_{IH}	2			V
Low-level input voltage, \overline{LOOP} and TXEN, V_{IL}			0.8	V
High-level output current, RXO and RXEN, I_{OH}			-0.4	mA
Low-level output voltage, RXO and RXEN, I_{OL}			16	mA
Setup time, driver mode, TXEN high before TXI \downarrow , t_{su1} (see Figure 7)	10			ns
Setup time, loop mode, \overline{LOOP} low before TXEN \uparrow , t_{su2} (see Figure 9)	15			ns
Setup time, loop mode, TXEN high before TXI \downarrow , t_{su3} (see Figure 9)	10			ns
Hold time, loop mode, TXEN high after TXI \uparrow , t_{h1} (see Figure 8)	10			ns
Hold time, loop mode, \overline{LOOP} low after TXEN \downarrow , t_{h2} (see Figure 8)	15			ns
Operating free-air temperature, T_A	0		70	°C



SN75ALS085

LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

SLLS054B – APRIL 1989 – REVISED MAY 1995

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT	
V_{IK}	Clamp voltage at all inputs	$I_I = -18 \text{ mA}$			-1.5	V	
$V_{(TO)}$	Driver input (TXI) threshold voltage	$T_A = 0^\circ\text{C}$	$V_{CC} = 4.75 \text{ V}$	3.202	3.752	V	
			$V_{CC} = 5 \text{ V}$	3.389	3.998		
			$V_{CC} = 5.25 \text{ V}$	3.577	4.244		
		$T_A = 25^\circ\text{C}$	$V_{CC} = 4.75 \text{ V}$	3.213	3.797	V	
			$V_{CC} = 5 \text{ V}$	3.400	4.043		
			$V_{CC} = 5.25 \text{ V}$	3.588	4.289		
		$T_A = 70^\circ\text{C}$	$V_{CC} = 4.75 \text{ V}$	3.239	3.849	V	
			$V_{CC} = 5 \text{ V}$	3.426	4.095		
			$V_{CC} = 5.25 \text{ V}$	3.614	4.341		
Receiver differential input threshold voltage					-275	mV	
V_{OC}	Driver output (TXO) common-mode voltage	Idle	TXEN at 0.8 V, LOOP2 at 2 V, LOOP1 at 2 V, See Figure 1	1	4.2	V	
		Active	TXEN at 2 V, LOOP2 at 2 V, See Figure 1	1	4.2		
		Active	TXEN at 2 V, LOOP2 at 2 V, See Figure 1	1	4.2		
V_{OD}	Driver output (TXO) differential voltage	Idle	TXEN at 0.8 V, LOOP2 at 2 V, LOOP1 at 2 V, See Figure 1		± 40	mV	
		Active	TXEN at 2 V, LOOP2 at 2 V, See Figure 1	-600	1315		
		Active	TXEN at 2 V, LOOP2 at 2 V, See Figure 1	600	1315		
V_{OH}	High-level output voltage	RXO, RXEN	$I_{OH} = -0.4 \text{ mA}$	2.4		V	
V_{OL}	Low-level output voltage	RXO, RXEN	$I_{OL} = 16 \text{ mA}$		0.5	V	
I_{IH}	High-level input current	TXEN, LOOP	$V_I = 2 \text{ V}$		20	μA	
		TXI	$V_I = 4.5 \text{ V}$		400		
		RXI, RXI	$V_{ID} = -0.5 \text{ V},$ $V_{IC} = 1 \text{ V to } 4.2 \text{ V}$		1000		
I_{IL}	Low-level input current	TXEN, LOOP	$V_I = 0.8 \text{ V}$		-200	mA	
		TXI	$V_I = 3.1 \text{ V}$		100		
			$V_I = 0.3 \text{ V}$		4		10
		RXI, RXI	$V_{ID} = 0.5 \text{ V},$ $V_{IC} = 1 \text{ V to } 4.2 \text{ V}$		1000		
I_{OD}	Driver differential output current	Idle	TXEN at 0.8 V, LOOP2 at 2 V, LOOP1 at 2 V, See Figure 2		± 4	mA	
I_{OS}	Short-circuit output current†	RXO, RXEN	V_O at 0 V, RXI at 2 V	RXI at 3 V,	-40	-150	mA
I_{CC}	Supply current		LOOP2 at 2 V, TXI at 4.5 V,	TXEN at 2 V, Outputs open		225	mA

† Not more than one output should be shorted at a time, and the duration of the test should not exceed 1 second.



SN75ALS085 LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

SLLS054B – APRIL 1989 – REVISED MAY 1995

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS†	MIN	MAX	UNIT
Driver fault condition current	TXO shorted to $\overline{\text{TXO}}$, Current measured in short		150	mA
	TXO at 0 V, $\overline{\text{TXO}}$ is open, Current measured at TXO		150	
	TXO is open, $\overline{\text{TXO}}$ at 0, Current measured at $\overline{\text{TXO}}$		150	
	TXO at 0 V, $\overline{\text{TXO}}$ at 0 V, Current measured at TXO and $\overline{\text{TXO}}$		150	
	TXO at 16 V, $\overline{\text{TXO}}$ is open, Current measured at TXO		150	
	TXO is open, $\overline{\text{TXO}}$ at 16 V, Current measured at TXO		150	
	TXO at 16 V, $\overline{\text{TXO}}$ at 16 V, Current measured at TXO and $\overline{\text{TXO}}$		150	
Receiver fault condition current	RXI shorted to $\overline{\text{RXI}}$, Current measured in short		10	mA
	RXI at 0 V, $\overline{\text{RXI}}$ is open, Current measured at RXI		3	
	RXI is open, $\overline{\text{RXI}}$ at 0 V, Current measured at RXI		3	
	RXI at 0 V, $\overline{\text{RXI}}$ at 0 V, Current measured at RXI and $\overline{\text{RXI}}$		3	
	RXI at 16 V, $\overline{\text{RXI}}$ at open, Current measured at RXI		10	
	RXI at open, $\overline{\text{RXI}}$ at 16 V, Current measured at $\overline{\text{RXI}}$		10	
	RXI at 16 V, $\overline{\text{RXI}}$ at 16 V, Current measured at RXI and $\overline{\text{RXI}}$		10	

† Fault conditions should be measured on only one channel at a time.



SN75ALS085

LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

SLLS054B – APRIL 1989 – REVISED MAY 1995

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

driver

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t _{PLH}	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 3		15	ns
t _{PHL}	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 3		15	ns
t _{PIL}	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 4		25	ns
t _{PIL}	TXEN	TXO, $\overline{\text{TXO}}$	TXI at 3.2 V, See Figure 5		25	ns
t _w		TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 6	260	8000	ns
V _{OD(U)}	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 6		-100	mV
t _{sk}	TXI	TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 3		±3	ns
t _r		TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 3	1	5	ns
t _f		TXO, $\overline{\text{TXO}}$	TXEN at 2 V, See Figure 3	1	5	ns

receiver

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t _{PLH}	$\overline{\text{RXI}}$, RXI	RXO	V _{IC} = 1 V to 4.2 V, See Figure 10		15	ns
t _{PHL}	$\overline{\text{RXI}}$, RXI	RXO	V _{IC} = 1 V to 4.2 V, See Figure 10		15	ns
t _{PLH}	$\overline{\text{RXI}}$, RXI	RXEN	V _{IC} = 1 V to 4.2 V, V _{ID} = -500 mV, See Figure 12		55	ns
t _{PHL}	$\overline{\text{RXI}}$, RXI	RXEN	V _{IC} = 1 V to 4.2 V, V _{ID} = 500 mV, See Figure 12	142	181	ns
t _{sk}	$\overline{\text{RXI}}$, RXI	RXO	V _{IC} = 1 V to 4.2 V, V _{ID} = 500 mV, See Figure 10		±3	ns
t _w			V _{IC} = 1 V to 4.2 V, V _{ID} = -175 mV, See Figure 11	25		ns
t _w			V _{IC} = 1 V to 4.2 V, V _{ID} = -275 mV, See Figure 11		50	ns
t _{r1}			V _{IC} = 1 V to 4.2 V, V _{ID} = ±500 mV, See Figure 10	1	8	ns
t _{r2}			V _{IC} = 1 V to 4.2 V, V _{ID} = ±500 mV, See Figure 12	1	8	ns
t _{f1}			V _{IC} = 1 V to 4.2 V, V _{ID} = ±500 mV, See Figure 10	1	8	ns
t _{f2}			V _{IC} = 2.5 V, V _{ID} = ±500 V, See Figure 12	1	8	ns
t _v			See Figure 10	-10	15	ns



SN75ALS085 LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

SLLS054B – APRIL 1989 – REVISED MAY 1995

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

loop

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t _{PLH}	Propogation delay time, low-to-high level output	TXI	RXO	LOOP at 0.8 V, TXEN at 2 V, See Figure 13	30	ns
t _{PHL}	Propogation delay time, high-to-low level output	TXI	RXO	LOOP at 0.8 V, TXEN at 2 V, See Figure 13	30	ns
t _{PLH}	Propogation delay time, low-to-high level output	TXEN	RXEN	LOOP at 0.8 V, See Figure 14	50	ns
t _{PHL}	Propogation delay time, high-to-low level output	TXEN	RXEN	LOOP at 0.8 V, See Figure 14	50	ns

PARAMETER MEASUREMENT INFORMATION

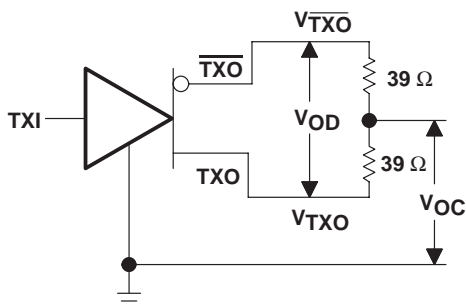


Figure 1. Driver Test Circuit

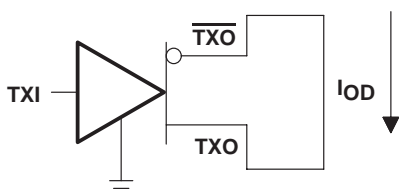
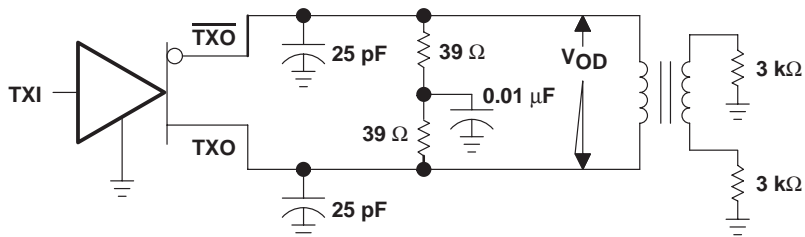
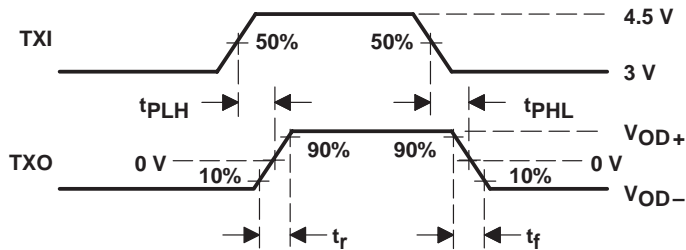


Figure 2. Driver Test Circuit

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

TRANSFORMER SPECIFICATIONS

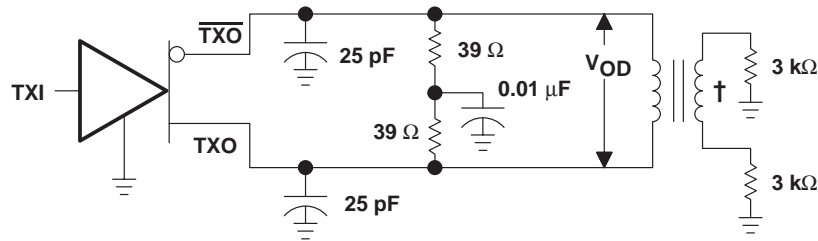
Turns Ratio	1:1
Magnetizing Inductance	26 to 30 μ H
Winding Resistance	0.6 Ω Max
Rise Time 10% to 90%	5 ns Max
Interwinding Capacitance	25 pF
Leakage Inductance	0.25 μ H Max
Inductive Q	1250 Min

Figure 3. Test Circuit and Voltage Waveforms

SN75ALS085 LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

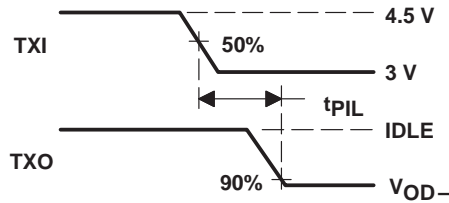
SLLS054B – APRIL 1989 – REVISED MAY 1995

PARAMETER MEASUREMENT INFORMATION



† See Figure 3

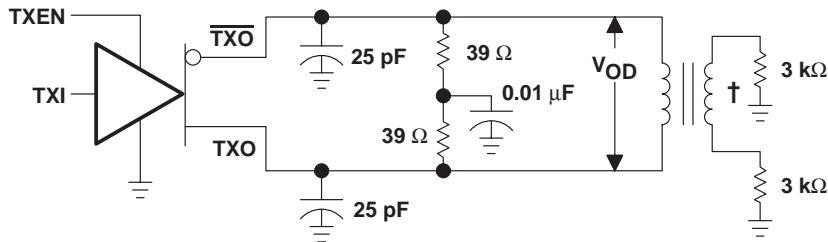
TEST CIRCUIT



VOLTAGE WAVEFORMS

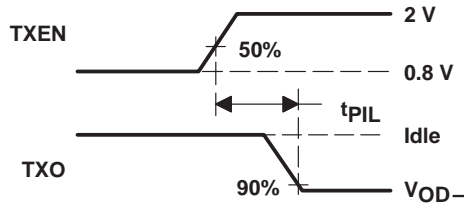
NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 4. Test Circuit and Voltage Waveforms



† See Figure 3

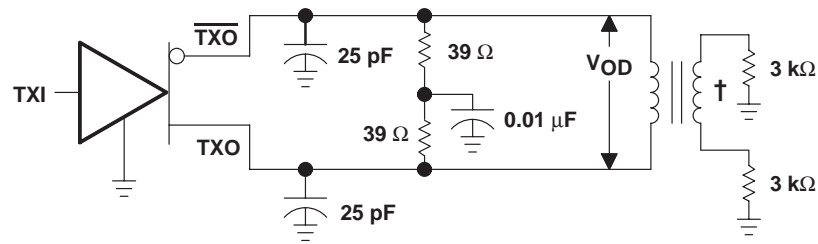
TEST CIRCUIT



VOLTAGE WAVEFORMS

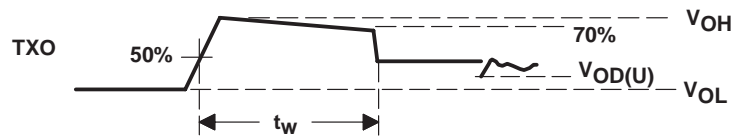
Figure 5. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



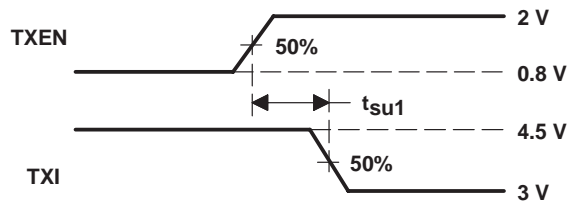
† See Figure 3

TEST CIRCUIT



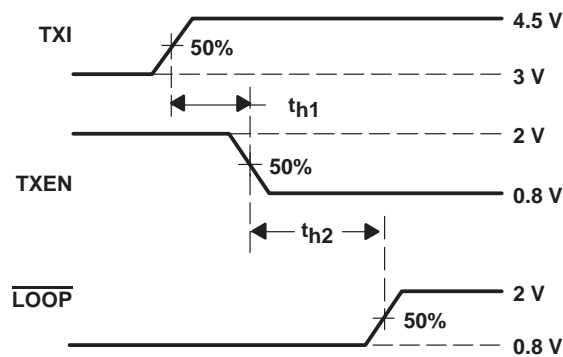
VOLTAGE WAVEFORMS

Figure 6. Test Circuit and Voltage Waveforms



NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 7



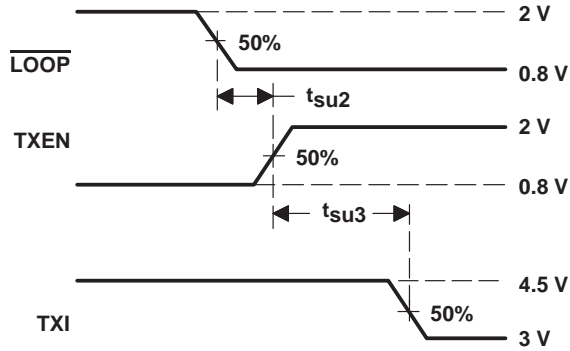
NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 8

SN75ALS085 LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

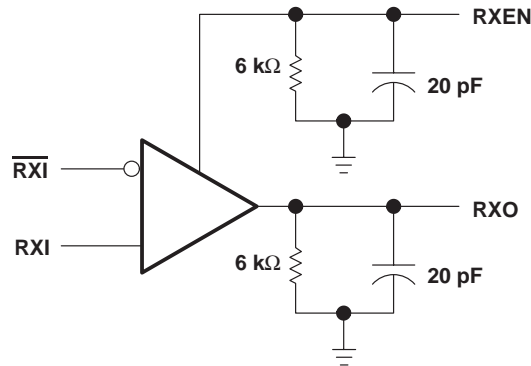
SLLS054B – APRIL 1989 – REVISED MAY 1995

PARAMETER MEASUREMENT INFORMATION

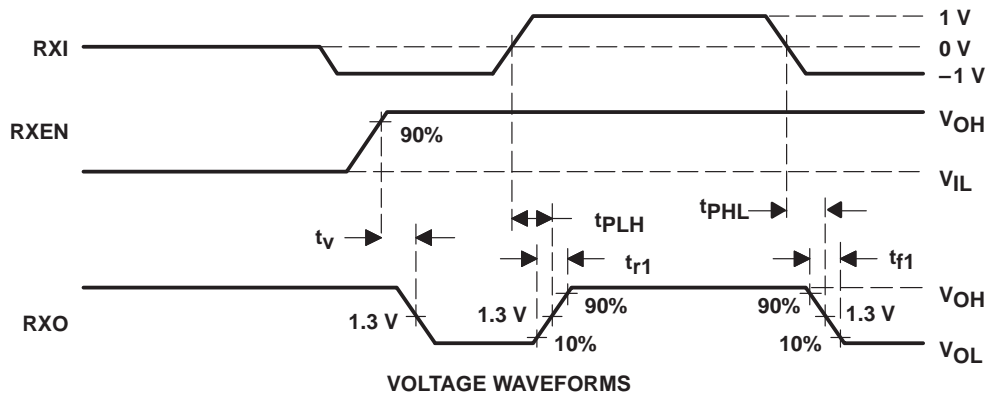


NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 9



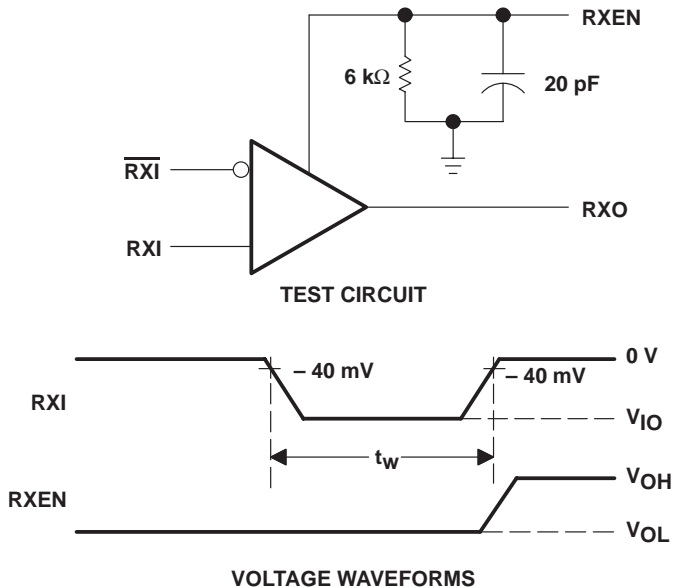
TEST CIRCUIT



NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

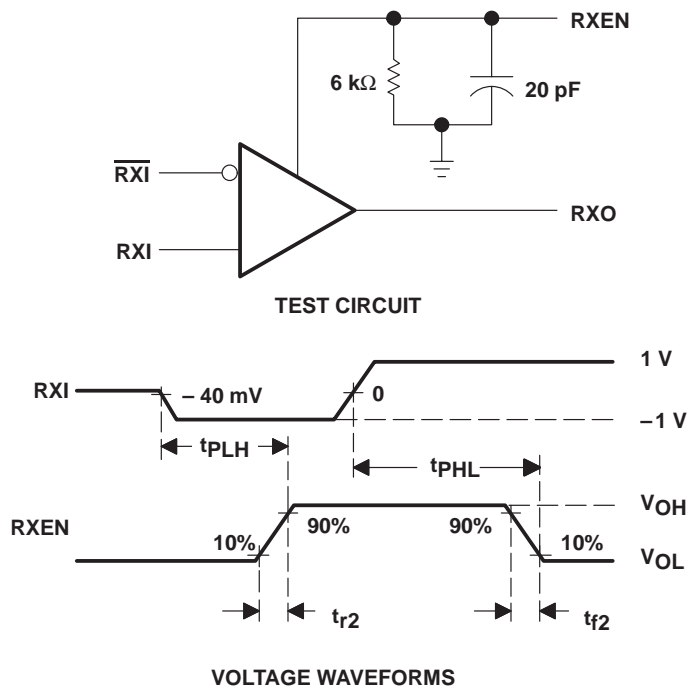
Figure 10. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 11. Test Circuit and Voltage Waveforms



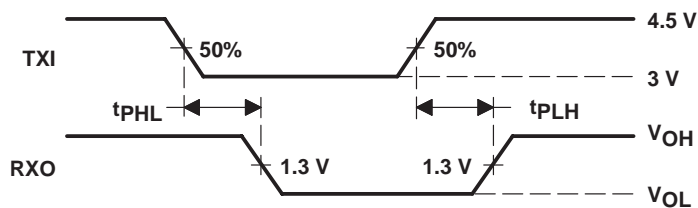
NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 12. Test Circuit and Voltage Waveforms

SN75ALS085 LAN ACCESS UNIT INTERFACE DUAL DRIVER/RECEIVER

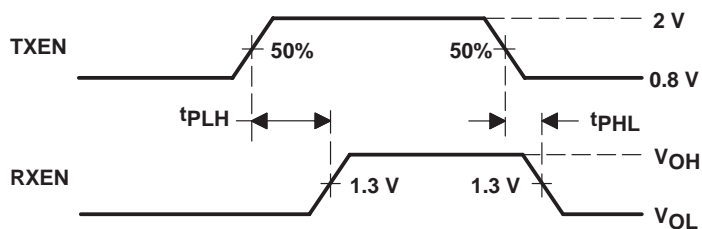
SLLS054B – APRIL 1989 – REVISED MAY 1995

PARAMETER MEASUREMENT INFORMATION



NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 13



NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 14

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.