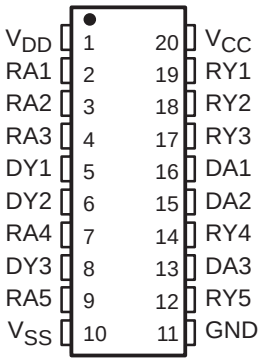
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Single Chip With Easy Interface Between UART and Serial Port Connector**
- **Less Than 9-mW Power Consumption**
- **Wide Driver Supply Voltage . . . 4.5 V to 13.2 V**
- **Driver Output Slew Rate Limited to 30 V/μs Max**
- **Receiver Input Hysteresis . . . 1100 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1-μs Noise Filter**
- **Functionally Interchangeable With Texas Instruments SN75185**

DW OR N PACKAGE
(TOP VIEW)



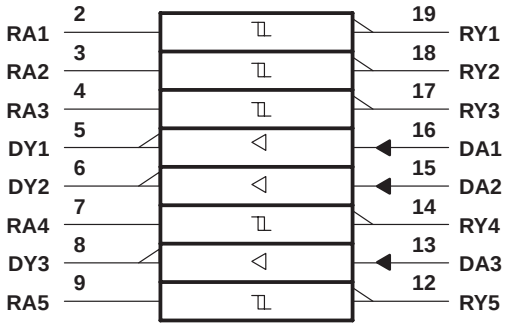
description

The SN75C185 is a low-power BiMOS device containing three independent drivers and five receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). The SN75C185 will typically replace one SN75188 and two SN75189 devices. This device is designed to conform to ANSI Standards EIA/TIA-232-E. The three drivers and five receivers of the SN75C185 are similar to those of the SN75C188 quad drivers and SN75C189A quad receivers, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/μs and the receivers have filters that reject input noise pulses that are shorter than 1 μs. Both these features eliminate the need for external components.

The SN75C185 has been designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in this device will interface to single inputs of peripheral devices such as ACEs, UARTS, or micro-processors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN75C185 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

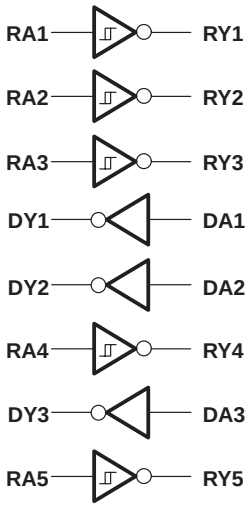
The SN75C185 is characterized for operation from 0°C to 70°C.

logic symbol†

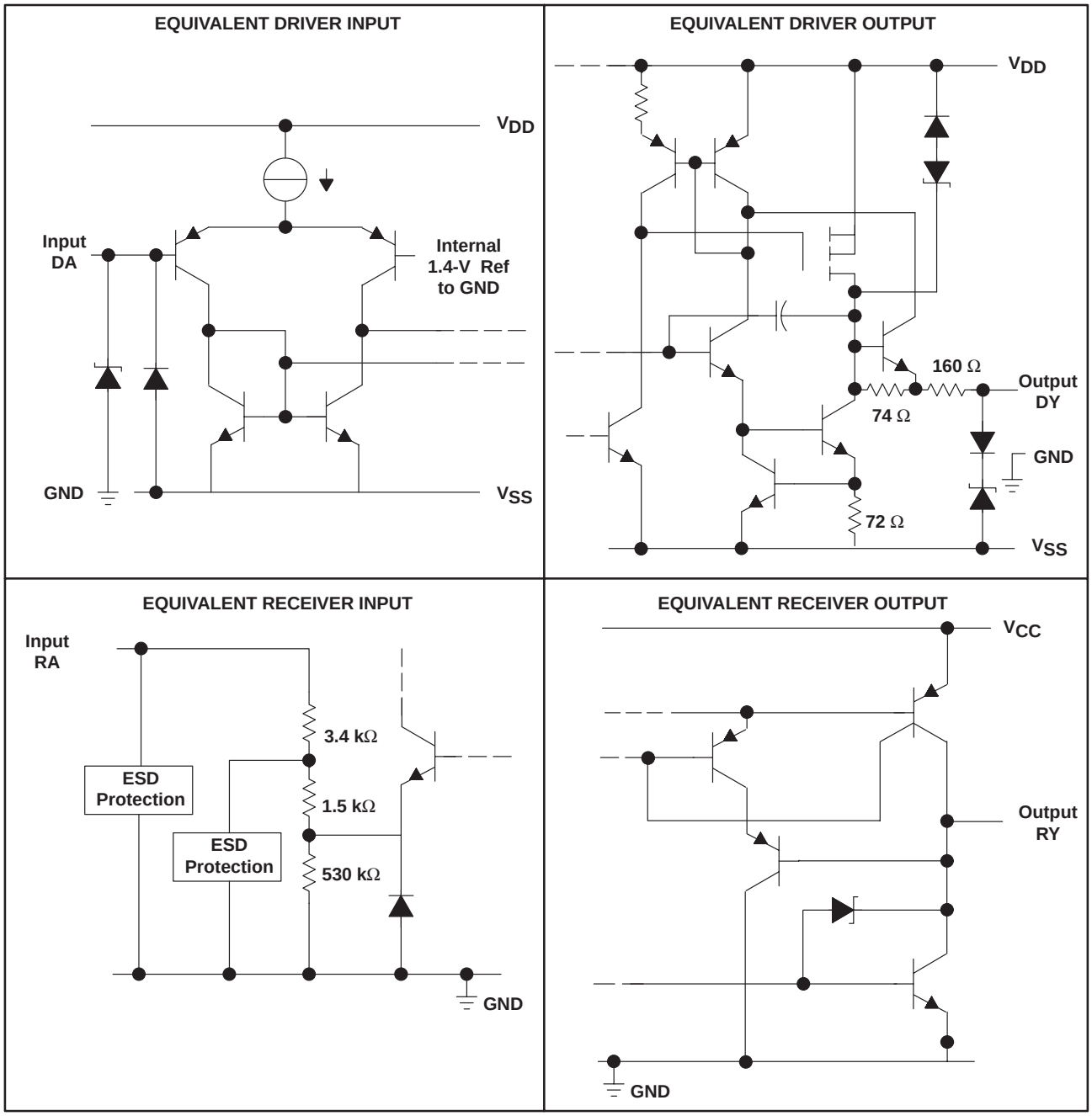


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



equivalent schematics of inputs and outputs



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 13.5 V
Supply voltage, V_{SS} . . . . . –13.5 V
Supply voltage, V_{CC} . . . . . 7 V
Input voltage range, V_I: Driver . . . . . V_{SS} to V_{DD}
Receiver . . . . . –30 V to 30 V
Output voltage range, V_O: Driver . . . . . V_{SS} – 6 V to V_{DD} + 6 V
Receiver . . . . . –0.3 V to V_{CC} + 0.3 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A \le 75°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	12	13.2	V
Supply voltage, V_{SS}		–4.5	–12	–13.2	V
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I (see Note 2)	Driver	$V_{SS}+2$		V_{DD}	V
	Receiver	–25		25	
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}				0.8	
High-level output current, I_{OH}	Receiver			–1	mA
High-level output current, I_{OL}				3.2	mA
Operating free-air temperature, T_A		0		70	°C

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if –10 V is a maximum, the typical value is a more negative voltage.

supply currents

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V,	V_{SS} = –5 V		115	200	µA
			V_{DD} = 12 V,	V_{SS} = –12 V		115	200	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V,	V_{SS} = –5 V		–115	–200	µA
			V_{DD} = 12 V,	V_{SS} = –12 V		–115	–200	
I_{CC}	Supply current from V_{CC}	No load All inputs at 0 or 5 V	V_{DD} = 5 V,	V_{SS} = –5 V			750	µA
			V_{DD} = 12 V,	V_{SS} = –12 V			750	

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V,	V_{SS} = –5 V	4	4.5		V
			V_{DD} = 12 V	V_{SS} = –12 V	10	10.8		
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V,	V_{SS} = –5 V		–4.4	–4	V
			V_{DD} = 12 V	V_{SS} = –12 V		–10.7	–10	
I_{IH}	High-level input current	V_I = 5 V, See Figure 2					1	µA
I_{IL}	Low-level input current	V_I = 0, See Figure 2					–1	µA
$I_{OS(H)}$	High-level short-circuit output current (see Note 3)	V_I = 0.8 V, See FIgure 1	V_O = 0 or V_O = V_{SS},		–4.5	–12	–19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current (see Note 3)	V_I = 2 V, See Figure 1	V_O = 0 or V_O = V_{DD},		4.5	12	19.5	mA
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0, See Note 4	V_O = – 2 V to 2 V,		300	400		Ω

† All typical values are at T_A = 25°C.

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if –10 V is a maximum, the typical value is a more negative voltage.
3. Not more than one output should be shorted at one time.
4. Test conditions are those specified by EIA/TIA-232-E.

switching characteristics, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ±10%, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output (see Note 5)	R_L = 3 kΩ to 7 kΩ, See Figure 3	C_L = 15 pF,		1.2	3	µs
t_{PHL}	Propagation delay time, high- to low-level output (see Note 5)				2.5	3.5	µs
t_{TLH}	Transition time, low- to high-level output			0.53	2	3.2	µs
t_{THL}	Transition time, high- to low-level output			0.53	2	3.2	µs
t_{TLH}	Transition time, low- to high-level output (see Note 6)	R_L = 3 kΩ to 7 kΩ, See Figure 3	C_L = 2500 pF,		1		µs
t_{THL}	Transition time, high- to low-level output (see Note 6)				1		µs
S_R	Output slew rate (see Note 6)	R_L = 3 kΩ to 7 kΩ, See Figure 3	C_L = 15 pF,	4	10	30	V/µs

NOTES: 5. t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.
6. Measured between 3-V and –3-V points of output waveform (EIA/TIA-232-E conditions), all unused inputs tied either high or low.

RECEIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshhold voltage	See Figure 5			1.6	2.1	2.55	V
V_{IT-}	Negative-going input threshhold voltage	See Figure 5			0.65	1	1.25	V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)				600	1100		mV
V_{OH}	High-level output voltage	V_I = 0.75 V,	I_{OH} = −20 µA,	See Figure 5 and Note 7	3.5			V
		V_I = 0.75 V, I_{OH} = −1 mA, See Figure 5	V_{CC} = 4.5 V		2.8	4.4		
			V_{CC} = 5 V		3.8	4.9		
			V_{CC} = 5.5 V		4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V,	I_{OL} = 3.2 mA,	See Figure 5		0.17	0.4	V
I_{IH}	High-level input current	V_I = 3 V			0.43	0.55	1	mA
		V_I = 25 V			3.6	4.6	8.3	
I_{IL}	Low-level input current	V_I = −3 V			−0.43	−0.55	−1	mA
		V_I = −25 V			−3.6	−5.0	−8.3	
$I_{OS(H)}$	Short-circuit output at high level	V_I = 0.75 V,	V_O = 0,	See Figure 4		−8	−15	mA
$I_{OS(L)}$	Short-circuit output at low level	V_I = V_{CC},	V_O = V_{CC},	See Figure 4		13	25	mA

† All typical values are at T_A = 25°C.

NOTE 7: If the inputs are left unconnected, the receiver interprets this as an input low, and the receiver outputs remain in the high state.

switching characteristics, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10%, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 5 kΩ,	C_L = 50 pF,	See Figure 6		3	4	µs
t_{PHL}	Propagation delay time, high- to low-level output					3	4	µs
t_{TLH}	Transition time, low- to high-level output					300	450	ns
t_{THL}	Transition time, high- to low-level output					100	300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise (see Note 8)	R_L = 5 kΩ,	C_L = 50 pF,	See Figure 6	1		4	µs

NOTE 8: The receiver ignores any postive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

PARAMETER MEASUREMENT INFORMATION

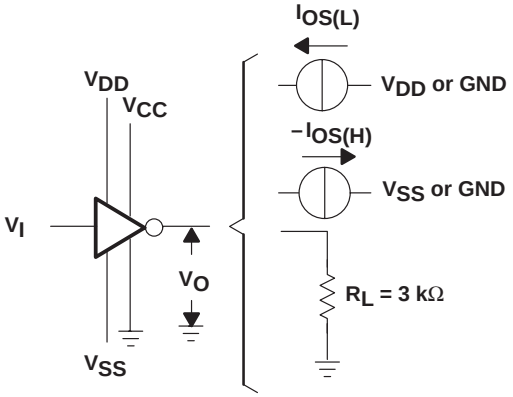


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

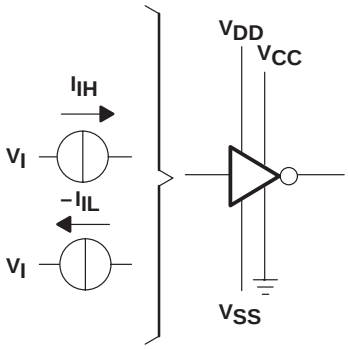
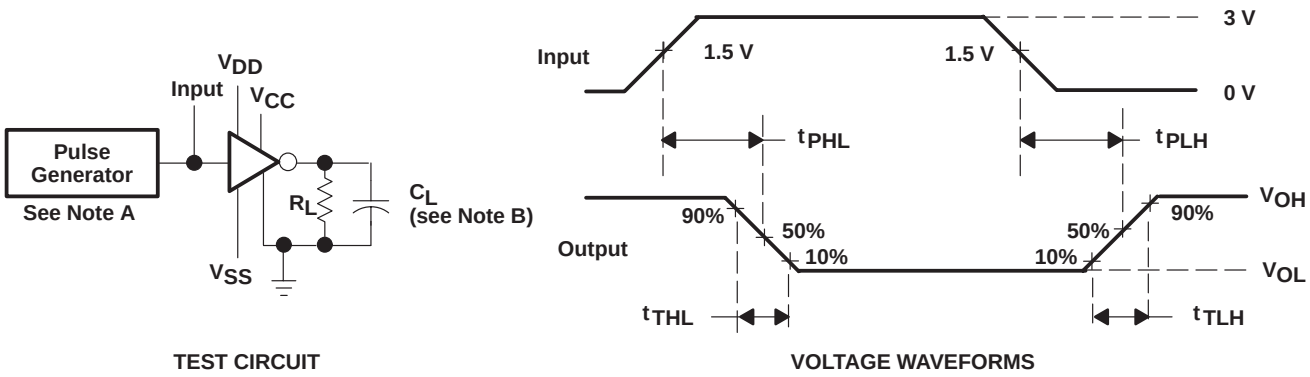


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



NOTES: A. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

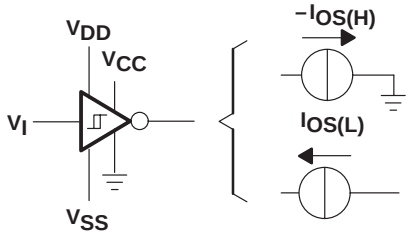


Figure 4. Receiver Test Circuit for $I_{OS(H)}$ and $I_{OS(L)}$

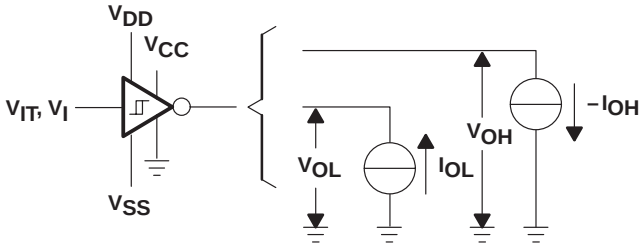
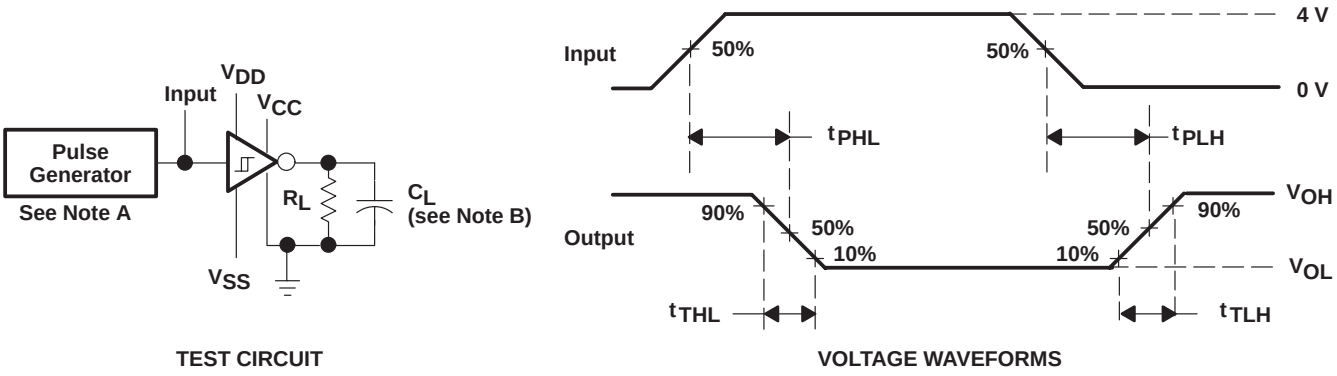


Figure 5. Receiver Test Circuit for V_{IT}, V_{OH}, and V_{OL}



NOTES: A. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

APPLICATION INFORMATION

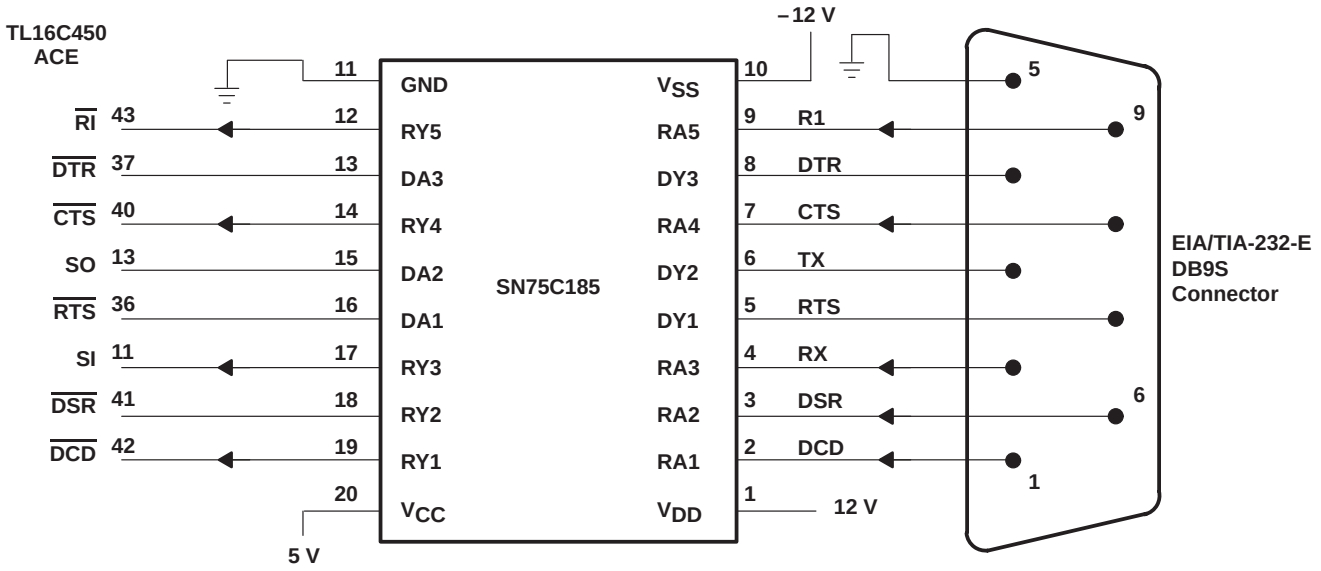


Figure 7. Typical Connection

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