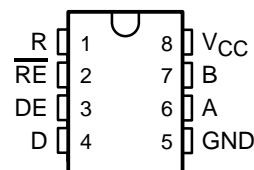- Bidirectional Transceiver
- Meet or Exceed the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)
- High-Speed Low-Power LinBiCMOS™ Circuitry
- Designed for High-Speed Operation in Both Serial and Parallel Applications
- Low Skew
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Very Low Disabled Supply-Current Requirements . . . 200 μA Maximum
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ±60 mA
- Thermal-Shutdown Protection
- Driver Positive-and Negative-Current Limiting
- Open-Circuit Fail-Safe Receiver Design
- Receiver Input Sensitivity . . . ±200 mV Max
- Receiver Input Hysteresis . . . 50 mV Typ
- Operate From a Single 5-V Supply
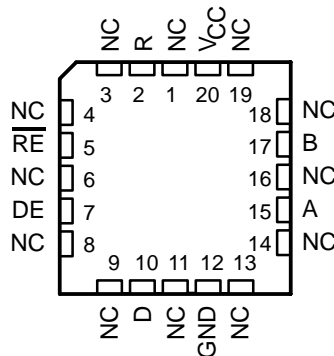- Glitch-Free Power-Up and Power-Down Protection

description

The SN55LBC176, SN65LBC176, and SN75LBC176 differential bus transceivers are monolithic, integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. They are designed for balanced transmission lines and meet ANSI Standard RS-485 and ISO 8482:1987(E).

The SN65LBC176 and SN75LBC176 combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can externally connect together to function as a direction control. The driver differential outputs and the receiver differential

D, JG, OR P PACKAGE
(TOP VIEW)

R	1	8	V_{CC}
$\overline{RE}$	2	7	B
DE	3	6	A
D	4	5	GND

FK PACKAGE
(TOP VIEW)

Top pins: NC(3), R(2), NC(1), V_{CC}(20), NC(19)

NC	4	18	NC
$\overline{RE}$	5	17	B
NC	6	16	NC
DE	7	15	A
NC	8	14	NC

Bottom pins: NC(9), D(10), NC(11), GND(12), NC(13)

NC – No internal connection

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A − B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level,   L = low level,   ? = indeterminate,
X = irrelevant,   Z = high impedance (off)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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TEXAS INSTRUMENTS

SN55LBC176, SN65LBC176, SN75LBC176
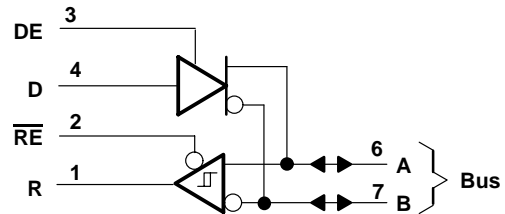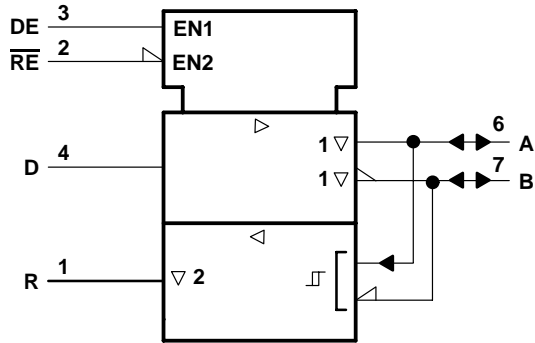# DIFFERENTIAL BUS TRANSCEIVERS

description (continued)

inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications. Very low device supply current can be achieved by disabling the driver and the receiver. Both the driver and receiver are available as cells in the Texas Instruments LinASIC™ Library.

These transceivers are suitable for ANSI Standard RS-485 and ISO 8482:1987 (E) applications to the extent that they are specified in the operating conditions and characteristics section of this data sheet. Certain limits contained in the ANSI Standard RS-485 and ISO 8482:1987 (E) are not met or cannot be tested over the entire military temperature range.

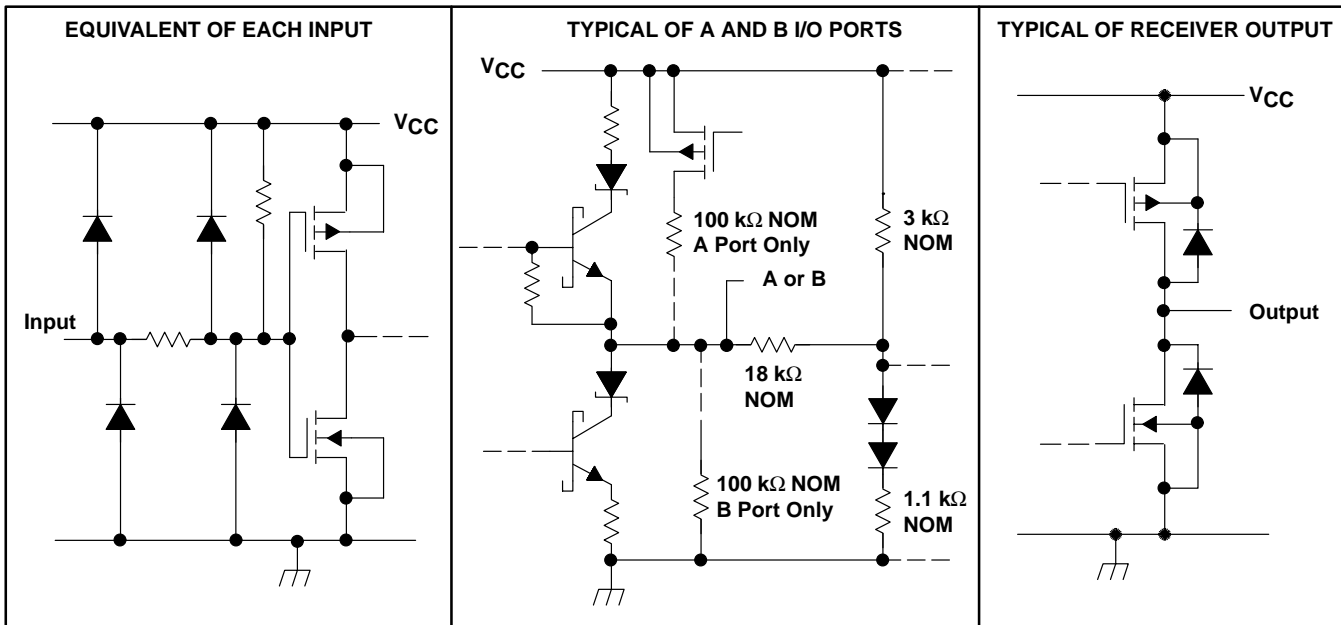The SN55LBC176 is characterized for operation from −55°C to 125°C. The SN65LBC176 is characterized for operation from −40°C to 85°C, and the SN75LBC176 is characterized for operation from 0°C to 70°C.

logic symbol†   logic diagram (positive logic)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and
  IEC Publication 617-12.

schematics of inputs and outputs

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Voltage range at any bus terminal . . . . −10 V to 15 V
Enable input voltage, V_I . . . . 5.5 V
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55LBC176 . . . . −55°C to 125°C
                                                                    SN65LBC176 . . . . −40°C to 85°C
                                                                    SN75LBC176 . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1:   All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 110°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	440 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN55LBC176	4.5	5	5.5	V
	SN65/75LBC176	4.75	5	5.25	
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN55LBC176	−55		125	°C
	SN65LBC176	−40		85	
	SN75LBC176	0		70	

NOTE 2:   Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

SN55LBC176, SN65LBC176, SN75LBC176
DIFFERENTIAL BUS TRANSCEIVERS

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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$			0	6	V
$|V_{OD1}|$	Differential output voltage	$I_O = 0$			1.5	6	V
$|V_{OD2}|$	Differential output voltage	$R_L = 54$ Ω, See Note 3	See Figure 1,	55LBC176	1.1		V
				65LBC176	1.1		
				75LBC176	1.5	5	
V_{OD3}	Differential output voltage	$V_{test} = -7$ V to 12 V, See Note 3	See Figure 2,	55LCB176	1.1		V
				65LBC176	1.1		
				75LBC176	1.5	5	
$\Delta|V_{OD}|$	Change in magnitude of differential output voltage †					±0.2	V
V_{OC}	Common-mode output voltage	$R_L = 54$ Ω or 100 Ω,	See Figure 1			3	V
						−1	
$\Delta|V_{OC}|$	Change in magnitude of common-mode output voltage†					±0.2	V
I_O	Output current	Output disabled, See Note 4	$V_O = 12$ V			1	mA
			$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V				−100	µA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−100	µA
I_{OS}	Short-circuit output current	$V_O = -7$ V				−250	mA
		$V_O = 0$				−150	
		$V_O = V_{CC}$				250	
		$V_O = 12$ V					
I_{CC}	Supply current	$V_I = 0$ or V_{CC}, No load	Receiver disabled and driver enabled	55LBC176		1.75	mA
				65LBC176		1.5	
				75LBC176			
			Receiver and driver disabled	55LBC176		0.25	
				65LBC176			
				75LBC176		0.2	

† $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.

NOTES: 3. This device meets the ANSI Standard RS-485 V_{OD} requirements above 0°C only.
4. This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		SN55LBC176			SN65LBC176 SN75LBC176			UNIT
				MIN	TYP	MAX	MIN	TYP†	MAX	
$t_{d(OD)}$	Differential output delay time	$R_L = 54\ \Omega$, $\quad C_L = 50\ pF$, See Figure 3		8		31	8		25	ns
$t_{t(OD)}$	Differential output transition time				12			12		ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(ODH)} - t_{d(ODL)}\rvert$)					6		0	6	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$,	See Figure 4			65			35	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$,	See Figure 5			65			35	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$,	See Figure 4			105			60	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$,	See Figure 5			105			35	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-485
V_O	V_{oa}, V_{ob}
$\lvert V_{OD1}\rvert$	V_o
$\lvert V_{OD2}\rvert$	V_t ($R_L = 54\ \Omega$)
$\lvert V_{OD3}\rvert$	V_t (test termination measurement 2)
$\Delta\lvert V_{OD}\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V_t}\rvert\rvert$
V_{OC}	$\lvert V_{os}\rvert$
$\Delta\lvert V_{OC}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$
I_{OS}	None
I_O	I_{ia}, I_{ib}

TEXAS INSTRUMENTS

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
$V_{IT−}$	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA		−0.2‡			V
V_{hys}	Hysteresis voltage (V_{IT+} − $V_{IT−}$) (see Figure 4)					50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OH} = −400 µA,		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OL} = 8 mA,				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	µA
I_I	Line input current	Other input = 0 V, See Note 5	V_I = 12 V				1	mA
			V_I = −7 V				−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					−100	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					−100	µA
r_I	Input resistance					12		kΩ
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver enabled and driver disabled				3.9	mA
			Receiver and driver disabled	SN55LBC176			0.25	mA
				SN65LBC176			0.25	
				SN75LBC176			0.2	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 5: This applies for both power on and power off. Refer to ANSI Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF

PARAMETER		TEST CONDITIONS	SN55LBC176		SN65LBC176 SN75LBC176			UNIT
			MIN	MAX	MIN	TYP†	MAX	
t_{PLH}	Propagation delay time, low- to high-level single-ended output	V_{ID} = −1.5 V to 1.5 V, See Figure 7	11	37	11		33	ns
t_{PHL}	Propagation delay time, high- to low-level single-ended output		11	37	11		33	ns
$t_{sk(p)}$	Pulse skew ($\mid t_{d(ODH)} − t_{d(ODL)} \mid$)			6		3	6	ns
t_{PZH}	Output enable time to high level	See Figure 8		35			35	ns
t_{PZL}	Output enable time to low level			35			30	ns
t_{PHZ}	Output disable time from high level	See Figure 8		35			35	ns
t_{PLZ}	Output disable time from low level			35			30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

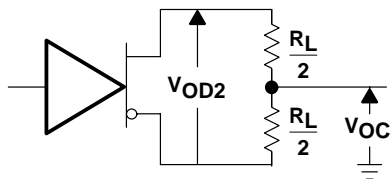POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

Figure 1. Driver V_{OD} and V_{OC}
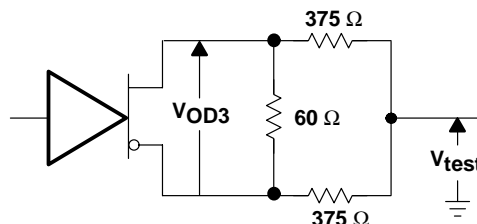
Figure 2. Driver V_{OD3}

Figure 3. Driver Test Circuit and Voltage Waveforms
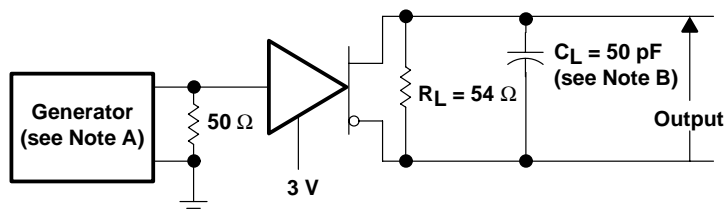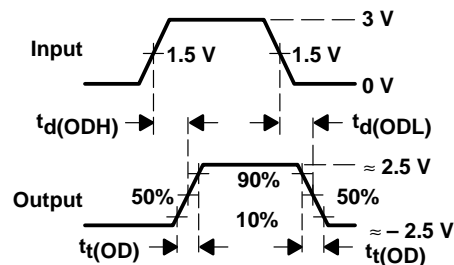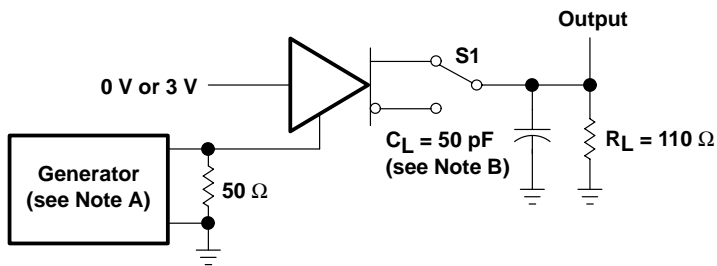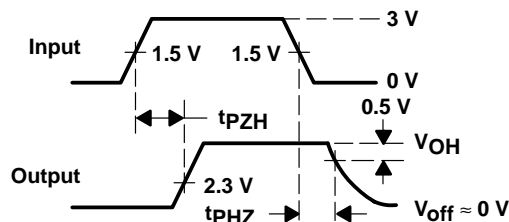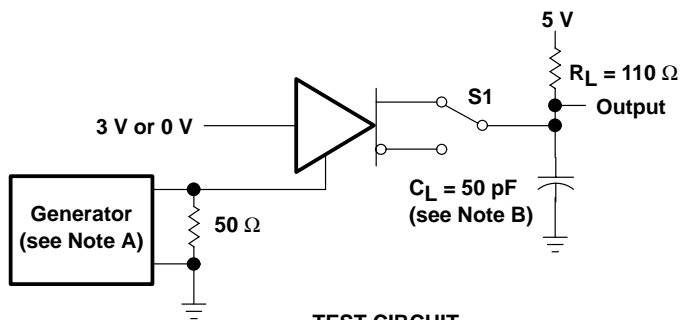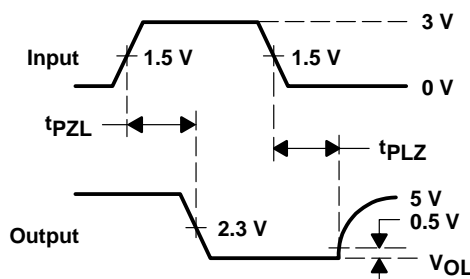
Figure 4. Driver Test Circuit and Voltage Waveforms

Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
        B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

Figure 6. Receiver V_{OH} and V_{OL}
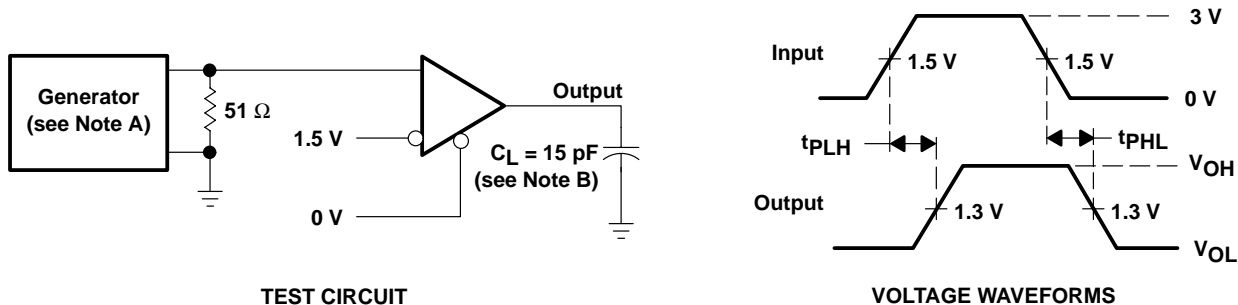
TEST CIRCUIT	VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
       B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

Figure 8. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
   B. C_L includes probe and jig capacitance.

SN55LBC176, SN65LBC176, SN75LBC176
DIFFERENTIAL BUS TRANSCEIVERS

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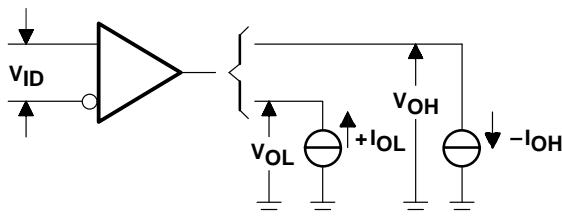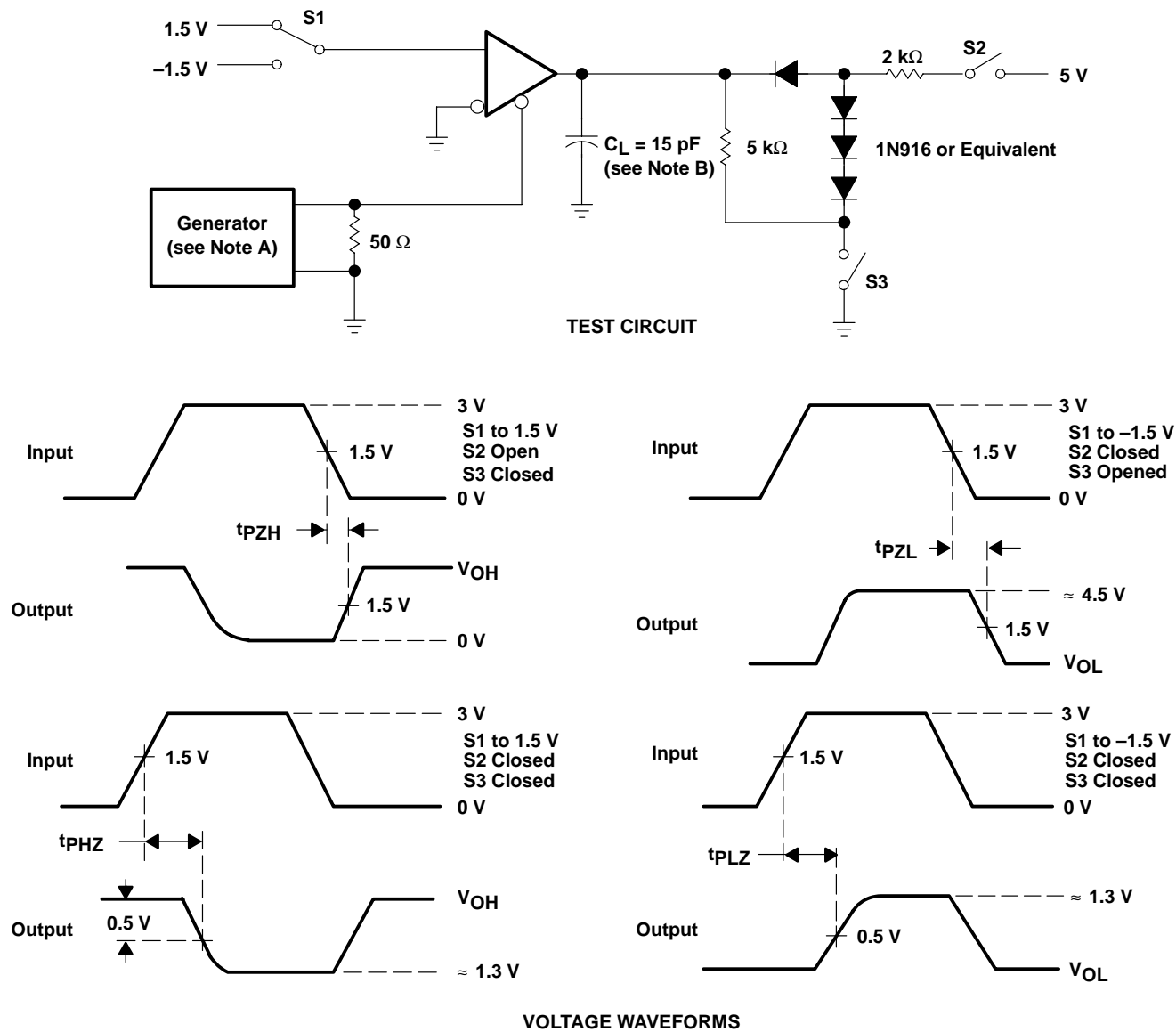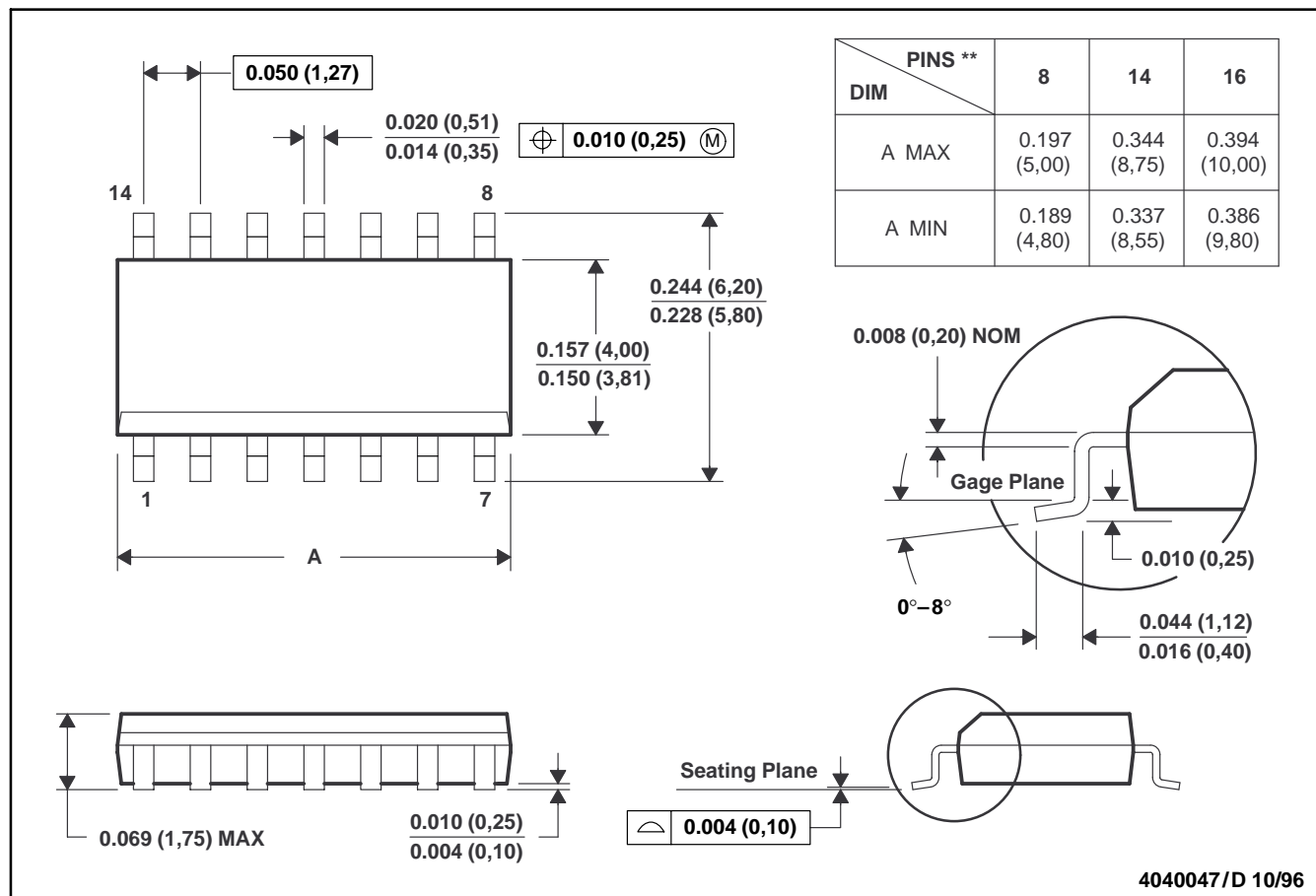
MECHANICAL INFORMATION

D (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

PINS ** DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

0.050 (1,27)

0.020 (0,51)
0.014 (0,35)   ⊕ 0.010 (0,25) Ⓜ

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,81)

1   7

A

0.008 (0,20) NOM

Gage Plane

0°−8°

0.010 (0,25)

0.044 (1,12)
0.016 (0,40)

0.069 (1,75) MAX

0.010 (0,25)
0.004 (0,10)

Seating Plane

⌒ 0.004 (0,10)

4040047 / D 10/96

NOTES: C. All linear dimensions are in inches (millimeters).
        D. This drawing is subject to change without notice.
        E. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
        F. Falls within JEDEC MS-012

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10

MECHANICAL INFORMATION

FK (S-CQCC-N)**

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN
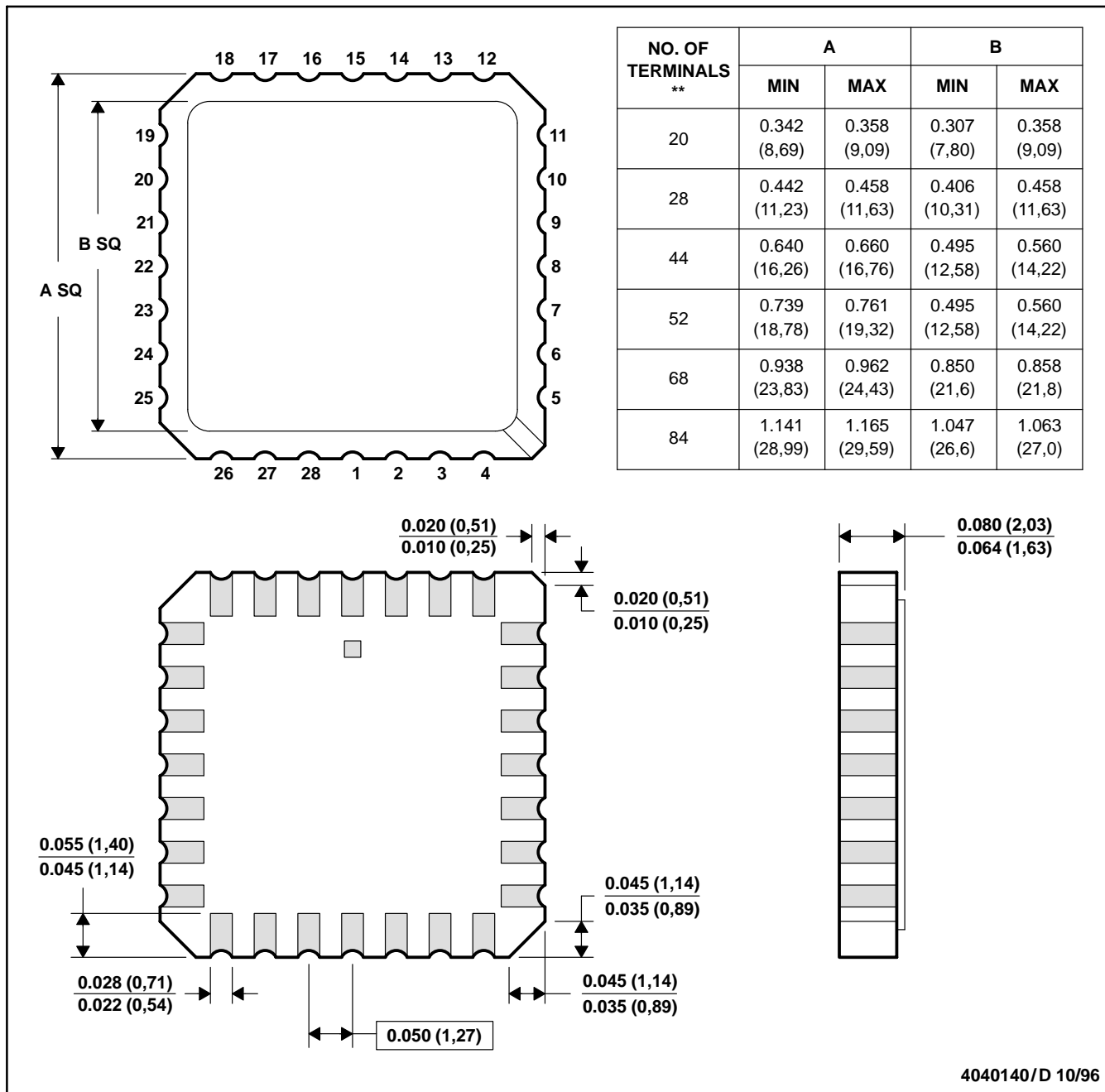
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
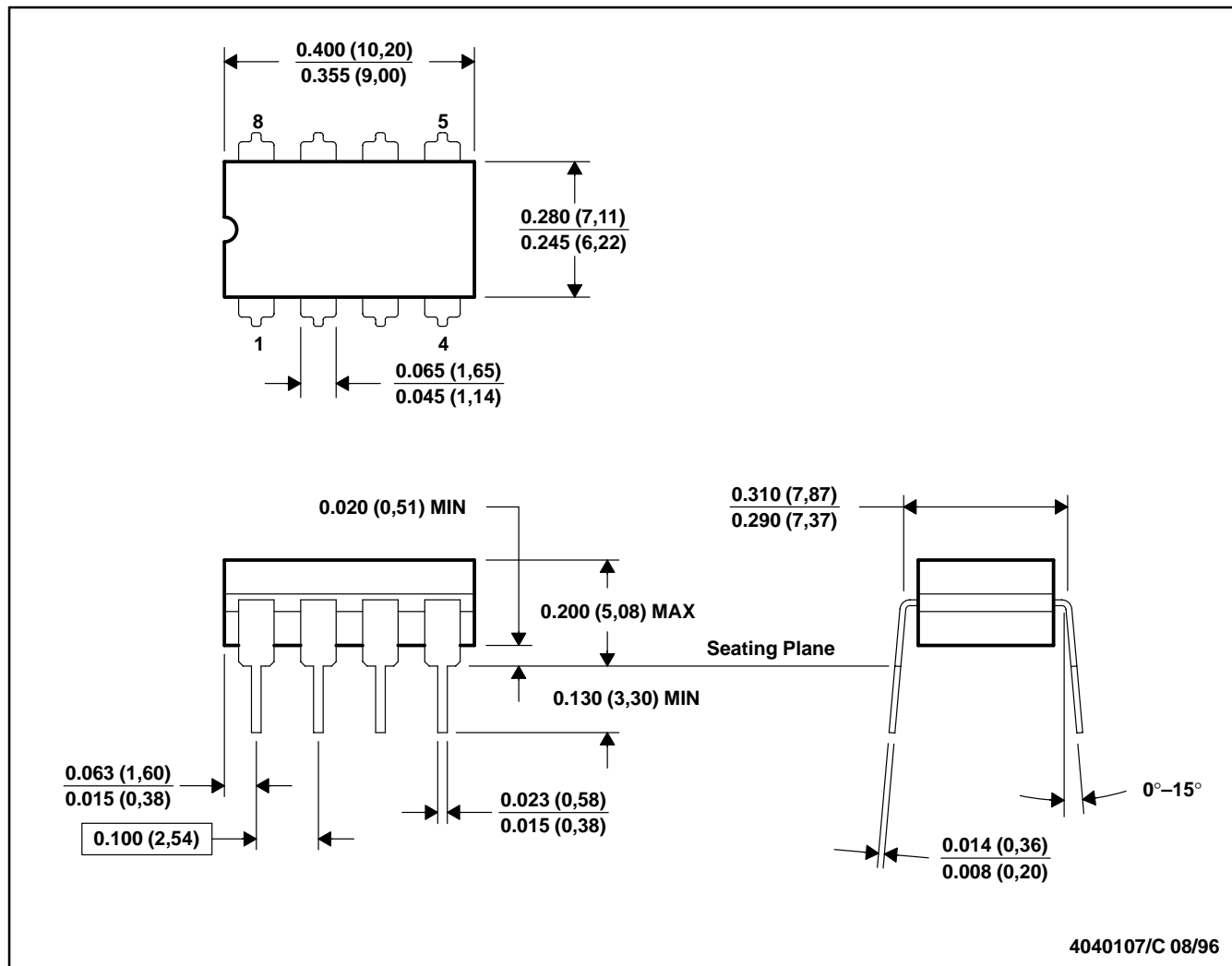E. Falls within JEDEC MS-004

![Texas Instruments logo]

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MECHANICAL INFORMATION

JG (R-GDIP-T8)   **CERAMIC DUAL-IN-LINE PACKAGE**

$$\frac{0.400\ (10,20)}{0.355\ (9,00)}$$

8   5

$$\frac{0.280\ (7,11)}{0.245\ (6,22)}$$

1   4

$$\frac{0.065\ (1,65)}{0.045\ (1,14)}$$

0.020 (0,51) MIN

$$\frac{0.310\ (7,87)}{0.290\ (7,37)}$$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$$\frac{0.063\ (1,60)}{0.015\ (0,38)}$$

$$\frac{0.023\ (0,58)}{0.015\ (0,38)}$$

0°–15°

0.100 (2,54)

$$\frac{0.014\ (0,36)}{0.008\ (0,20)}$$

4040107/C 08/96

NOTES: A. All linear dimensions are in inches (millimeters).
   B. This drawing is subject to change without notice.
   C. This package can be hermetically sealed with a ceramic lid using glass frit.
   D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
   E. Falls within MIL-STD-1835 GDIP1-T8
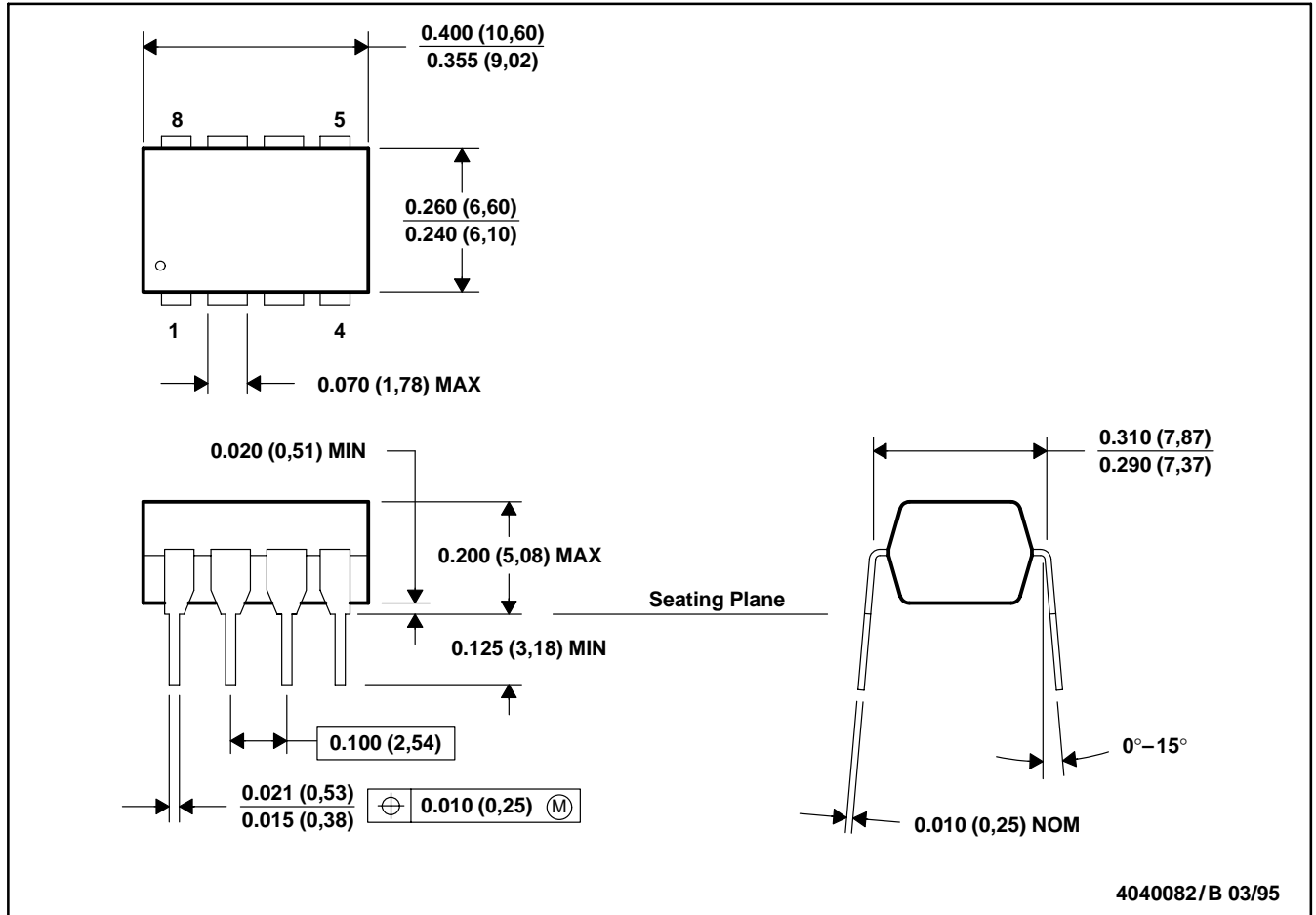
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MECHANICAL INFORMATION

P (R-PDIP-T8)   **PLASTIC DUAL-IN-LINE PACKAGE**

$$\frac{0.400\ (10,60)}{0.355\ (9,02)}$$

$$\frac{0.260\ (6,60)}{0.240\ (6,10)}$$

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

$$\frac{0.021\ (0,53)}{0.015\ (0,38)}$$ ⊕ 0.010 (0,25) Ⓜ

$$\frac{0.310\ (7,87)}{0.290\ (7,37)}$$

0°−15°

0.010 (0,25) NOM

4040082 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

TEXAS
INSTRUMENTS

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