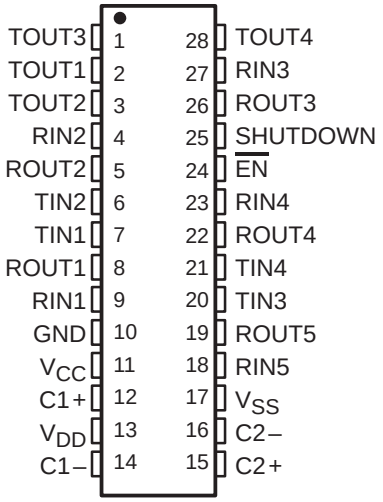
SLLS137D – MAY 1992 – REVISED MAY 1995

- **Operates With Single 5-V Power Supply**
- **Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-232-E and ITU Recommendation V.28**
- **Improved Performance Replacement for MAX241**
- **Operate at Data Rates Up to 100 kbs Over a 3-Meter Cable**
- **Low-Power Shutdown Mode: ≤1 μA Typ**
- **LinBiCMOS™ Process Technology**
- **Four Drivers and Five Receivers**
- **±30-V Input Levels**
- **3-State TTL/CMOS Receiver Outputs**
- **±9-V Output Swing With a 5-V Supply**
- **Applications**
  - **EIA/TIA-232-E Interface**
  - **Battery-Powered Systems**
  - **Terminals**
  - **Modems**
  - **Computers**

DW PACKAGE
(TOP VIEW)



description

The SN75LBC241† is a low-power LinBiCMOS™ line interface device containing four independent drivers and five receivers. It is designed to provide a plug-in replacement for the Maxim MAX241. The SN75LBC241 provides a capacitive charge-pump voltage generator to produce EIA/TIA-232 voltage levels from a 5-V supply. The charge-pump oscillator frequency is 20 kHz. Each receiver converts EIA/TIA-232 inputs to 5-V TTL/CMOS levels. The receivers have a typical threshold of 1.2 V and a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into EIA/TIA-232 levels.

The SN75LBC241 includes a receiver, 3-state control line and a low-power shutdown control line. Whenever the $\overline{EN}$ line is high, the receiver outputs are placed in a high-impedance state. When $\overline{EN}$ is low, normal operation is enabled.

The shutdown mode reduces power dissipation to less than 5 μW typically. In this mode, receiver outputs have high impedance, driver outputs are turned off, and the charge-pump circuit is turned off. When SHUTDOWN is high, the shutdown mode is enabled. When SHUTDOWN is low, normal operation is enabled.

This device has been designed to conform to ANSI Standard EIA/TIA-232-E and ITU Recommendation V.28 specifications.

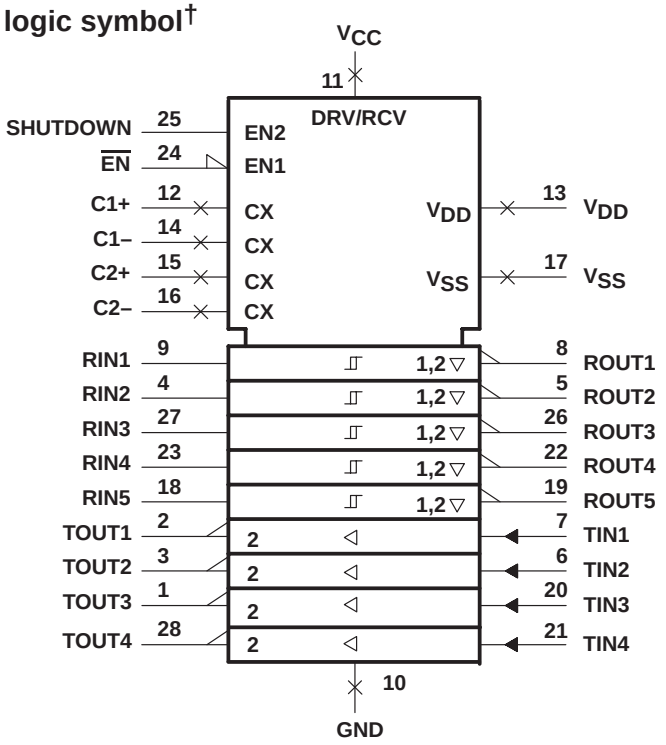
The SN75LBC241 has been designed using LinBiCMOS™ technology and cells contained in the TI's LinASIC™ library. Use of LinBiCMOS™ circuitry increases latch-up immunity in this device over an all-CMOS design.

The SN75LBC241 is characterized for operation from 0°C to 70°C.

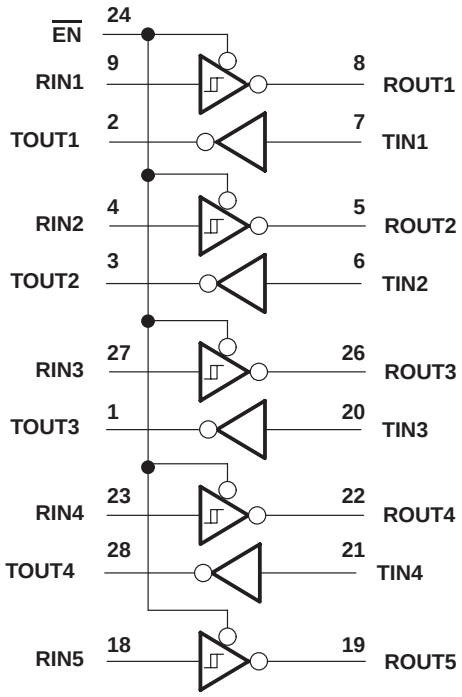
† Patent pending

LinBiCMOS and LinASIC are trademarks of Texas Instruments Incorporated.

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Input supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 6 V
Positive output supply voltage range, V_{DD} . . . . . V_{CC} – 0.3 V to 15 V
Negative output supply voltage range, V_{SS} . . . . . 0.3 V to –15 V
Input voltage range, V_I: Driver . . . . . –0.3 V to V_{CC} + 0.3 V
Receiver . . . . . ±30 V
Output voltage range, V_O: TOUT . . . . . V_{SS} – 0.3 V to V_{DD} + 0.3 V
ROUT . . . . . –0.3 V to V_{CC} + 0.3 V
Short-circuit duration: TOUT . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1348 mW	10.8 mW/°C	862 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	TIN	2			V
	$\overline{EN}$, SHUTDOWN	2.4			
Low-level input voltage, V_{IL}	TIN, $\overline{EN}$, SHUTDOWN			0.8	V
External charge-pump capacitor	C1–C4 (see Figure 1)	1			μF
External charge-pump capacitor voltage rating	C1, C3 (see Figure 1)	6.3			V
	C2, C4 (see Figure 1)	16			
Receiver input voltage, V_I				±30	V
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	TOUT	R_L = 3 kΩ to GND, See Note 2	5	9		V
		ROUT	I_{OH} = –1 mA	3.5			
V_{OL}	Low-level output voltage	TOUT	R_L = 3 kΩ to GND, See Note 3		–9‡	–5	V
		ROUT	I_{OL} = 3.2 mA			0.4	
V_{IT+}	Receiver positive-going input threshold voltage	RIN	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
$V_{IT–}$	Receiver negative-going input threshold voltage	RIN	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage ($V_{IT+} – V_{IT–}$)	RIN	V_{CC} = 5 V		0.5	1	V
r_i	Receiver input resistance	RIN	V_{CC} = 5 V, T_A = 25°C	3	5	7	kΩ
r_o	Output resistance	TOUT	$V_{DD} = V_{SS} = V_{CC} = 0$, V_O = ±2 V	300			Ω
I_{OS}	Short circuit output current§	TOUT	V_{CC} = 5.5 V, V_O = 0		±10		mA
I_{IS}	Short circuit input current	TIN	V_I = 0			200	μA
I_{CC}	Supply current		V_{CC} = 5.5 V, T_A = 25°C, All outputs open		4	8	mA
			All outputs open, T_A = 25°C, Shutdown terminal high		1	10	μA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
§ Not more than one output should be shorted at one time.
NOTES: 2. Total I_{OH} drawn from TOUT1, TOUT2, TOUT3, TOUT4 and V_{DD} terminal should not exceed 12 mA.
3. Total I_{OL} drawn from TOUT1, TOUT2, TOUT3, TOUT4 and V_{SS} terminal should not exceed –12 mA.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	See Figure 2		500		ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	See Figure 2		500		ns
t_{PZH}	Receiver output enable time to high level	See Figure 5		100		ns
t_{PZL}	Receiver output enable time to low level	See Figure 5		100		ns
t_{PHZ}	Receiver output disable time from high level	See Figure 5		50		ns
t_{PLZ}	Receiver output disable time from low level	See Figure 5		50		ns
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 4			30	V/µs
$SR_{(tr)}$	Driver transition region slew rate	C_L = 2500 pF, See Figure 4	4	6		V/µs

APPLICATION INFORMATION

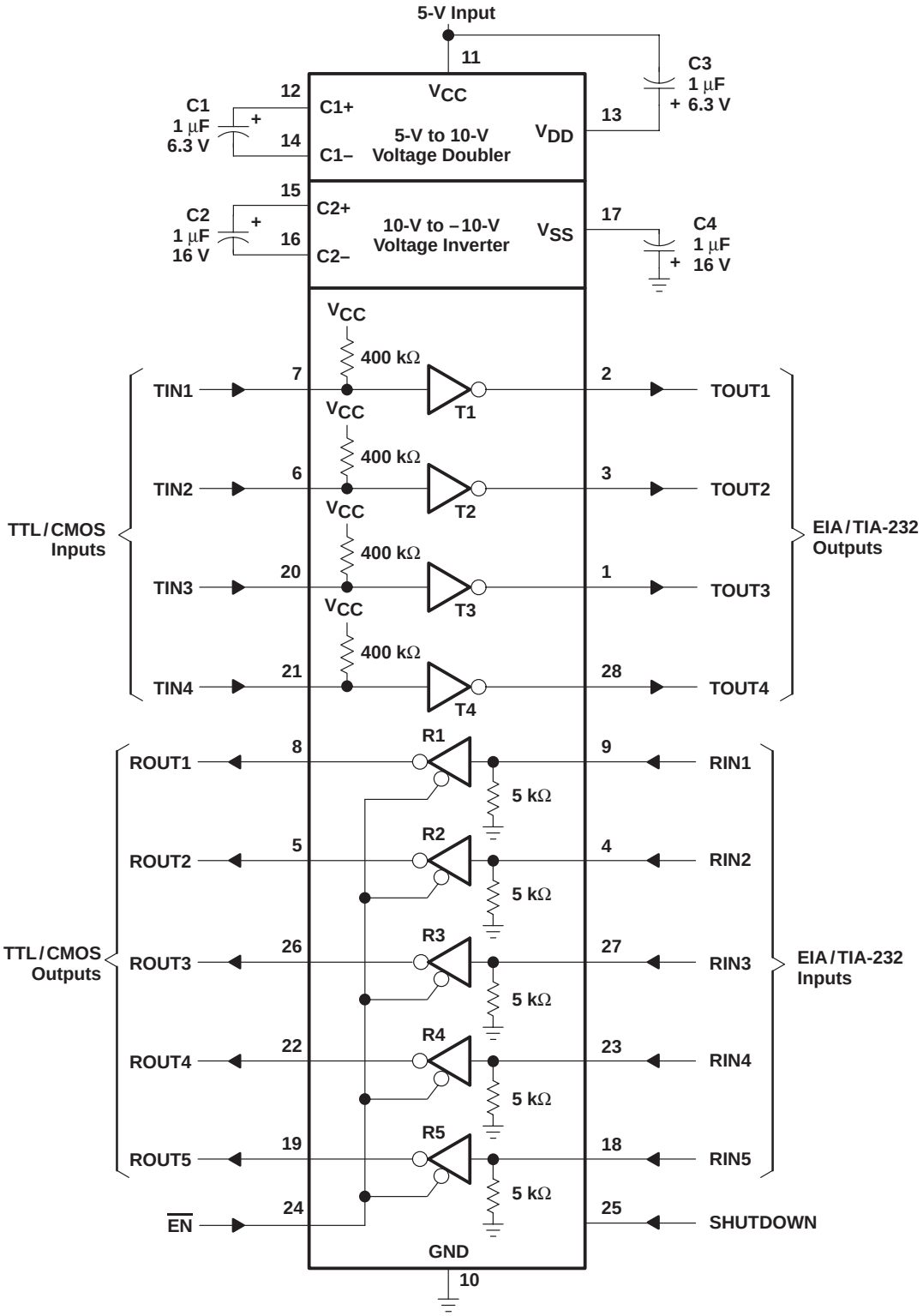


Figure 1. Typical Operating Circuit

PARAMETER MEASUREMENT INFORMATION

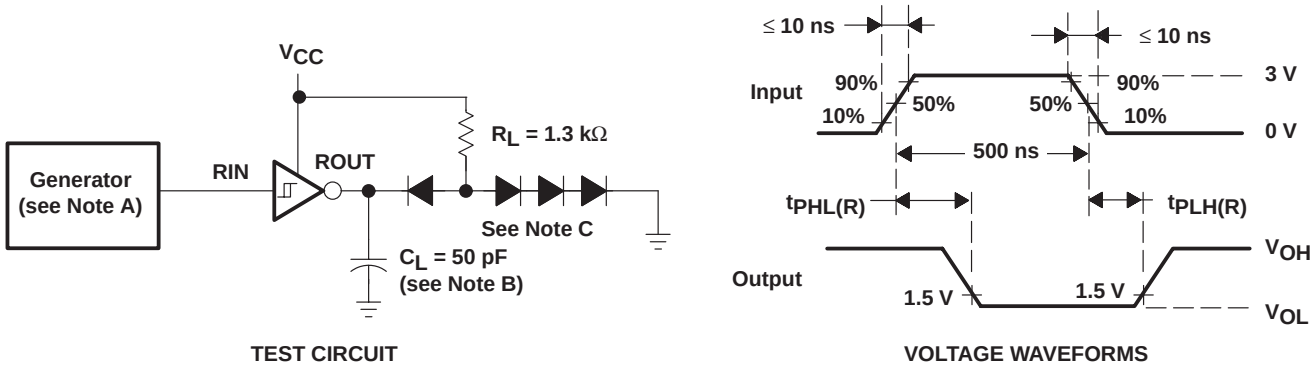


Figure 2. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement

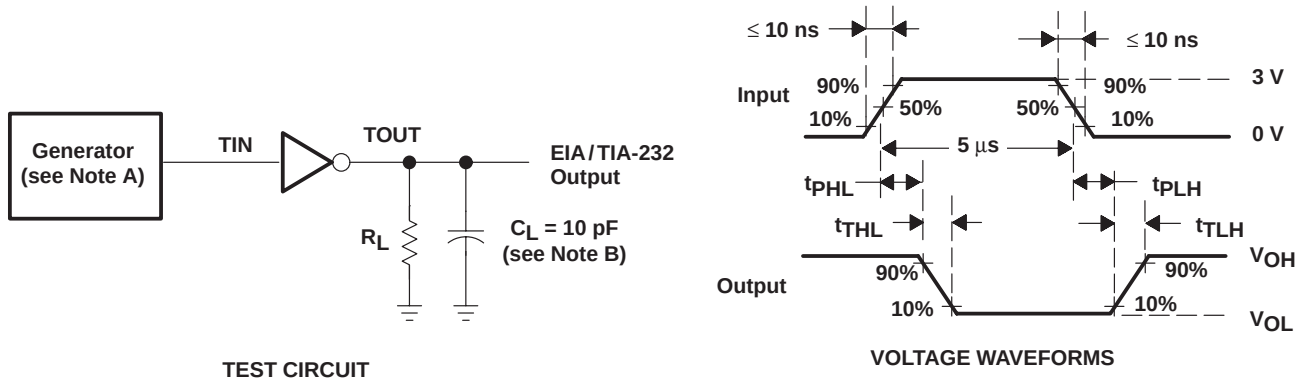
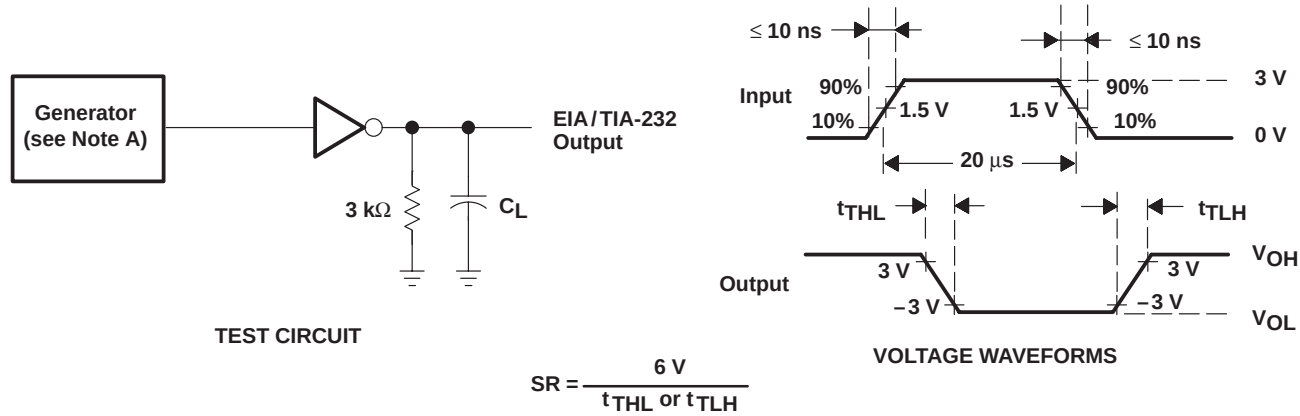


Figure 3. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement (5-μs Input)



$$SR = \frac{6\ V}{t_{THL}\ \text{or}\ t_{TLH}}$$

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 4. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurement (20-μs Input)

PARAMETER MEASUREMENT INFORMATION

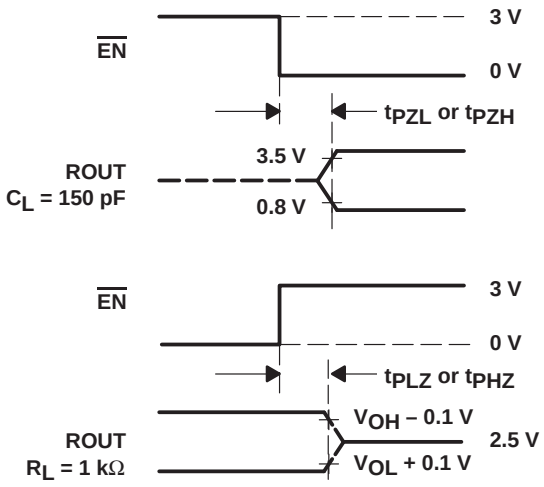


Figure 5. Receiver Output Enable and Disable Timing

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.