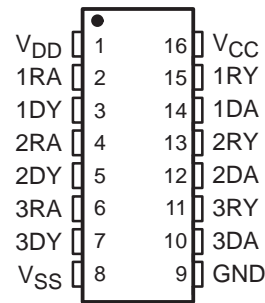


# SN75C1406 TRIPLE LOW-POWER DRIVERS/RECEIVERS

SLLS148C – MAY 1990 – REVISED MARCH 1997

- Meet or Exceed the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28
- Very Low Power Consumption  
5 mW Typ
- Wide Driver Supply Voltage Range  
 $\pm 4.5$  V to  $\pm 15$  V
- Driver Output Slew Rate Limited to  
30 V/ $\mu$ s Max
- Receiver Input Hysteresis . . . 1000 mV Typ
- Push-Pull Receiver Outputs
- On-Chip Receiver 1- $\mu$ s Noise Filter
- Functionally Interchangeable With Motorola MC145406 and Texas Instruments TL145406

D, DW, OR N PACKAGE  
(TOP VIEW)



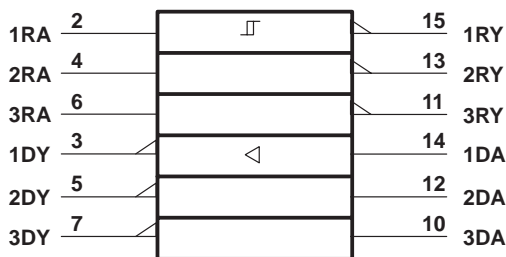
## description

The SN75C1406 is a low-power BiMOS device containing three independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device is designed to conform to ANSI EIA/TIA-232-E. The drivers and receivers of the SN75C1406 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/ $\mu$ s, and the receivers have filters that reject input noise pulses shorter than 1  $\mu$ s. Both these features eliminate the need for external components.

The SN75C1406 is designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN75C1406 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN75C1406 is characterized for operation from 0°C to 70°C.

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram

Typical of each receiver



Typical of each driver



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

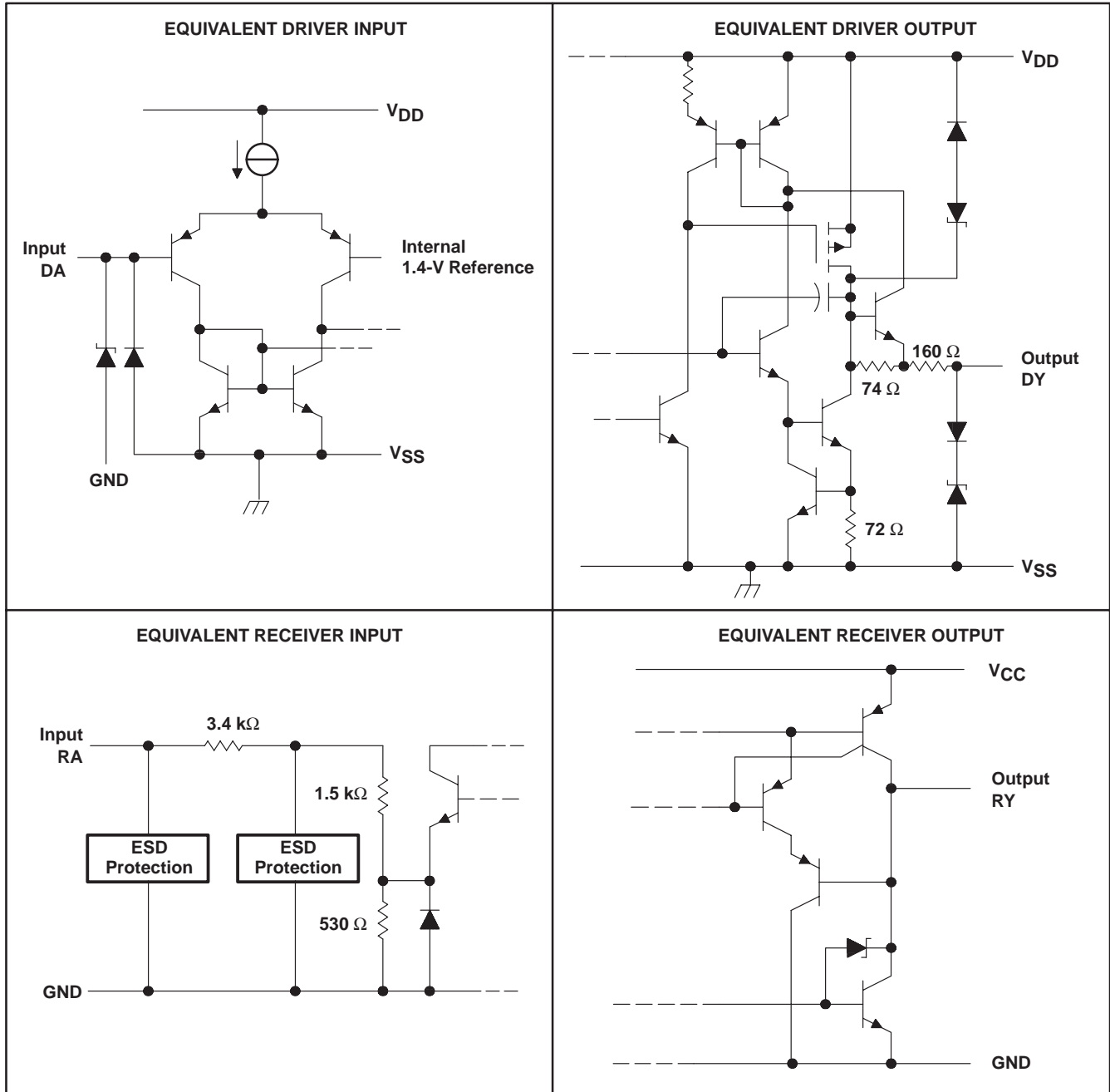
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# SN75C1406 TRIPLE LOW-POWER DRIVERS/RECEIVERS

SLLS148C – MAY 1990 – REVISED MARCH 1997

## schematics of inputs and outputs



All resistor values shown are nominal.

# SN75C1406 TRIPLE LOW-POWER DRIVERS/RECEIVERS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note 1)	15 V
Supply voltage, $V_{SS}$	-15 V
Supply voltage, $V_{CC}$	7 V
Input voltage range, $V_I$ : Driver	$V_{SS}$ to $V_{DD}$
Receiver	-30 V to 30 V
Output voltage range, $V_O$ : Driver	$(V_{SS} - 6\text{ V})$ to $(V_{DD} + 6\text{ V})$
Receiver	-0.3 V to $(V_{CC} + 0.3\text{ V})$
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : SN75C1406	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
DW	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{DD}$		4.5	12	15	V
Supply voltage, $V_{SS}$		-4.5	-12	-15	V
Supply voltage, $V_{CC}$		4.5	5	6	V
Input voltage, $V_I$	Driver	$V_{SS} + 2$		$V_{DD}$	V
	Receiver	$\pm 25$			
High-level input voltage, $V_{IH}$		2			V
Low-level input voltage, $V_{IL}$				0.8	V
High-level output current, $I_{OH}$				-1	mA
Low-level output current, $I_{OL}$				3.2	mA
Operating free-air temperature, $T_A$		0		70	°C



# SN75C1406

## TRIPLE LOW-POWER DRIVERS/RECEIVERS

SLLS148C – MAY 1990 – REVISED MARCH 1997

### DRIVER SECTION

electrical characteristics over operating free-air temperature range,  $V_{DD} = 12\text{ V}$ ,  $V_{SS} = -12\text{ V}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	V <sub>IH</sub> = 0.8 V, See Figure 1	R <sub>L</sub> = 3 kΩ,	V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -5 V	4	4.5	V
				V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V	10	10.8	
V <sub>OL</sub>	Low-level output voltage (see Note 2)	V <sub>IH</sub> = 2 V, See Figure 1	R <sub>L</sub> = 3 kΩ,	V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -5 V	-4.4	-4	V
				V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V	-10.7	-10	
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 5 V,	See Figure 2			1	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0,	See Figure 2			-1	
I <sub>OS(H)</sub>	High-level short circuit output current‡	V <sub>I</sub> = 0.8 V, V <sub>O</sub> = 0 or V <sub>SS</sub> ,	See Figure 1	-7.5	-12	-19.5	mA
I <sub>OS(L)</sub>	Low-level short circuit output current‡	V <sub>I</sub> = 2 V, V <sub>O</sub> = 0 or V <sub>DD</sub> ,	See Figure 1	7.5	12	19.5	mA
I <sub>DD</sub>	Supply current from V <sub>DD</sub>	No load, All inputs at 2 V or 0.8 V		V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -5 V	115	250	μA
				V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V	115	250	
I <sub>SS</sub>	Supply current from V <sub>SS</sub>	No load, All inputs at 2 V or 0.8 V		V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -5 V	-115	-250	μA
				V <sub>DD</sub> = 12 V, V <sub>SS</sub> = -12 V	-115	-250	
r <sub>O</sub>	Output resistance	V <sub>DD</sub> = V <sub>SS</sub> = V <sub>CC</sub> = 0, See Note 3	V <sub>O</sub> = -2 V to 2 V,	300	400		Ω

† All typical values are at T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time.

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.

3. Test conditions are those specified by EIA/TIA-232-E.

switching characteristics at T<sub>A</sub> = 25°C, V<sub>DD</sub> = 12 V, V<sub>SS</sub> = -12 V, V<sub>CC</sub> = 5 V ± 10%

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
t <sub>pLH</sub>	Propagation delay time, low- to high-level output§	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 15 pF, See Figure 3			1.2	3	μs	
t <sub>pHL</sub>	Propagation delay time, high- to low-level output§				2.5	3.5	μs	
t <sub>TLH</sub>	Transition time, low- to high-level output¶				0.53	2	3.2	μs
t <sub>THL</sub>	Transition time, high- to low-level output¶				0.53	2	3.2	μs
t <sub>TLH</sub>	Transition time, low- to high-level output#	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 2500 pF, See Figure 3			1	2	μs	
t <sub>THL</sub>	Transition time, high- to low-level output#	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 2500 pF, See Figure 3			1	2	μs	
SR	Output slew rate	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 15 pF, See Figure 3			4	10	30	V/μs

§ t<sub>pHL</sub> and t<sub>pLH</sub> include the additional time due to on-chip slew rate and are measured at the 50% points.

¶ Measured between 10% and 90% points of output waveform

# Measured between 3-V and -3-V points of output waveform (EIA/TIA-232-E conditions) with all unused inputs tied either high or low



## RECEIVER SECTION

**electrical characteristics over operating free-air temperature range,  $V_{DD} = 12\text{ V}$ ,  $V_{SS} = -12\text{ V}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IT+}$	Positive-going input threshold voltage	See Figure 5	1.7	2	2.55	V
$V_{IT-}$	Negative-going input threshold voltage	See Figure 5	0.65	1	1.25	V
$V_{hys}$	Input hysteresis voltage ( $V_{IT+} - V_{IT-}$ )		600	1000		mV
$V_{OH}$	High-level output voltage	$V_I = 0.75\text{ V}$ , $I_{OH} = -20\text{ }\mu\text{A}$ , See Figure 5 and Note 4	3.5			V
		$V_I = 0.75\text{ V}$ , $I_{OH} = -1\text{ mA}$ , See Figure 5	$V_{CC} = 4.5\text{ V}$	2.8	4.4	
		$V_{CC} = 5\text{ V}$	3.8	4.9		
		$V_{CC} = 5.5\text{ V}$	4.3	5.4		
$V_{OL}$	Low-level output voltage	$V_I = 3\text{ V}$ , $I_{OL} = 3.2\text{ mA}$ , See Figure 5		0.17	0.4	V
$I_{IH}$	High-level input current	$V_I = 2.5\text{ V}$	3.6	4.6	8.3	mA
		$V_I = 3\text{ V}$	0.43	0.55	1	
$I_{IL}$	Low-level input current	$V_I = -2.5\text{ V}$	-3.6	-5	-8.3	mA
		$V_I = -3\text{ V}$	-0.43	-0.55	-1	
$I_{OS(H)}$	High-level short-circuit output current	$V_I = 0.75\text{ V}$ , $V_O = 0$ , See Figure 4		-8	-15	mA
$I_{OS(L)}$	Low-level short-circuit output current	$V_I = V_{CC}$ , $V_O = V_{CC}$ , See Figure 4		13	25	mA
$I_{CC}$	Supply current from $V_{CC}$	No load, All inputs at 0 or 5 V	$V_{DD} = 5\text{ V}$ , $V_{SS} = -5\text{ V}$	320	450	$\mu\text{A}$
			$V_{DD} = 12\text{ V}$ , $V_{SS} = -12\text{ V}$	320	450	

† All typical values are at  $T_A = 25^\circ\text{C}$ .

NOTE 4: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

**switching characteristics at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 12\text{ V}$ ,  $V_{SS} = -12\text{ V}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	$C_L = 50\text{ pF}$ , $R_L = 5\text{ k}\Omega$ , See Figure 6		3	4	$\mu\text{s}$
$t_{PHL}$	Propagation delay time, high- to low-level output			3	4	$\mu\text{s}$
$t_{TLH}$	Transition time, low- to high-level output‡			300	450	ns
$t_{THL}$	Transition time, high- to low-level output‡			100	300	ns
$t_{W(N)}$	Duration of longest pulse rejected as noise§	$C_L = 50\text{ pF}$ , $R_L = 5\text{ k}\Omega$	1		4	$\mu\text{s}$

‡ Measured between 10% and 90% points of output waveform

§ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of  $t_{W(N)}$  and accepts any positive- or negative-going pulse greater than the maximum of  $t_{W(N)}$ .

PARAMETER MEASUREMENT INFORMATION

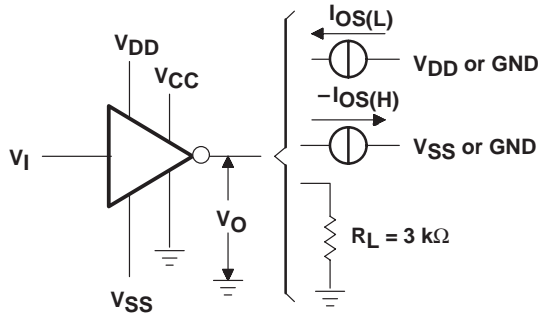


Figure 1. Driver Test Circuit  
 $V_{OH}$ ,  $V_{OL}$ ,  $I_{OS(L)}$ ,  $I_{OS(H)}$

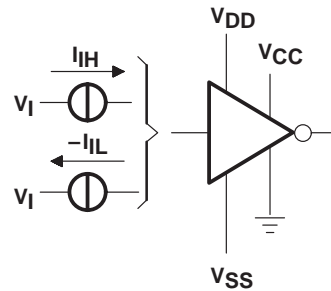
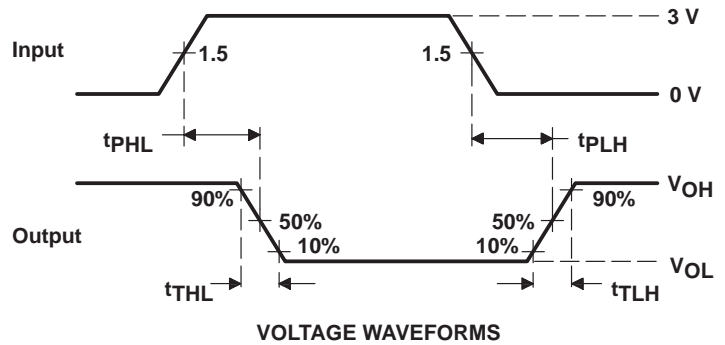
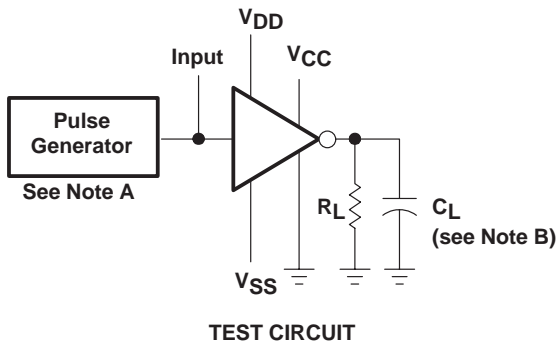


Figure 2. Driver Test Circuit,  $I_{IL}$ ,  $I_{IH}$



NOTES: A. The pulse generator has the following characteristics:  $t_w = 25 \mu s$ ,  $PRR = 20 \text{ kHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = t_f < 50 \text{ ns}$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

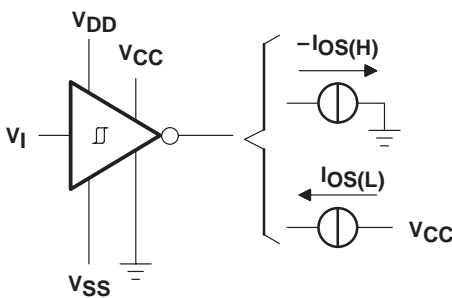


Figure 4. Receiver Test Circuit,  $I_{OS(H)}$ ,  $I_{OS(L)}$

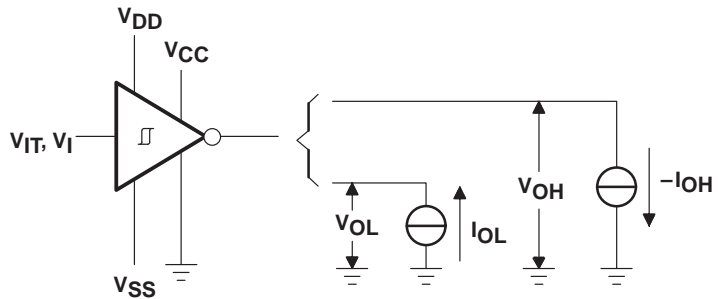
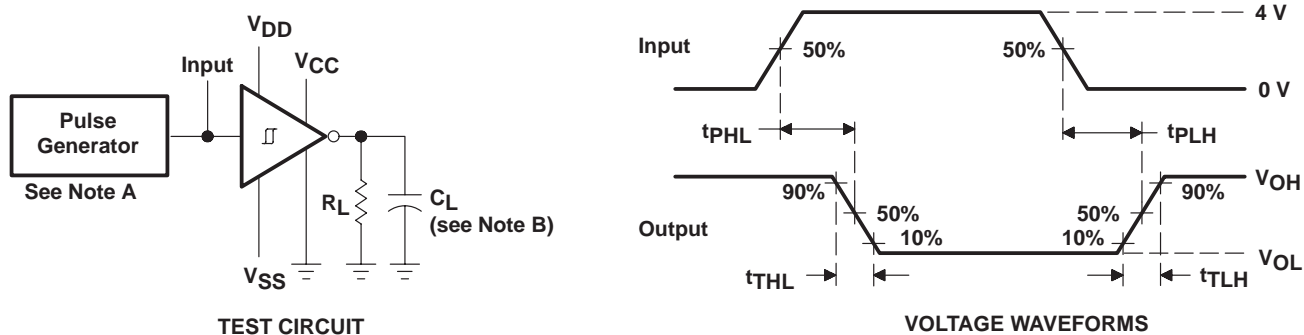


Figure 5. Receiver Test Circuit,  $V_{IT}$ ,  $V_{OL}$ ,  $V_{OH}$

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics:  $t_w = 25 \mu s$ ,  $PRR = 20 \text{ kHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = t_f < 50 \text{ ns}$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

The EIA/TIA-232-E specification is for data interchange between a host computer and a peripheral at signaling rates up to 20 kbps. Many EIA/TIA-232-E devices will operate at higher data rates with lower capacitive loads (short cables). For reliable operation at greater than 20 kbps, the designer needs to have control of both ends of the cable. By mixing different types of EIA/TIA-232-E devices and cable lengths, errors can occur at higher frequencies (above 20 kbps). When operating within the EIA/TIA-232-E requirements of less than 20 kbps and with compliant line circuits, interoperability is assured. For applications operating above 20 kbps, the design engineer should consider devices and system designs that meet the EIA/TIA-423-B requirements.

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