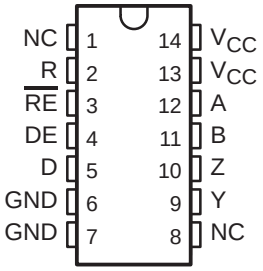
- **Meets TIA/EIA-422-B, TIA/EIA-485-A, and CCITT Recommendations V.11 and X.27**
- **Low Supply-Current Requirements 30 mA Max**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Common-Mode Output Voltage Range of –7 V to 12 V**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 60 mV Typ**
- **Receiver Common-Mode Input Voltage Range of ±12 V**
- **Operates From Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**

N OR NS† PACKAGE
(TOP VIEW)



NC – No internal connection
† The NS package is only available in left-end taped and reeled (order device SN75ALS181NSLE).

description

The SN75ALS181 is a differential driver and receiver pair designed for bidirectional data communication on multipoint bus transmission lines. The design provides for balanced transmission lines and meets TIA/EIA-422-B and TIA/EIA-485-A, and CCITT recommendations V.10, V.11, X.26, and X.27.

The SN75ALS181 combines a 3-state differential line driver and a differential-input line receiver that operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate pins for greater flexibility and are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage changes, making the device suitable for party-line applications.

The SN75ALS181 is characterized for operation from 0°C to 70°C.

Function Tables

EACH DRIVER

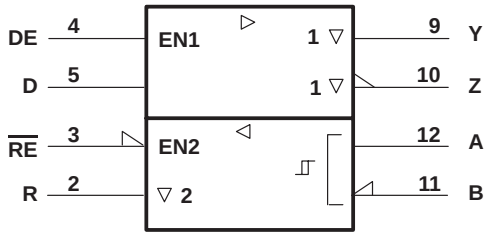
INPUT D	ENABLE DE	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL A – B	ENABLE $\overline{RE}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

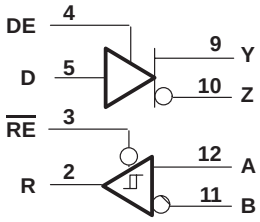
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†

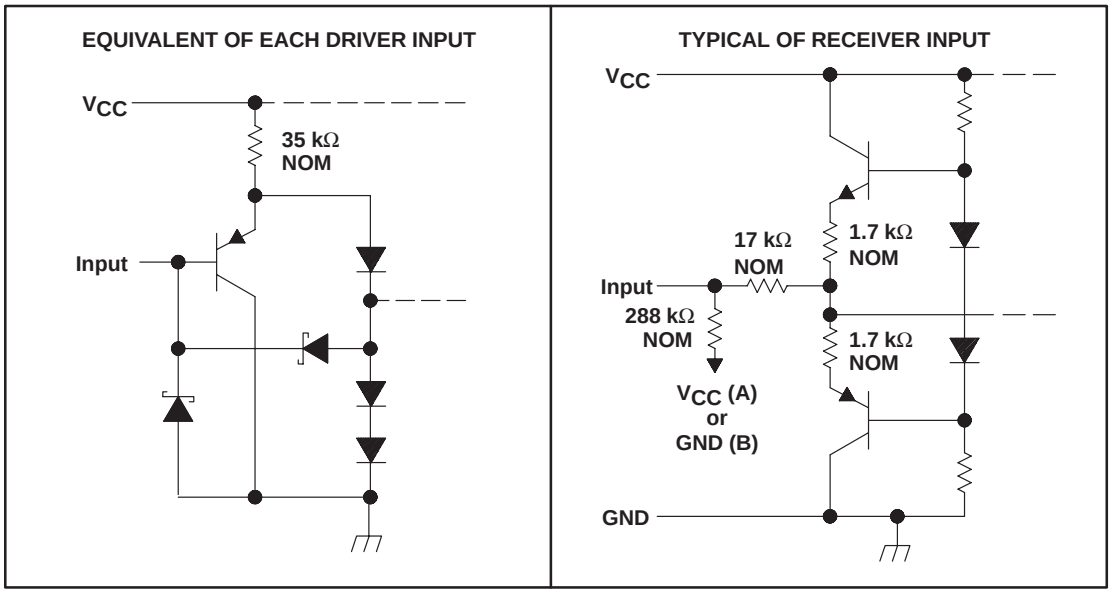


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

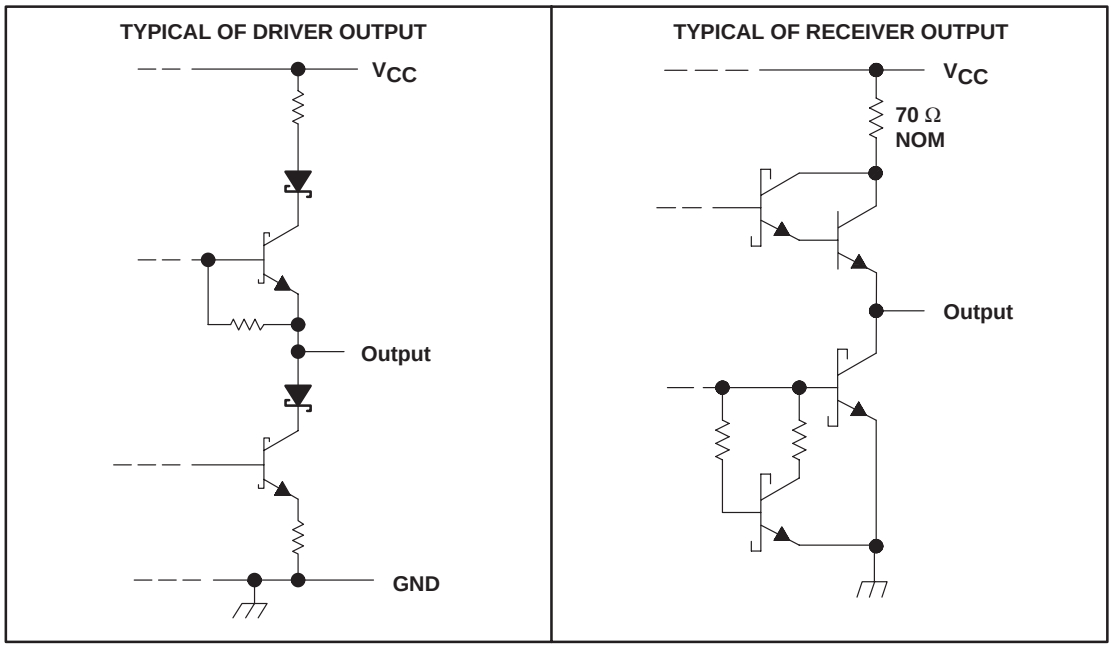
logic diagram (positive logic)



schematics of inputs



schematics of outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, DE, $\overline{RE}$, and D inputs . . . . . 7 V
Output voltage range, driver . . . . . –9 V to 14 V
Input voltage range, receiver . . . . . –14 V to 14 V
Receiver differential input voltage range (see Note 2) . . . . . –14 V to 14 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	4.0 mW/°C	445 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode output voltage, V_{OC} (see Note 3)	Driver	–7		12	V
Common-mode input voltage, V_{IC} (see Note 3)	Receiver	–12		12	V
High-level input current, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input current, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			–60	mA
	Receiver			–400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	mA
Operating free-air temperature, T_A		0		70	°C

NOTE 3: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this table for common-mode output voltage level only.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 5 V, R_L = 100 Ω	See Figure 1	1/2 V_{OD1}			V
				2			
$\|V_{OD2}\|$	Differential output voltage	R_L = 54 Ω		1.5	2.3	5	
$\|V_{OD3}\|$	Differential output voltage	V_{test} = –7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage (see Note 4)	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
						–1	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage (see Note 4)					±0.2	V
I_{OZ}	High-impedance-state output current	V_O = –7 V to 12 V,	See Note 5			±100	µA
I_{IH}	High-level input current	V_{IH} = 2.4 V				20	µA
I_{IL}	Low-level input current	V_{IL} = 0.4 V				–100	µA
I_{OS}	Short-circuit output current	V_O = –7 V				–250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				250	
		V_O = 0 V				–150	
I_{CC}	Supply current (total package)	No load	Outputs enabled		21	30	mA
			Outputs disabled		14	21	

NOTES: 4. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
5. This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{dD}	Differential output delay time, t_{dDH} or t_{dDL}	R_L = 54 Ω,	C_L = 50 pF, See Figure 3	9	13	20	ns
$t_{sk(p)}$	Pulse skew ($\|t_{dDH} - t_{dDL}\|$)				1	8	
t_t	Differential output transition time			3	10	16	
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		36	53	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		39	56	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		20	31	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		9	20	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage, differential input	V_O = 2.7 V,	I_O = –0.4 mA				0.2	V
V_{T-}	Negative-going threshold voltage, differential input	V_O = 0.5 V,	I_O = 8 mA	See Note 8	–0.2			V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)					60		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	I_I = –18 mA					–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –400 μA,	See Figure 6	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV,	I_{OL} = 8 mA,	See Figure 6			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input at 0 V, See Note 5	V_I = 12 V				1	mA
			V_I = –7 V				–0.8	
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2.7 V					20	μA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.4 V					–100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0 V		–15		–85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled			21	30	mA
			Outputs disabled			14	21	

NOTE 5: This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF (unless otherwise noted) (see Figure 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	V_{ID} = –1.5 V to 1.5 V	10	16	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –1.5 V to 1.5 V	10	16	25	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PLH} - t_{PHL} \rvert$)	V_{ID} = –1.5 V to 1.5 V		1	8	ns
t_{PZH}	Output enable time to high level			7	15	ns
t_{PZL}	Output enable time to low level			9	19	ns
t_{PHZ}	Output disable time from high level			18	27	ns
t_{PLZ}	Output disable time from low level			10	15	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

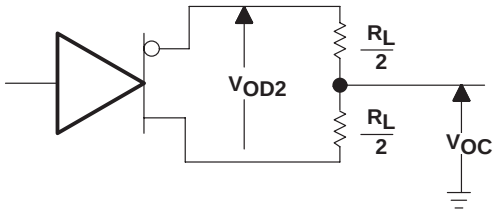


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

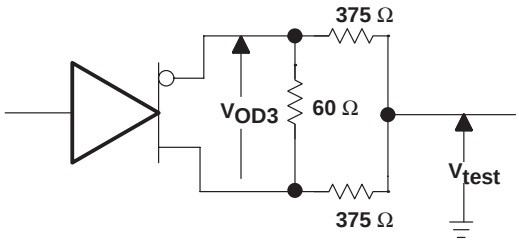
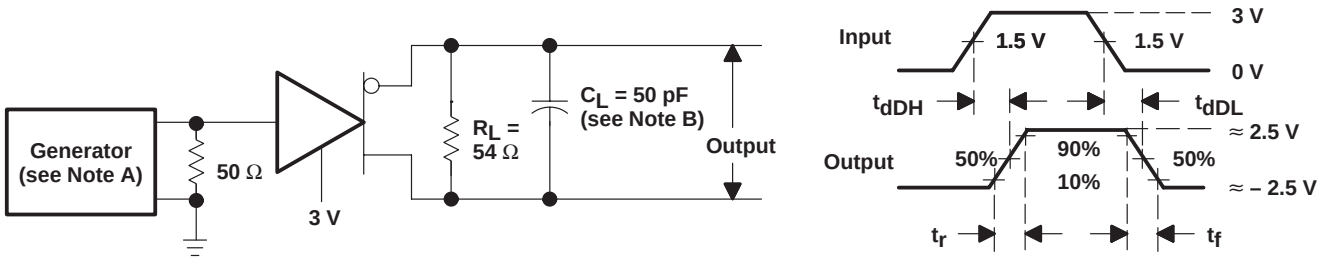


Figure 2. Driver Circuit, V_{OD3}

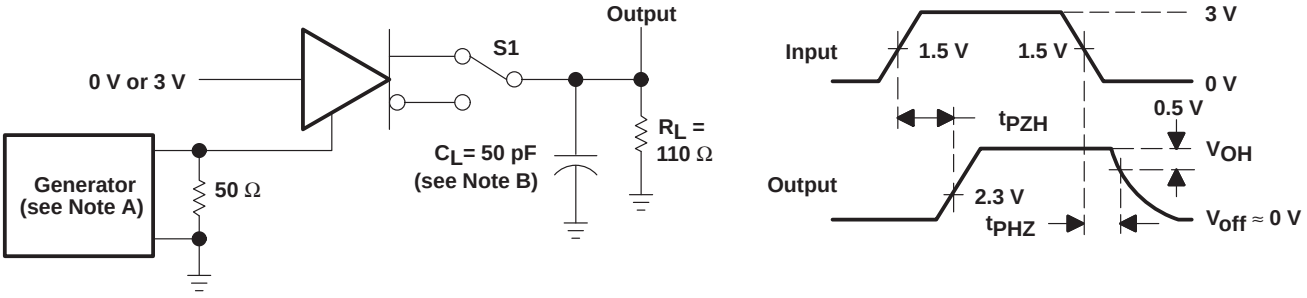


TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Differential-Output Delay and Transition Times

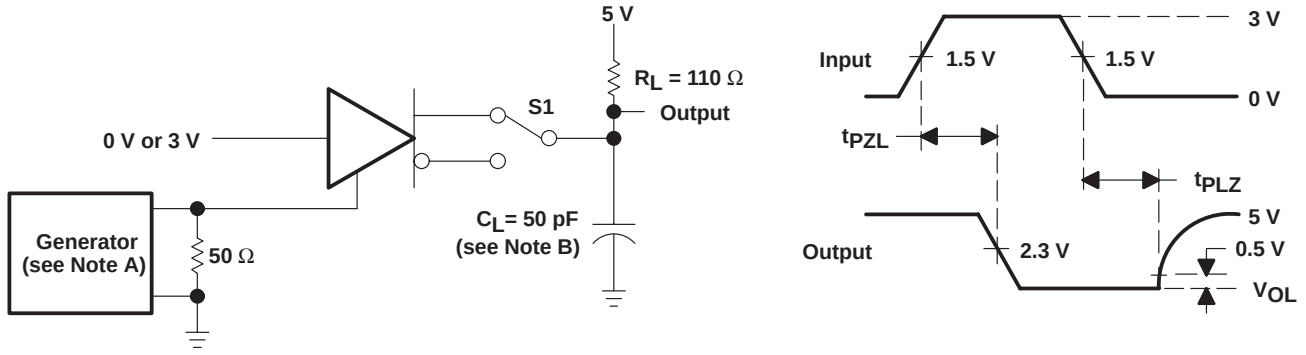
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Enable and Disable Times



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 5. Driver Enable and Disable Times

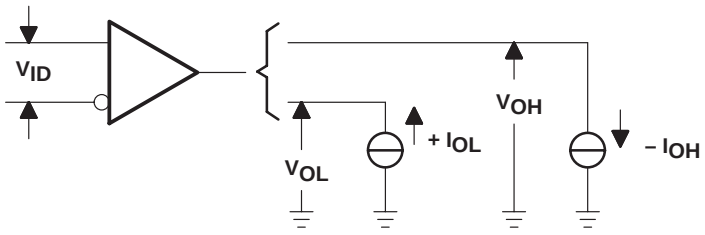
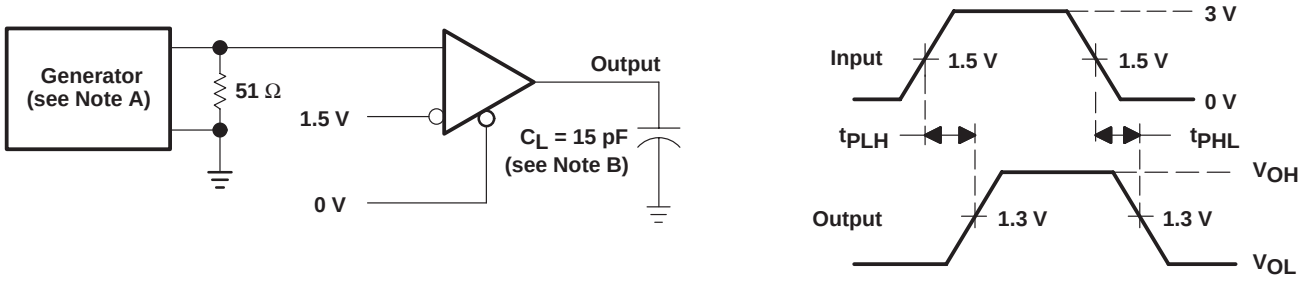


Figure 6. Receiver, V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION

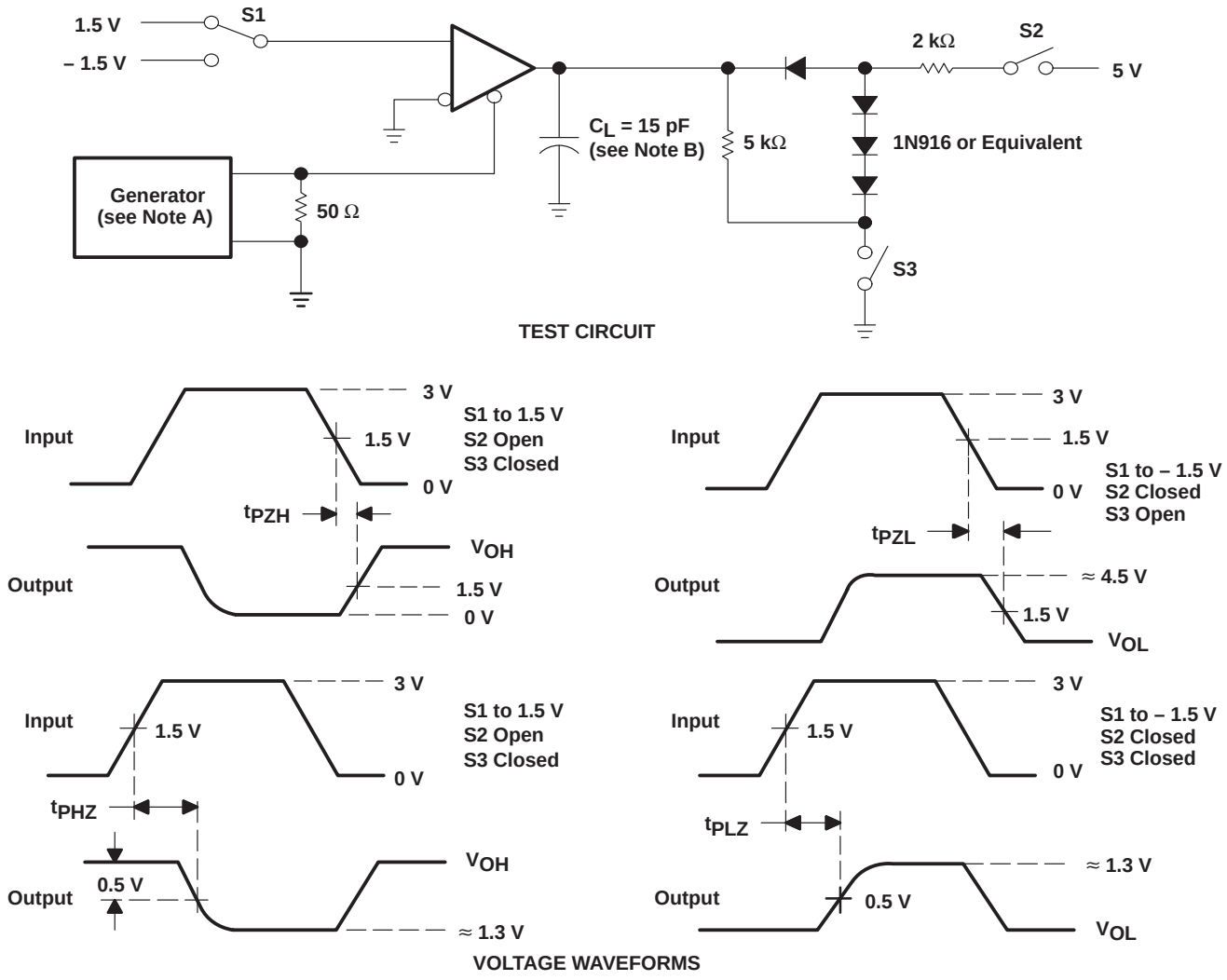


TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Propagation-Delay Times

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 8. Receiver Output Enable and Disable Times

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