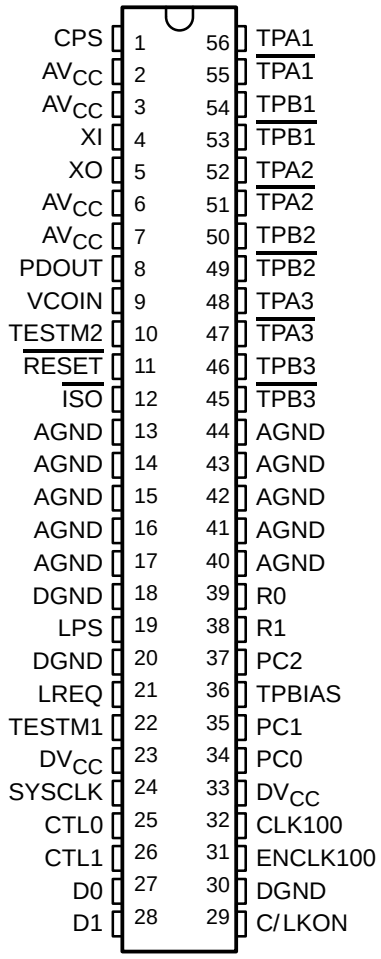
SLLS167A – MARCH 1994 – REVISED MARCH 1996

- **Supports Provisions of IEEE 1394-1995 for High-Performance Serial Bus**
- **Fully Interoperable With FireWire™ Implementation of IEEE 1394-1995**
- **Provides Three Fully Compliant Cable Ports at 100 Mbits Per Second (Mbits/s)**
- **Cable Ports Monitor Line Conditions for Active Connection to Remote Node**
- **Inactive Ports Disabled to Save Power**
- **Logic Performs System Initialization and Arbitration Functions**
- **Encode and Decode Functions Included for Data Strobe Bit Level Encoding**
- **Incoming Data Resynchronized to Local Clock**
- **Interface to Link Layer Controller Supports Optional Electrical Isolation**
- **Data Interface to Link Layer Controller Provided Through Two Parallel Lines at 50 Mbits/s**
- **25-MHz Crystal Oscillator and PLL Provide Transmit, Receive Data, and Link Layer Controller Clocks at 50 MHz**
- **Selectable Oscillator Input for External 100-MHz Reference Signal**
- **Node Power Class Information Signaling for System Power Management**
- **Cable Power Presence Monitoring**
- **Cable Bias and Driver Termination Voltage Supply**
- **Single 5-V Supply Operation**
- **Separate Multiple Package Terminals Provided for Analog and Digital Supplies and Grounds**
- **High-Performance 56-Pin SSOP (DL) Package**

DL PACKAGE
(TOP VIEW)



description

The TSB11C01 provides the analog transceiver functions needed to implement a 3-port node in a cable-based IEEE 1394-1995 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB11C01 is designed to interface with a link layer controller, such as the TSB12C01A.

description (continued)

The TSB11C01 requires either an external 24.576-MHz crystal or an external 98.304-MHz reference oscillator input. When using the crystal oscillator option, an internal phase-locked loop (PLL) generates the required 98.304-MHz reference signal. Selecting the external oscillator option turns off both the crystal oscillator and the PLL. The 98.304-MHz reference signal is internally divided to provide the 49.152-MHz ±100 ppm clock signals that control transmission of the outbound encoded strobe and data information. The 49.152-MHz clock signal is also supplied to the associated link layer controller for synchronization of the two chips and is used for resynchronization of the received data.

Data bits to be transmitted are received from the link layer controller on two parallel paths and are latched internally in the TSB11C01 in synchronization with the 49.152-MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304 Mbits/s as the outbound data strobe information stream. During transmit, the encoded data information is transmitted differentially on the TPB cable pair(s) and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception, the TPA and TPB transmitters of the receiving cable port are disabled and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data strobe information is decoded to recover the receive clock signal and the serial data bits. The serial data bits are split into two parallel streams, resynchronized to the local system clock and sent to the associated link layer controller. The received data is also transmitted (repeated) out of the other active cable ports.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. In addition, the TPB channel monitors the incoming cable common-mode voltage for the presence of the remotely supplied twisted-pair bias voltage. The presence or absence of this bias voltage is used as an indication of cable connection status.

The TSB11C01 provides a 1.86-V nominal bias voltage for driver load termination. This bias voltage, when seen through a cable by a remote receiver, senses the presence of an active connection. The value of this bias voltage has been chosen to allow interoperability between transceivers operating from either 5-V nominal supplies or 3-V nominal supplies. This bias voltage source should be stabilized by using an external filter capacitor of approximately 1 μF.

The line drivers in the TSB11C01 operate in the high-impedance current mode and are designed to work with external 112-Ω line matching resistor networks. One network is provided at each end of each twisted-pair cable. Each network is composed of a pair of series-connected 56-Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair A-package terminals is connected to the TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B-package terminals is coupled to ground through a parallel RC network with recommended values of 5 kΩ and 250 pF. The values of the external resistors are designed to meet the IEEE 1394-1995 specifications when connected in parallel with the internal receiver circuits.

The driver output current, along with other internal operating currents, is set by an external resistor. This resistor is connected between R1 and R0 and has a value of 6.36 kΩ ±0.5%.

Two terminals set up various test conditions used in manufacturing. Terminals TESTM1 and TESTM2 should be connected to V_{CC} for normal operation.

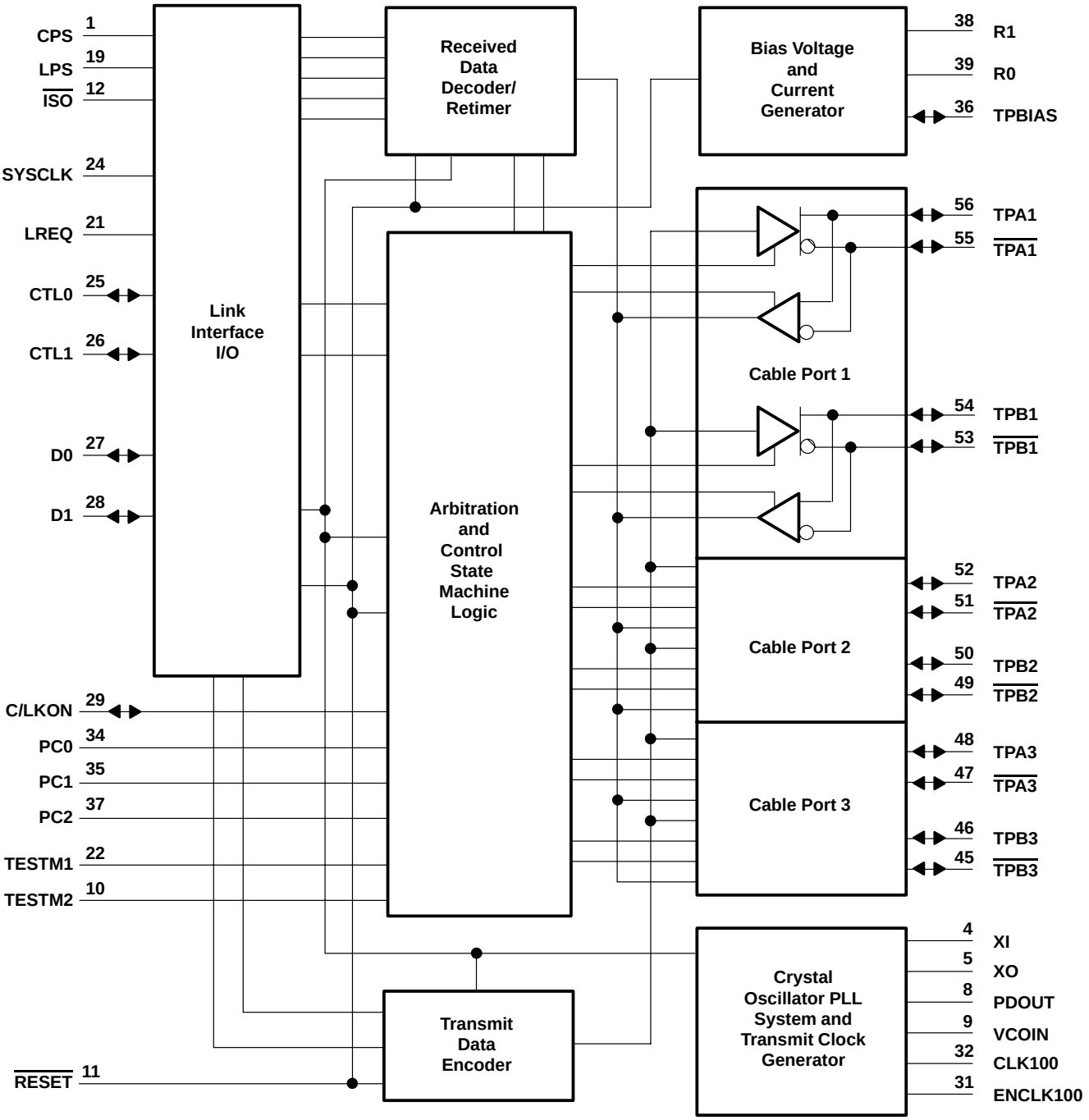
Four terminals are used as inputs to set four configuration status bits in the self identification packet. These terminals are hardwired high or low as a function of the equipment design. PC[0:2] are three terminals that indicate either the need for power from the cable or the ability to supply power to the cable. The fourth terminal, C/LKON, indicates if a node is a contender for configuration manager. C/LKON can also output a 6.114-MHz ±100 ppm signal, indicating reception of a link-on packet. See Table 4–27 of the IEEE 1394-1995 standard for additional details.

description (continued)

The TSB11C01 supports an optional isolation barrier between itself and its link layer controller. When $\overline{\text{ISO}}$ is tied high, the link interface outputs behave normally; when tied low, an internal differentiating logic is enabled and the outputs become short pulses that can be coupled through a capacitor or transformer.

The TSB11C01 is characterized for operation from 0°C to 70°C.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	13–17, 40–44		Analog circuit ground
AV_{CC}	2, 3, 6, 7		Analog circuit supply voltage
CLK100	32	I	Optional external clock input
C/LKON	29	I/O	Configuration manager contender status input or link-on output
CPS	1	I	Cable power status
CTL[0:1]	25, 26	I/O	Link interface bidirectional control signals
D[0:1]	27, 28	I/O	Link interface bidirectional data signals
DGND	18, 20, 30		Digital circuit ground
DV_{CC}	23, 33		Digital circuit supply voltage
ENCLK100	31	I	Disable crystal oscillator and PLL, enable CLK100 input
$\overline{ISO}$	12	I	Physical (phy) link interface isolation status
LPS	19	I	Link power status
LREQ	21	I	Link request from controller
PDOUT	8	O	Output from PLL phase detector, input to external filter
PC[0:2]	34, 35, 37	I	Power class bits 0 through 2 inputs
R[0:1]	38, 39		External bias current-setting resistor
$\overline{RESET}$	11	I	Reset
TESTM1, TESTM2	22, 10	I	Test mode control, normally tied high
SYSCLK	24	O	49.152-MHz clock to link controller
TPA1, TPA2, TPA3	56, 52, 48	I/O	Port n cable pair A, positive signal
$\overline{TPA1}$, $\overline{TPA2}$, $\overline{TPA3}$	55, 51, 47	I/O	Port n cable pair A, negative signal
TPB1, TPB2, TPB3	54, 50, 46	I/O	Port n cable pair B, positive signal
$\overline{TPB1}$, $\overline{TPB2}$, $\overline{TPB3}$	53, 49, 45	I/O	Port n cable pair B, negative signal
TPBIAS†	36	O	Cable termination voltage source
VCOIN	9	I	Input to VCO, output from external filter
XI, XO	4, 5	I/O	External crystal for oscillator

† The output voltage at TPBIAS (terminal 36) is approximately 50 mV below the target design value. This can cause the measured TPBIAS output voltage to fall outside the specified limits when under the worst case conditions of minimum supply voltage and maximum load current. To adjust the output voltage at TPBIAS to the specified limit, connect an external resistor of approximately 785 Ω between TPBIAS (terminal 36) and AV_{CC} (terminals 2, 3, 6, or 7). The nominal TPBIAS output voltage will be adjusted to the target design value on a future revision of this device.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 6 V
Input voltage range, V_I . . . . . 0.5 V to V_{CC} + 0.5 V
Output voltage range at any output, V_O . . . . . 0.5 V to V_{CC} + 0.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DL	2500 mW	20 mW/°C	1600 mW

‡ This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$) and uses a board mounted device rated at 50°C/W.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	CMOS inputs	0.7 V_{CC}			V
Low-level input voltage, V_{IL}	CMOS inputs			0.2 V_{CC}	V
Differential input voltage, V_{ID}	Cable inputs	142		260	mV
Common-mode input voltage, V_{IC}	Cable inputs	1.12		2.54	V
High-level output current, I_{OH}	SYSCLK			–16	mA
	CTL0, CTL1, D0, D1			–12	
Low-level output current, I_{OL}	SYSCLK			16	mA
	CTL0, CTL1, D0, D1			12	
Output current, I_O	TPBIAS	–5		2.5	mA

electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

driver

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OD}	Differential output voltage	R_L = 55 Ω	180	260	mV
I_{IC}	Common-mode input current	Driver enabled	–0.55	0.55	mA
V_{OFF}	Off-state voltage	Driver disabled		20	mV

receiver

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
I_{IC}	Common-mode input current	Driver disabled	–20	20	μA
z_{ID}	Differential input impedance		5		kΩ
				6	pF
z_{IC}	Common-mode input impedance		20		kΩ
				24	pF
	Cable bias detect threshold, TPBx inputs		0.6	1.12	V

device

PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
	Power status threshold	0.4-MΩ resistor	4.7	7.5	V
V_{OH}	High-level output voltage	I_{OH} = MAX, V_{CC} = MIN	3.7		V
V_{OL}	Low-level output voltage	I_{OL} = MIN, V_{CC} = MAX		0.5	V
	Positive arbitration comparator threshold		89	168	mV
	Negative arbitration comparator threshold		–168	–89	mV
	TPBIAS output voltage		1.71	2	V
V_{IT+}	Positive input threshold voltage, LREQ, CTL, D inputs		V_{CC}/2 + 0.2	V_{CC}/2 + 1.1	V
V_{IT-}	Negative input threshold voltage, LREQ, CTL, D inputs		V_{CC}/2 – 1.1	V_{CC}/2 + 0.2	V
I_{CC}	Supply current	V_{CC} = 5.25 V		140	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
	Transmit jitter			±0.8	ns
t_r	Transmit rise time	C_L = 10 pF, R_L = 55 Ω		3	ns
t_f	Transmit fall time			3	ns
t_{su}	Setup time, D, CTL, LREQ low or high before SYSCLK↑		5		ns
t_h	Hold time, D, CTL, LREQ low or high after SYSCLK↑		0		ns
t_d	Delay time, SYSCLK to D, CTL		5	13	ns

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, No air flow		50		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			12		°C/W

PARAMETER MEASUREMENT INFORMATION

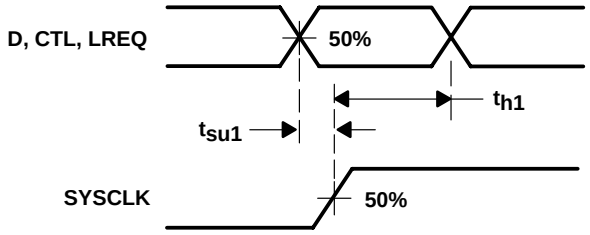


Figure 1. D, CTL Output Delay Relative to SYSCLK Waveforms

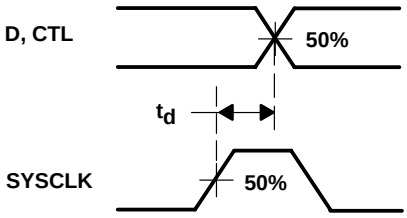


Figure 2. D, CTL, LREQ Input Setup and Hold Time Waveforms

APPLICATION INFORMATION

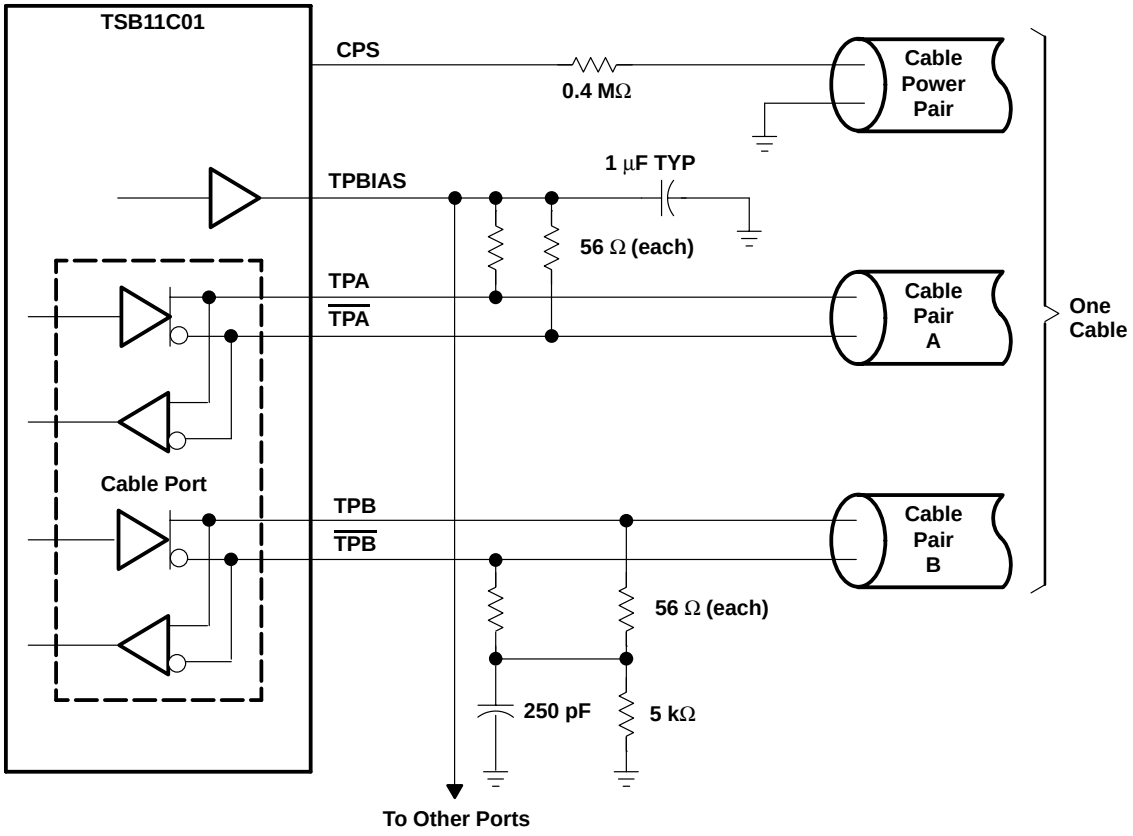


Figure 3. Twisted-Pair Cable Interface Connections

internal register configuration

The accessible internal registers of this device are listed in Table 1 and the description of the fields are listed in Table 2.

Table 1. Accessible Internal Registers

ADDRESS	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	GC					
0010	SPD		Reserved		NP			
0011	AStat1		BStat1		Ch1	Con1	Reserved	
0100	AStat2		BStat2		Ch2	Con2	Reserved	
0101	AStat3		BStat3		Ch3	Con3	Reserved	
0110	Reserved							
0111	Reserved							

APPLICATION INFORMATION

internal register configuration (continued)

Table 2. Internal Register Field Descriptions

FIELD	SIZE (Bits)	TYPE	DESCRIPTION
AStat(n)	2	Rd	These bits give the line state of TPA of port n. 11 = Z 01 = 1 10 = 0 00 = invalid
BStat(n)	2	Rd	These bits give the line state of TPB of port n, the encoding is the same as AStat(n).
Ch(n)	1	Rd	When Ch(n) = 1, then port n is a child; otherwise, it is a parent.
Con(n)	2	Rd	When Con(n) = 1, then port n is connected; otherwise it is disconnected.
CPS	1	Rd	This bit is the cable power status for the CPS terminal.
IBR	1	Rd/Wr	This bit initiates bus reset at next opportunity.
GC	6	Rd/ Wr	These bits are the gap count may be changed by the serial bus manager to optimize performance. See the IEEE 1394-1995 standard for details.
NP	4	Rd	These bits are the number of ports on this TSB11C01 and are always set to 0011.
Physical ID	6	Rd	These bits contain the address of the local node determined during self identification.
R	1	Rd	This bit indicates that the local node is the root.
RHB	1	Rd/ Wr	This is the root hold-off bit that instructs the local node to try to become the root during the next bus reset.
SPD	2	Rd	These bits indicate the top signalling speed of this TSB11C01 and is always cleared.

external components and connections

Cable power status (CPS): This terminal is normally connected to the cable power through a 0.4-MΩ resistor. This circuit feeds an internal comparator, which detects the presence of cable power. This information is available to the link layer controller.

Oscillator crystal (XI and XO): These terminals are usually connected to an external 24.576-MHz parallel-resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the specifications of the external crystal used and on circuit board layout.

PLL/VCO filter (PDOUT and VCOIN): These terminals are for an external lag-lead filter required for stable operation of the frequency multiplier running off the crystal oscillator.

Test mode control inputs (TESTM1 and TESTM2): These terminals are used in manufacturing to enable production line testing of the TSB11C01. For normal use, these should be tied to V_{CC}.

Logic reset input ($\overline{\text{RESET}}$): When forced low, this terminal causes a bus reset condition on the active cable ports and resets the internal logic to the reset/start state. An internal pullup resistor is provided that is connected to V_{CC}, so only an external delay capacitor is required. This input is a standard logic buffer and may also be driven by a logic buffer.

Link power status input (LPS): A 10-kΩ resistor connected to V_{CC} supplying the link layer controller to monitor the link power status. When the link is not powered on, SYSCLK is disabled and the TSB11C01 performs only the basic repeater functions required for network initialization and operation.

Link request input (LREQ): An input from the link layer controller that is used by the link to signal the TSB11C01 of a request to perform some service

System clock output (SYSCLK): This terminal provides a 49.152-MHz clock signal to which the data, control, and link request information is synchronized.

APPLICATION INFORMATION

external components and connections (continued)

Control I/Os (CTL[0:1]): These terminals are bidirectional signals communicated between the TSB11C01 and the link layer controller that control passage of information between the two devices

Data I/Os (D0 and D1): These terminals are bidirectional information signals communicated between the TSB11C01 and the link layer controller

Power class bits 0 through 2 inputs (PC[0:2]): These terminals are used as inputs to set the bit values of the three power class bits in the self-ID packet. They may be programmed by tying the terminals high to V_{CC} or low to GND.

Enable external clock input (ENCLK100): This terminal is a logic input that allows a choice between using the internal crystal oscillator and PLL frequency multiplier or an external 98.304-MHz signal source. When tied high, the internal crystal oscillator and the PLL are disabled and the external clock input can be used.

External clock input (CLK100): When this terminal is asserted high (enabled), an external 98.304-MHz oscillator can drive the TSB11C01. Input voltages as low as 0.2 V peak-to-peak may be used, and the input should be ac coupled through a capacitor of 300 pF or greater. When the crystal oscillator and PLL are being used, it is recommended that this terminal be tied to GND.

Twisted-pair cable bias-voltage output (TPBIAS): This terminal provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and for signalling to the remote nodes that there is a valid cable connection.

Configuration manager contender input or link-on output (C/LKON): C/LKON is a bidirectional terminal that is used as an input to specify in the self-ID packet that the node is a configuration manager contender. As an output, it signals the reception of a link-on message by supplying a 6.114-MHz signal. The bit-value programming is done by tying the terminal through a 10-kΩ resistor high (V_{CC}) or low (GND). The use of the series resistor allows the link-on output to override the input value when necessary.

Current setting resistor (R[0:1]): An internal reference voltage is applied across the resistor connected between these two terminals to set the internal operating currents and the cable driver output currents. A low temperature-coefficient (TC) resistor should be used to meet the IEEE 1394-1995 output voltage limits.

Supply filters (AV_{CC} and DV_{CC}): A combination of high-frequency decoupling capacitors is suggested for these terminals, such as paralleled 0.1 μF and 0.001 μF. These supply lines are separated on the device to provide noise isolation. They should be tied together at a low-impedance point on the circuit board. Individual filter networks are desirable.

APPLICATION INFORMATION

external components and connections (continued)

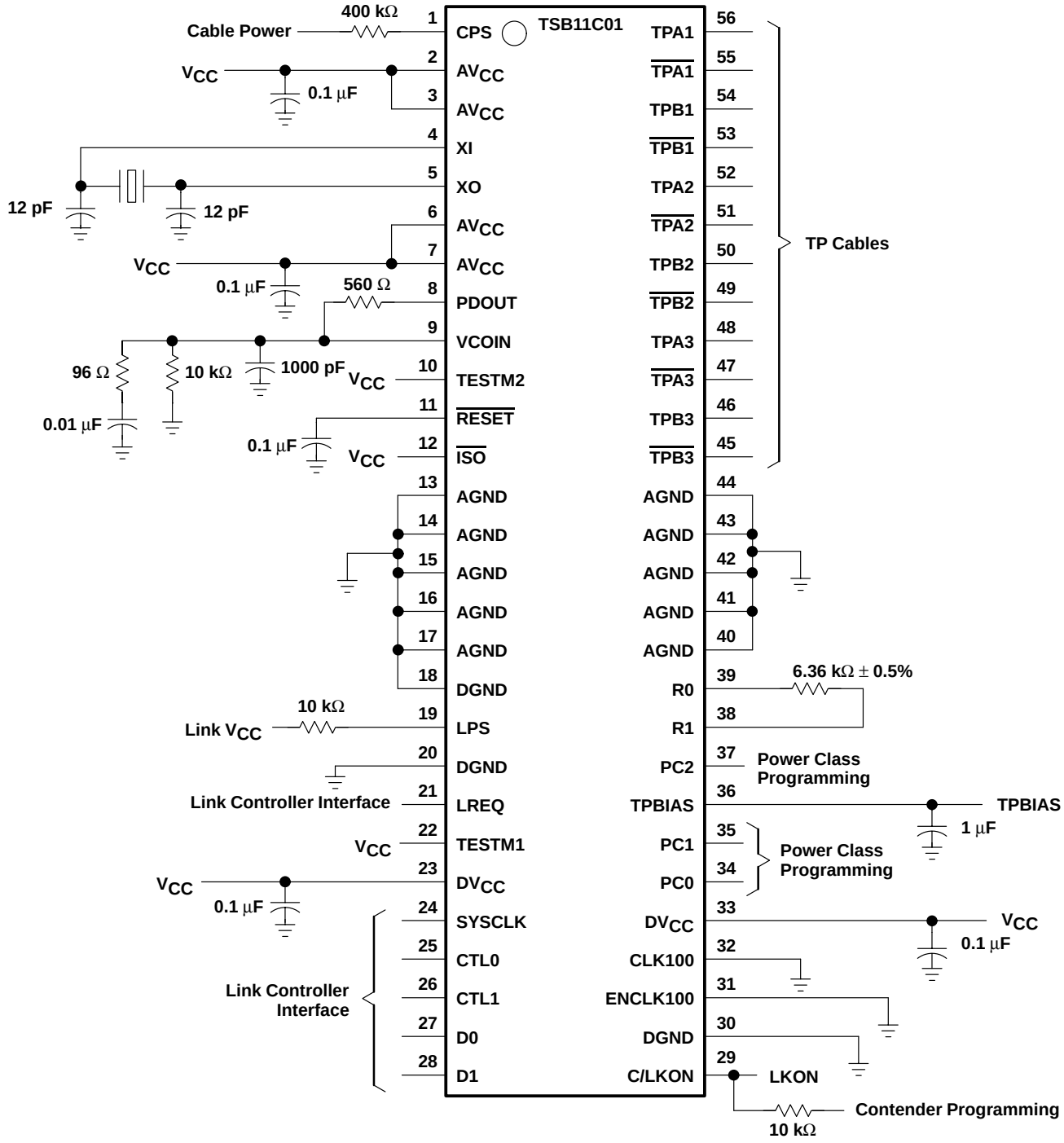


Figure 4. External Component Hookup Circuit

PRINCIPLES OF OPERATION

external components and connections (continued)

The TSB11C01 is designed to operate with a link layer controller such as the Texas Instruments TSB12C01A. These devices use an interface described in annex I of the IEEE 1394-1995 standard. Details of how the TSB12C01A devices operate are described in the TSB12C01A data manual (literature number SLLS219). The following describes the operation of the physical (phy) link interface.

The TSB11C01 supports 100 Mbits/s data transfers and has two bidirectional data lines D[0:1] crossing the interface. In addition, there are two bidirectional control lines CTL[0:1], the 50-MHz SYSCLK line from the TSB11C01 to the link, and the link request line (LREQ) from the link to the TSB11C01. The TSB11C01 has control of all the bidirectional terminals. The link is allowed to drive these terminals only after it has been given permission by the TSB11C01. The dedicated LREQ request terminal is used by the link for any activity it wishes to initiate.

There are four operations that may occur in the phy link interface: request, status, transmit, and receive. With the exception of the request operation, all actions are initiated by the TSB11C01.

When the TSB11C01 has control of the bus the CTL[0:1] lines are encoded as shown in Table 3.

Table 3. TSB11C01 Control of Bus Functions

CTL [0:1]	NAME	DESCRIPTION OF ACTIVITY
00	Idle	No activity is occurring (this is the default mode).
01	Status	Status information is being sent from the TSB11C01 to the link
10	Receive	An incoming packet is being sent from the TSB11C01 to the link
11	Transmit	The link has been given control of the bus to send an outgoing packet.

When the link has control of the bus (TSB11C01 permission) the CTL[0:1] lines are encoded as shown in Table 4.

Table 4. Link Control of Bus Functions

CTL [0:1]	NAME	DESCRIPTION OF ACTIVITY
00	Idle	The link has released the bus (transmission has been completed).
01	Hold	The link is holding the bus prior to sending a packet.
10	Transmit	An outgoing packet is being sent from the link to the TSB11C01.
11	Reserved	None

When the link wishes to request the bus or access a register that is located in the TSB11C01, a serial stream of information is sent across the LREQ line. The length of the stream varies depending on whether the transfer is a bus request, a read command, or a write command (see Table 5). Regardless of the type of transfer, a start bit of 1 is required at the beginning of the stream and a stop bit of 0 is required at the end of the stream. Bit 0 is the most significant and is transmitted first.

Table 5. Link Request Functions

NO. of BITS	REQUEST TYPE
7	Bus Request
9	Read Register Request
17	Write Register Request

PRINCIPLES OF OPERATION

external components and connections (continued)

For a bus request, the length of the LREQ data stream is 7 bits, as shown in Table 6.

Table 6. Bus Request Functions

BIT(S)	NAME	DESCRIPTION
0	Start Bit	This bit indicates the beginning of the transfer (always a 1).
1–3	Request Type	This bit indicates the type of bus request (see Table 7 for the encoding of this field).
4–5	Request Speed	These bits should always be 00 for the TSB11C01 100-Mbits/s speed.
6	Stop Bit	This bit indicates the end of the transfer (always a 0).

For a read register request, the length of the LREQ data stream is 9 bits, as shown in Table 7.

Table 7. Read Register Request Functions

BIT(S)	NAME	DESCRIPTION
0	Start Bit	This bit indicates the beginning of the transfer (always a 1).
1–3	Request Type	These bits are always a 100 indicating that this is a read register request.
4–7	Address	These bits contain the address of the TSB11C01 register to be read.
8	Stop Bit	This bit indicates the end of the transfer (always a 0).

For a write register request, the length of the LREQ data stream is 17 bits, as shown in Table 8 and LREQ timing is shown in Figure 5.

Table 8. Write Register Request Functions

BIT(S)	NAME	DESCRIPTION
0	Start Bit	This bit indicates the beginning of the transfer (always a 1).
1–3	Request Type	These bits are always a 101 indicating that this is a write register request.
4–7	Address	These bits conatin the address of the TSB11C01 register to be written to.
8–15	Data	These bits contain the data that is to be written to the specified register address.
16	Stop Bit	This bit indicates the end of the transfer (always a 0).

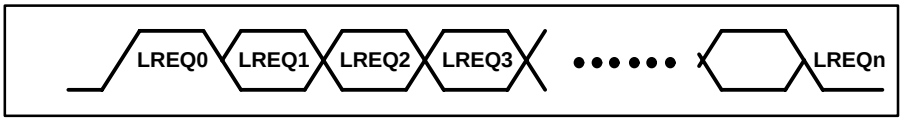


Figure 5. LREQ Timing (Each Cell Represents One Clock-Sample Time)

PRINCIPLES OF OPERATION

external components and connections (continued)

The 3-bit request-type field has the following possible values as shown in Table 9.

Table 9. Request Functions

LREQ[1:3]	NAME	DESCRIPTION
000	TakeBus	Immediate request. Upon detection of an idle, take control of the bus immediately (no arbitration).
001	IsoReq	Isochronous request. Arbitrate after an isochronous gap.
010	PriReq	Priority request. Arbitrate after a fair gap, ignore fair protocol.
011	FairReq	Fair request. Arbitrate after a fair gap; use fair protocol.
100	RdReg	Return the specified register contents through a status transfer.
101	WrReg	Write to the specified register.
110, 111	Reserved	Reserved

bus request

For fair or priority access, the link requests control of the bus at least one clock after the phy link interface becomes idle. When the link senses that the CTL terminals are in a receive state (CTL[0:1] = 10), it knows that the request has been lost. This is true any time during or after the link sends the bus request transfer. The TSB11C01 ignores any fair or priority requests when it asserts the receive state while the link is requesting the bus. The link then reissues the request one clock after the next interface idle.

The cycle master uses a normal priority request to send a cycle start message. After receiving a cycle start, the link can issue an isochronous bus request. When arbitration is won, the link proceeds with the isochronous transfer of data. The isochronous request is cleared in the TSB11C01 once the link sends another type of request or when the isochronous transfer has been completed.

The TakeBus request is issued when the link needs to send an acknowledgment after reception of a packet addressed to it. This request must be issued during packet reception. This is done to minimize the delays that the TSB11C01 has to wait between the end of a packet and the transmittal of an acknowledgment. As soon as the packet ends, the TSB11C01 immediately grants access of the bus to the link. The link sends an acknowledgment to the sender unless the header cycle redundancy check (CRC) of the packet is bad. In this case, the link releases the bus immediately; it is not be allowed to send another type of packet on this grant. To ensure this, the link is forced to wait 160 ns after the end of the packet is received. The TSB11C01 then gains control of the bus and the acknowledgment indicating the CRC error is sent. The bus is released and allowed to proceed with another request.

It is conceivable that two separate nodes might believe that an incoming packet is intended for them. The nodes then issue a TakeBus request before checking the CRC of the packet. Since both nodes seize control of the bus at the same time, a temporary localized collision of the bus occurs somewhere between the competing nodes. This collision would be interpreted by the other nodes on the network as being a ZZ line state, not a bus reset. As soon as the two nodes check the CRC, the mistaken node drops its request and the false line state is removed. The only side effect is the loss of the intended acknowledgment packet (this is handled by the higher layer protocol).

PRINCIPLES OF OPERATION

read/write requests

When the link requests to read the specified register contents, the TSB11C01 sends the contents of the register to the link through a status transfer. If an incoming packet is received while the TSB11C01 is transferring status information to the link, the TSB11C01 continues to attempt to transfer the contents of the register until it is successful.

For write requests, the TSB11C01 loads the data field into the appropriately addressed register as soon as the transfer has been completed. The link is allowed to request read or write operations at any time.

A status transfer is initiated by the TSB11C01 when it has some status information to transfer to the link. The transfer is initiated by asserting CTL[0:1] = 01 and D[0:1] = 00 (100 Mbits/s only). The D[0:1] = 00 represents the speed at which the status transfer is to occur; status information at 100 Mbits/s is always transmitted two bits at a time.

The status transfer can be interrupted by an incoming packet from another node. When this occurs, the TSB11C01 attempts to resend the status information after the packet has been acted upon. The TSB11C01 continues to attempt to complete the transfer until the information has been successfully transmitted.

NOTE

There must be at least one idle cycle between consecutive status transfers. The definition of the bits in the status transfer is shown in Table 10.

status request

Length of stream: 4 or 16 bits

Table 10. Status Request Functions

BIT(s)	NAME	DESCRIPTION
0	Arbitration Reset Gap	This bit indicates that the TSB11C01 has detected that the bus has been idle for an arbitration reset gap time (this time is defined in the IEEE 1394-1995 standard). This bit is used by the link in its busy/retry state machine.
1	Subaction Gap	This bit indicates that the TSB11C01 has detected that the bus has been idle for a subaction gap time (this time is defined in the IEEE 1394-1995 standard). This bit is used by the link to detect the completion of an isochronous cycle.
2	Bus Reset	This bit indicates that the TSB11C01 has entered the bus reset state
3	State Time Out	The TSB11C01 has stayed in a particular state for too long.
4–7	Address	These bits hold the address of the TSB11C01 register whose contents are transferred to the link.
8–15	Data	The data that is to be sent to the link

Normally, the TSB11C01 sends just the first 4 bits of status data to the link. These bits are used by the link state machines; however, when the link has initiated a read register request the TSB11C01 sends the full status packet to the link (see Figure 6). The TSB11C01 also sends a full status packet to the link if it has some important information to pass on to the link. Currently, the only condition where this occurs is after the self identification process when the TSB11C01 needs to inform the link of its new node address (physical ID register).

PRINCIPLES OF OPERATION

status request (continued)

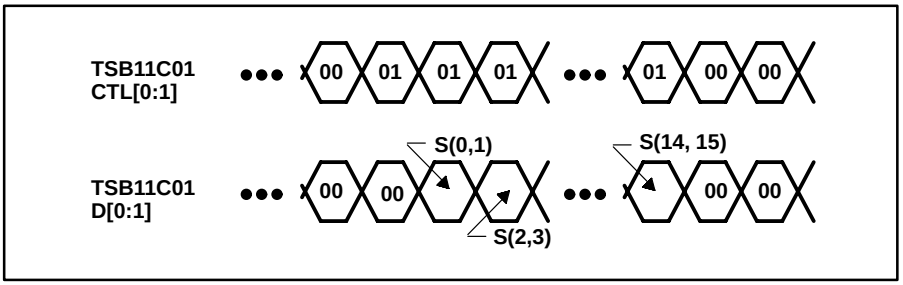


Figure 6. Status Transfer Timing

There may be times where the TSB11C01 wants to start a second status transfer. The TSB11C01 waits at least one clock cycle with the CTL lines idle before it begins a second transfer.

transmit

When the link wants to transmit information, it first requests access to the bus through the LREQ line. When the TSB11C01 receives this request, it arbitrates to gain control of the bus. When the TSB11C01 wins ownership of the bus, it grants the bus to the link by asserting the transmit state on the CTL terminals for at least one SYSCLK cycle. The link takes control of the bus by asserting either hold or transmit on the CTL lines. Hold is used by the link to keep control of the bus if it needs more time to prepare the data for transmission. The TSB11C01 keeps control of the bus for the link by asserting a data-on state on the bus. It is not necessary for the link to use hold when it is ready to transmit as soon as bus ownership is granted.

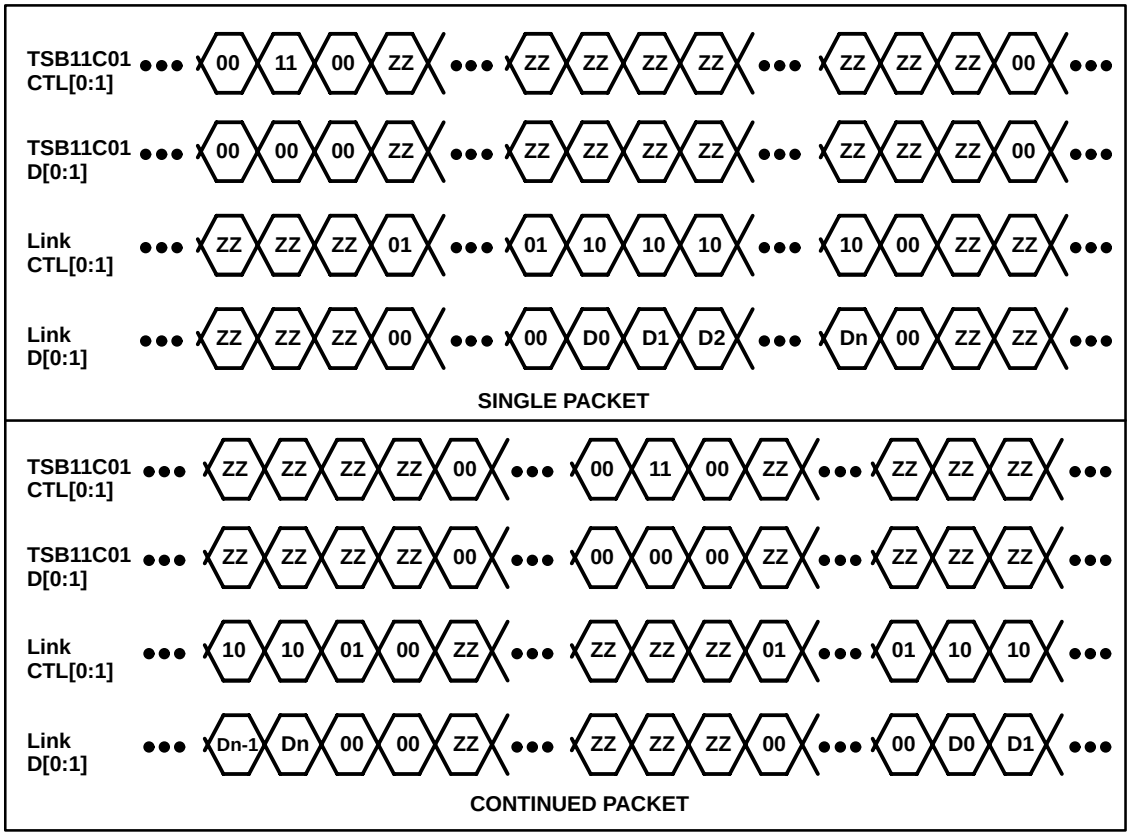
When the link is prepared to send data, it asserts transmit on the CTL lines as well as sending the first bits of the packet on the D[0:1] lines. The transmit state is held on the CTL terminals until the last bits of data have been sent. The link then asserts idle on the CTL lines for one clock cycle, after which it releases control of the interface.

There are times when the link needs to send another packet without releasing the bus. For example, the link may want to send consecutive isochronous packets or it may want to attach a response to an acknowledgment. To do this, the link asserts hold instead of idle when the first packet of data has been completely transmitted. Hold, in this case, informs the TSB11C01 that the link needs to send another packet without releasing control of the bus. The TSB11C01 waits a set amount of time before asserting transmit, and the link can then proceed with the transmission of the second packet. After all data has been transmitted and the link has asserted idle on the CTL lines, the TSB11C01 asserts its own idle state on the CTL lines. When sending multiple packets in this fashion, all data must be transmitted at the same speed. This is because the transmission speed is set during arbitration, and since the arbitration step is skipped, there is no way of informing the network of a change in speed.

PRINCIPLES OF OPERATION

transmit timing

Transmit timing is shown in Figure 7.



ZZ = high-impedance state D0 – Dn = packet data

Figure 7. Transmit Timing

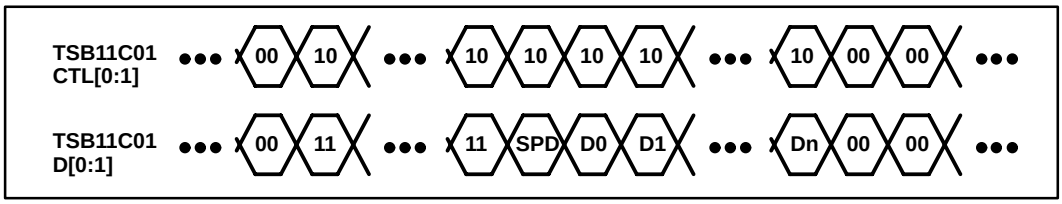
receive operation

When data is received by the TSB11C01 from the serial bus, it transfers the data to the link for further processing. The TSB11C01 asserts receive (10) on the CTL lines and 11 on the D lines. The TSB11C01 indicates the start of the packet by placing the speed code on the data bus. The TSB11C01 then proceeds with the transmission of the packet to the link on the D lines while keeping the receive status on the CTL lines. Once the packet has been completely transferred, the TSB11C01 asserts idle on the CTL lines to complete the receive operation. The speed code is a phy link protocol and not included in the CRC.

PRINCIPLES OF OPERATION

receive timing

The receive timing is shown in Figure 8.



SPD = speed code D0 – Dn = packet data

Figure 8. Receive Timing

The speed code for the receiver is shown in Table 11.

Table 11. Receiver Speed Code

D[0:1]	DATA RATE
00	100 Mbits/s

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