ERRATA TO THE TSB11C01 DATA SHEET

(TEXAS INSTRUMENTS LITERATURE NO. SLLS167A, MARCH 1996)

This document contains corrections and additions to information in the TSB11C01 data sheet (TI Literature Number SLLS167A, March 1996), also included in *IEEE 1394 Circuits Data Book*, 1997 (TI Literature Number SLLD004).

General

a. The output voltage at TPBIAS (terminal 36) is approximately 50 mV below the target design value. This can cause the measured TPBIAS output voltage to fall outside the specified limits when operated under the worst-case conditions of minimum supply voltage and maximum load current.

   – To adjust the output voltage of TPBIAS to the specified limit, connect an external resistor of approximately 685 Ω between TPBIAS (terminal 36) and AV_{CC} (terminals 2, 3, 6, or 7).

   The nominal TPBIAS output voltage will be adjusted to the target design value on a future revision of this device.

b. The TPBIAS output voltage limits have been changed to match the limits of the IEEE 1394-1995 standard. TPBIAS minimum is 1.665 V and maximum is 2.015 V.

c. To ensure reliable operation when this device is the root node and is connected to a link layer controller that is the cycle master, the application must wait for a cycle-done interrupt (CyDne, bit 22 of the Interrupt register of the link layer controller [TSB12C01A]) before making a TSB11C01 register access. The register access must be completed before the next cycle start interrupt (CySt, bit 21 of the Interrupt register of the link layer controller [TSB12C01A]).

d. An interrupt status packet is not sent to the link layer controller for cable power failure. The cable power status must be polled occasionally.

e. A write to the phy layer control register 1 from the link layer controller causes the register to remain in a write-enabled state. The phy layer logic does not automatically unaddress the write operation to control register 1. A subsequent phy configuration packet would be unable to change the gap count unless control register 1 write-enable logic is unaddressed first. This can be done from the link layer controller by either reading control register 1 or performing a read or write access to any of the other registers in the phy layer.

f. Electrical isolation as described in Appendix J of IEEE 1394–1995 is not the currently recommended by TI and the TSB11C01 is not tested to a level that would be required to implement the isolation in Appendix J of the standard. TI has an improved isolation technique that is the recommended isolation solution.

   – Please see *Galvanic Isolation of the IEEE 1394–1995 Serial Bus* (TI Literature Number SLLA011).

g. Current design of TI phy layers has the gap times set to:

– subaction–gap = ((gap_count × 16)+state_machine_delay) × BASE_RATE_PERIOD

– arb–reset–gap = ((gap_count × 32)+state_machine_delay) × BASE_RATE_PERIOD

where the BASE_RATE_PERIOD is 10ns, and the state_machine_delay is approximately (8×BASE_RATE_PERIOD). This varies from the standard in that the state_machine_delay does not match the spec values of 28 and 52 for the respective gaps.

All phy layers also have a hysteresis time (arb delay time) built in, which is set to:

– delay–time = ((gap_count × 4)+state_machine_delay) × BASE_RATE_PERIOD

After a subaction–gap or arb–reset–gap has been detected, the phy will send the appropriate status to the link. It will then wait for the delay-time period, and then service any bus requests made by the link.

– See section 8.4.6.2 of IEEE 1394–1995 for minimum acceptable gap counts.

h. All TI phy cores can receive phy configuration packets that will update their gap count. The TSB11C01 will not update it's own gap count when sending a phy configuration packet. There is the potential for a bus hang in the system due to an inherent problem in the IEEE 1394–1995 standard. A provision in the standard requires the phy to see two bus resets without an intermediate write to the gap count register before the phy will reset it's gap count to the default 3F. This results in the possibility of nodes having different gap counts after power up or a bus reset. Different gap counts can cause the system to hang if a node with a short gap count senses that self_ID is over and starts sending out packets before another node with a longer gap count exits the self_ID phase.

It is ***very important*** that all nodes wait until they receive a phy configuration packet after a bus reset before sending any packets. If an TSB11C01 node is the *bus manager:*

1. It should first wait at least 10 μs to allow nodes with their gap count set to 3F to exit the self_ID phase.
2. Next, the node should set it's local gap count with a Link/PHY write and then immediately send a phy configuration packet to set the gap counts in all other nodes in the network.

This must be the first packet transmission after self–ID.

3. All other nodes in the system ***must*** wait until they see a phy configuration packet before they start any packet transmissions after a bus reset.

i. The TSB11C01 should not be connected directly to a low-voltage (3.3 V nominal) link layer controller. The TSB11C01 does not have TTL thresholds; it has thresholds centered to accommodate IEEE 1394–1995 suggested isolation. This results in a combination of phy and link thresholds for a low voltage link device that does not guarantee interoperability.

j. The received data prefix (data prefix time + speed signal length) for the TSB11C01 has a minimum time of 180 ns. If the node transmitting to the TSB11C01 does not provide 180 ns of data prefix, the first few bits of the packet may be missed. The remainder of the packet will be transferred to the link where it will fail the CRC checks and be ignored. If the node is repeating data, only that portion of the packet recognized (after the missed bits) will be repeated. All Texas Instruments physical layers provide at least 180 ns of data prefix.

h. The digital core in the TSB11C01 PHY may not always correctly process back-to-back packets that are spaced too closely together. For the packets to be processed correctly, the total of the idle time following the data end of the first packet, the arbitration time for the second packet, and the data prefix time of the second packet must be approximately 450 ns or greater.

A symptom of this problem is when a node communicating with the TSB11C01 sends two packets to the TSB11C01 too quickly and the initial bits of the second packet are not received. This causes a header CRC error and the packet to be discarded. An example of this case is when a node is root (so it sources the cycle start packets), and the same node is also sending isochronous packets to an TSB11C01 node. Since the root does not need to arbitrate for the bus, it will transmit the isochronous packet with a minimal idle time after the cycle start packet. This is an example of *back-to-back* packets that may not be processed properly.

Workaround:

A workaround to this problem for combinations of links and PHYs that have a turn-around time that is too short is to make the node that has the TSB11C01 the root. This will ensure that every node transmitting to the TSB11C01 must first arbitrate to send a packet. The arbitration time has been shown in the TI lab using TI PHYs to be enough extra time to keep the problem from occurring. Note that the only requirement is that the node sending the isochronous data to the TSB11C01 must not be root. One method of ensuring this is to make the TSB11C01 the root, and can be accomplished using a PHY configuration packet.

TSB11C01 document changes

aa. The last paragraph on page 2 of the data sheet (page 6–4 of the *IEEE 1394 Circuits Data Book*, 1997) states that C/LKON outputs a 6.114 MHz signal. The correct value is exactly 1/16 of the oscillator frequency or

$$(98.304\ \text{MHz} \pm 100\ \text{ppm}) \div 16 = 6.144\ \text{MHz} \pm 100\ \text{ppm}$$

bb. The following changes should be made to the switching characteristics table on page 7 of the data sheet (page 6–9 of the *IEEE 1394 Circuits Data Book*, 1997):

switching characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_h	Hold time, D, CTL, LREQ low or high ***before*** SYSCLK↑		2		ns
t_d	Delay time, SYSCLK to D, CTL		2	11	ns

cc. On page 7 of the data sheet (page 6–9 of the *IEEE 1394 Circuits Data Book*, 1997), the titles of Figures 1 and 2 should be reversed to read as follows:

Figure 1. D, CTL, LREQ Input Setup and Hold Time Waveforms

Figure 2. D, CTL Output Delay Relative to SYSCLK Waveforms

dd. Replace the transfer timing diagram in Figure 6 (page 16 of the data sheet, page 6–18 of the *IEEE 1394 Circuits Data Book*, 1997) with the following diagram:

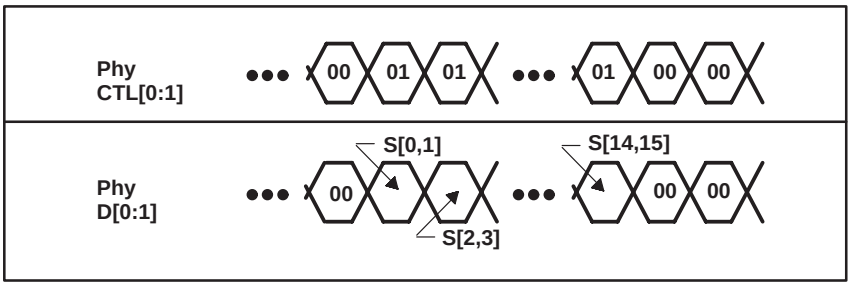

Figure 6. Status Transfer Timing

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