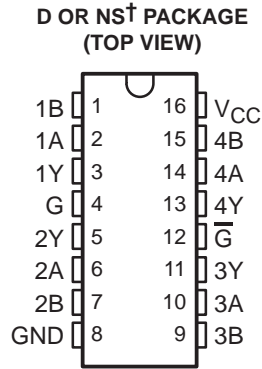# AM26LV32C
LOW-VOLTAGE HIGH-SPEED
QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS202C – MAY 1995 – REVISED SEPTEMBER 1998

- **Switching Rates up to 32 MHz**
- **Operates from a Single 3.3-V Supply**
- **Ultra-Low Power Dissipation . . . 27 mW Typ**
- **Open-Circuit Fail Safe**
- **−0.3-V to 5.5-V Common-Mode Range With ±200 mV Sensitivity**
- **Accepts 5-V Logic Inputs With a 3.3-V Supply**
- **Input Hysteresis . . . 50 mV Typ**
- **235 mW With Four Receivers at 32 MHz**
- **Pin Compatible With AM26C32, AM26LS32, and MB570**

D OR NS† PACKAGE
(TOP VIEW)

1B	1	16 V_{CC}
1A	2	15 4B
1Y	3	14 4A
G	4	13 4Y
2Y	5	12 $\overline{G}$
2A	6	11 3Y
2B	7	10 3A
GND	8	9 3B

† The NS package is only available left-ended taped and reeled.

description

The AM26LV32, BiCMOS, quadruple, differential line receiver with 3-state outputs is designed to be similar to TIA/EIA-422-B and ITU Recommendation V.11 receivers with reduced common-mode voltage range due to reduced supply voltage.

The device is optimized for balanced bus transmission at switching rates up to 32 MHz. The enable function is common to all four receivers and offers a choice of active-high or active-low inputs. The 3-state outputs permit connection directly to a bus-organized system. Each device features receiver high input impedance and input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range from −0.3 V to 5.5 V. When the inputs are open circuited, the outputs are in the high logic state. This device is designed using the Texas Instruments (TI™) proprietary LinIMPACT-C60™ technology, facilitating ultra-low power consumption without sacrificing speed.

This device offers optimum performance when used with the AM26LV31 quadruple line drivers.

The AM26LV32C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUT	ENABLES		OUTPUT
	G	$\overline{G}$	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
Open circuit	H	X	H
	X	L	H
X	L	H	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

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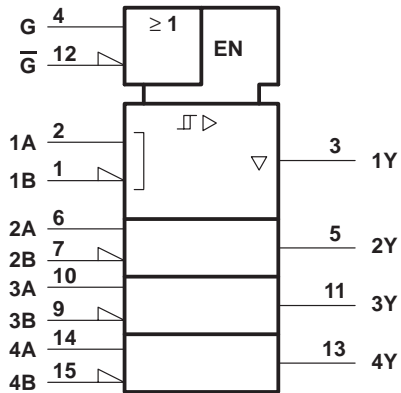
logic symbol[†]

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984
and IEC Publication 617-12.

logic diagram (positive logic)
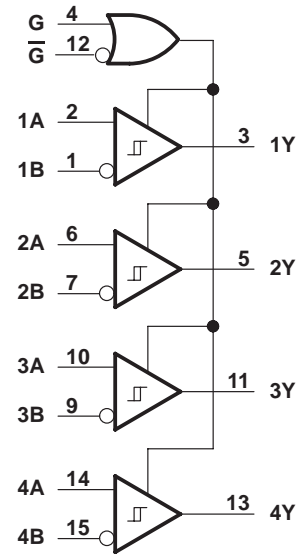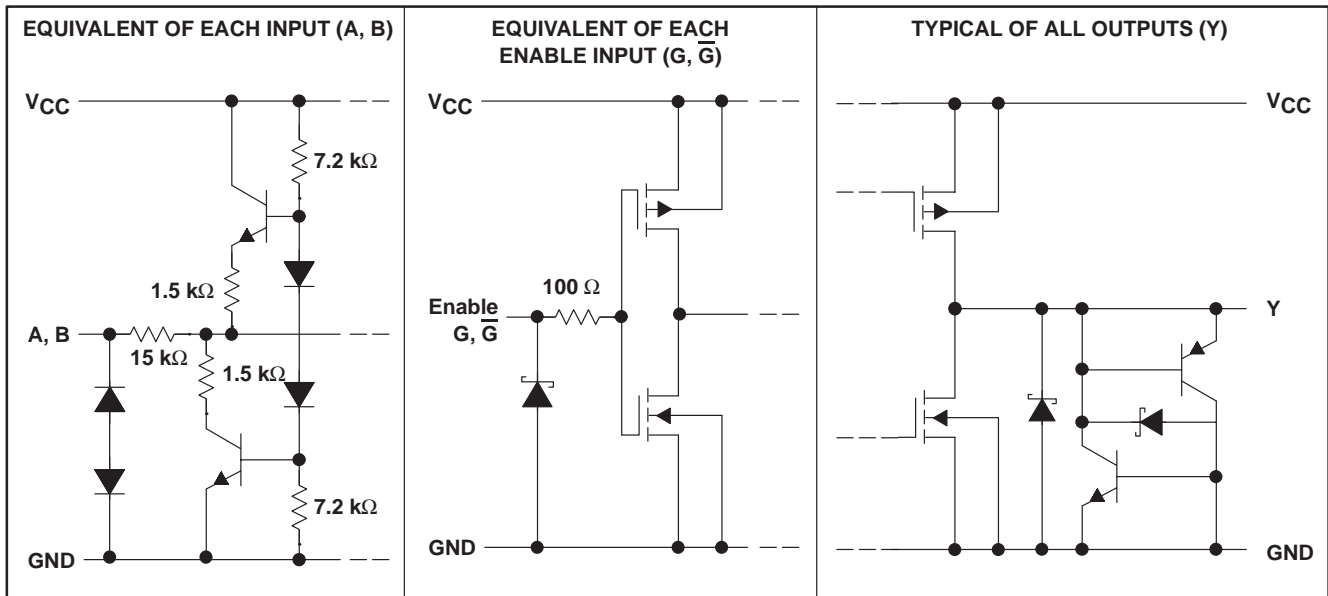

schematics of equivalent inputs and outputs

EQUIVALENT OF EACH INPUT (A, B)	EQUIVALENT OF EACH ENABLE INPUT (G, $\overline{G}$)	TYPICAL OF ALL OUTPUTS (Y)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . −0.3 V to 6 V

Input voltage range, V_I (A or B inputs) . . . . −4 V to 8 V

Differential input voltage, V_{ID} (see Note 2) . . . . ±12 V

Enable input voltage range . . . . −0.3 V to 6 V

Output voltage range, V_O . . . . −0.3 V to 6 V

Maximum output current, I_O . . . . ±25 mA

Package thermal impedance, θ_{JA} (see Note 3): D package . . . . 113°C/W

NS package . . . . 111°C/W

Storage temperature range, T_{stg} . . . . −65°C to 150°C

Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, $V_{IH(EN)}$	2			V
Low-level input voltage, $V_{IL(EN)}$			0.8	V
Common-mode input voltage, V_{IC}	−0.3		5.5	V
Differential input voltage, V_{ID}			±5.8	
High-level output current, I_{OH}			−5	mA
Low-level output current, I_{OL}			5	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended supply-voltage and operating free-air temperature ranges (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Differential input high-threshold voltage					0.2	V
V_{IT-}	Differential input low-threshold voltage			−0.2			V
V_{IK}	Enable input clamp voltage	$I_I = -18$ mA			−0.8	−1.5	V
V_{OH}	High-level output voltage	$V_{ID} = 200$ mV,	$I_{OH} = -5$ mA	2.4	3.2		V
V_{OL}	Low-level output voltage	$V_{ID} = -200$ mV,	$I_{OL} = 5$ mA		0.17	0.5	V
I_{OZ}	High-impedance-state output current	$V_O = 0$ to V_{CC}				±50	μA
$I_{IH(E)}$	High-level enable input current	$V_{CC} = 0$ or 3 V,	$V_I = 5.5$ V			10	μA
$I_{IL(E)}$	Low-level enable input current	$V_{CC} = 3.6$ V,	$V_I = 0$ V			−10	
r_I	Input resistance			7	12		kΩ
I_I	Input current	$V_I = 5.5$ V or -0.3 V,	All other inputs GND			±700	μA
I_{CC}	Supply current	$V_{I(E)} = V_{CC}$ or GND,	No load, line inputs open		8	17	mA
C_{pd}	Power dissipation capacitance‡	One channel			150		pF

† All typical values are at $V_{CC} = 3.3$ V and $T_A = 25°$C.
‡ C_{pd} determines the no-load dynamic current: $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$.

switching characteristics, $V_{CC} = 3.3$ V, $T_A = 25°$C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 1	8	16	20	ns
t_{PHL}	Propagation delay time, high- to low-level output		8	16	20	ns
t_t	Transistion time (t_r or t_f)	See Figure 1		5		ns
t_{PZH}	Output-enable time to high level	See Figure 2		17	40	ns
t_{PZL}	Output-enable time to low level	See Figure 3		10	40	ns
t_{PHZ}	Output-disable time from high level	See Figure 2		20	40	ns
t_{PLZ}	Output-disable time from low level	See Figure 3		16	40	ns
$t_{sk(p)}$	Pulse skew	See Note 4		4	6	ns
$t_{sk(o)}$	Skew limit	See Note 5		4	6	ns
$t_{sk(lim)}$	Skew limit (device to device)	See Note 6		6	9	ns

NOTES: 4. $t_{sk(p)}$ is $|t_{PLH} - t_{PHL}|$ of each channel.
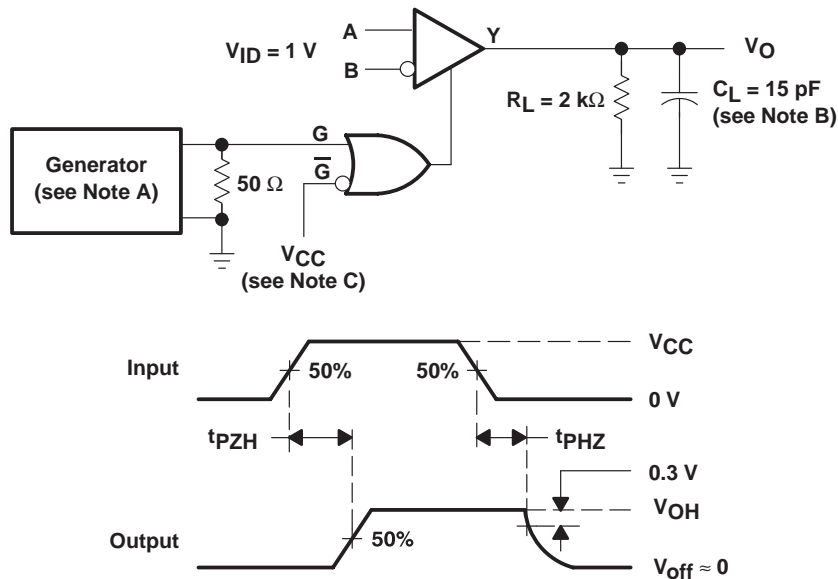5. $t_{sk(o)}$ is the maximum difference in propagation delay times between any two channels of one device.
6. $t_{sk(lim)}$ is the maximum difference in propagation delay times between any two channels of any two devices.

PARAMETER MEASUREMENT INFORMATION
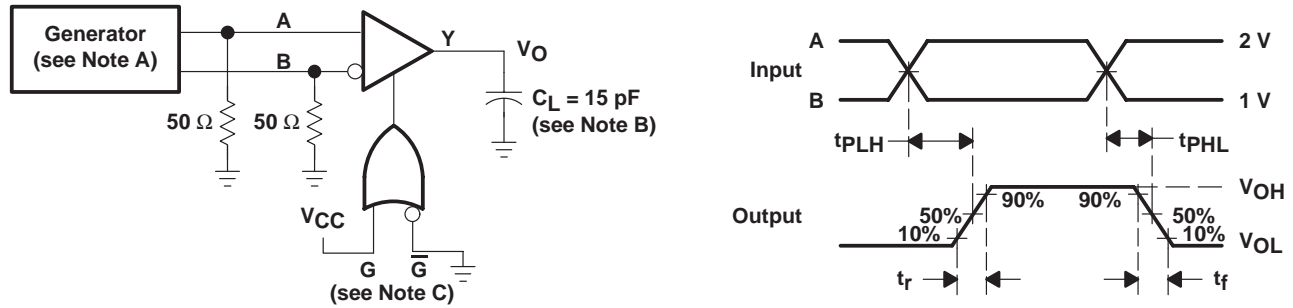
NOTES: A. The input pulse is supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR = 10 MHz, t_r and t_f (10% to 90%) ≤ 2 ns, 50% duty cycle.
B. C_L includes probe and jig capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

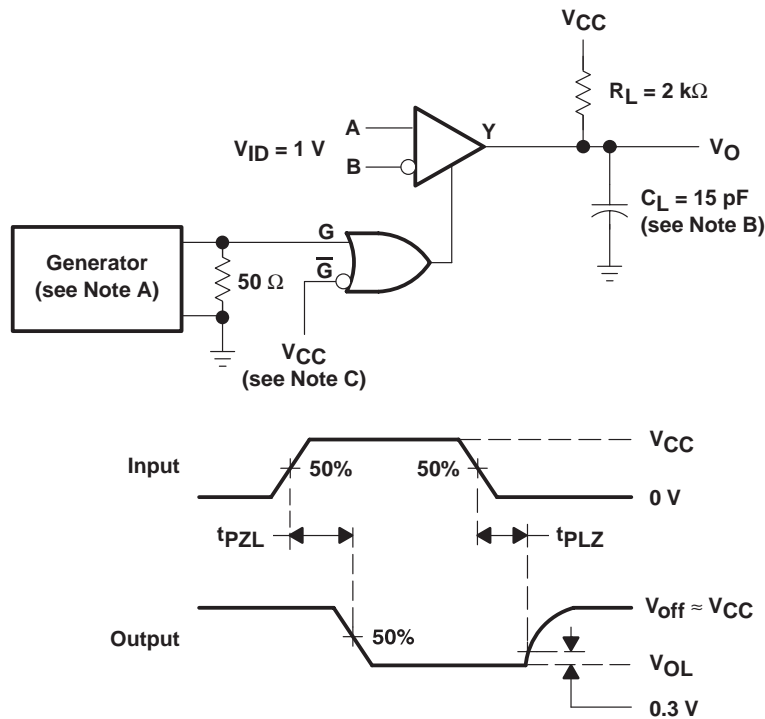**Figure 1. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR = 10 MHz, t_r and t_f (10% to 90%) ≤ 2 ns, 50% duty cycle.
B. C_L includes probe and jig capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

Figure 2. t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms

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NOTES: A. The input pulse is supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR = 10 MHz, t_r and t_f (10% to 90%) ≤ 2ns, 50% duty cycle.
   B. C_L includes probe and jig capacitance.
   C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

Figure 3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

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