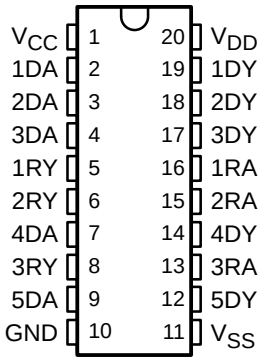
- **Single Chip With Easy Interface Between UART and Serial Port Connector of an External Modem or Other Computer Peripheral**
- **Five Drivers and Three Receivers Meet or Exceed the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28 Standards**
- **Designed to Support Data Rates Up To 120 kbps**
- **Complement To The GD75232**
- **Provides Pin-To-Pin Replacement For the Goldstar GD75323**
- **Pin-Out Compatible With SN75196**
- **Functional Replacement For the MC145405**

DW OR N PACKAGE
(TOP VIEW)



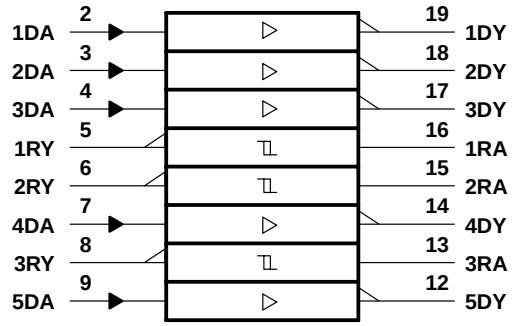
description

The GD75323 combines five drivers and three receivers from the trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers respectively. The flow-through design of the GD75323 decreases the part count, reduces the board space required, and allows easy interconnection of the UART and serial-port connector. The all-bipolar circuits and processing of the GD75323 provide a rugged, low-cost solution for this function.

The GD75323 complies with the requirements of the ANSI EIA/TIA-232-E and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and a peripheral at signal rates up to 20 kbps. The switching speeds of the GD75323 are fast enough to support rates up to 120 kbps with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates up to 120 kbps, use of ANSI Standard EIA/TIA-423-B and EIA/TIA-422-B and ITU Recommendations V.10 and V.11 are recommended.

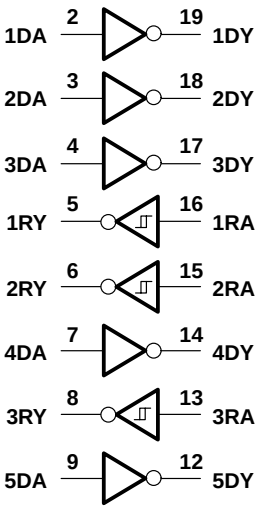
The GD75323 is characterized for operation over a temperature range of 0°C to 70°C.

logic symbol†



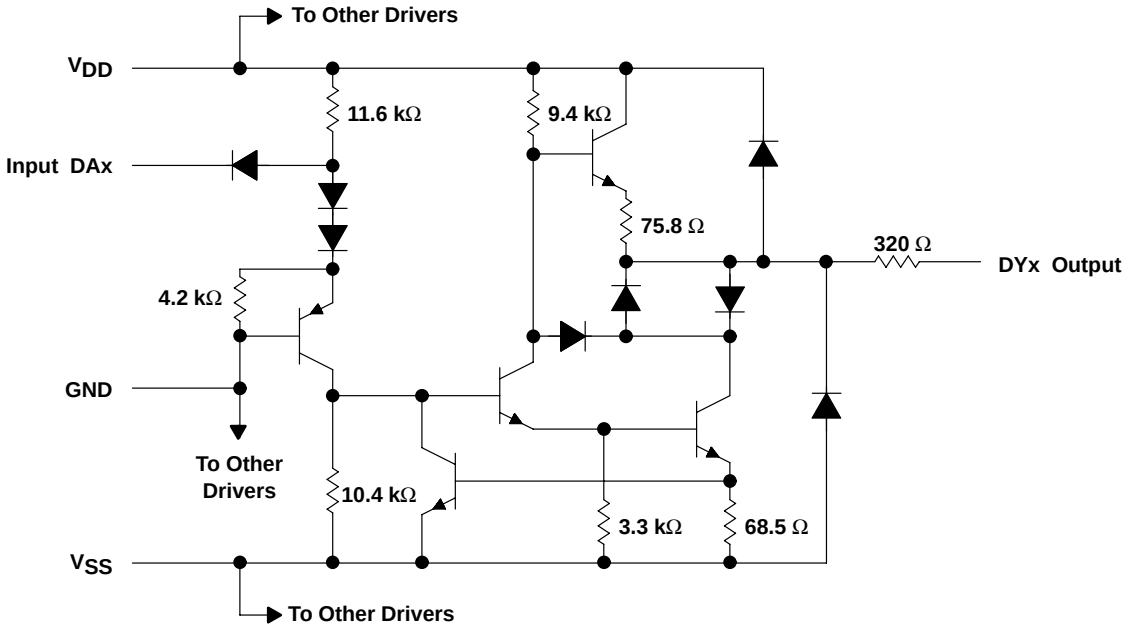
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



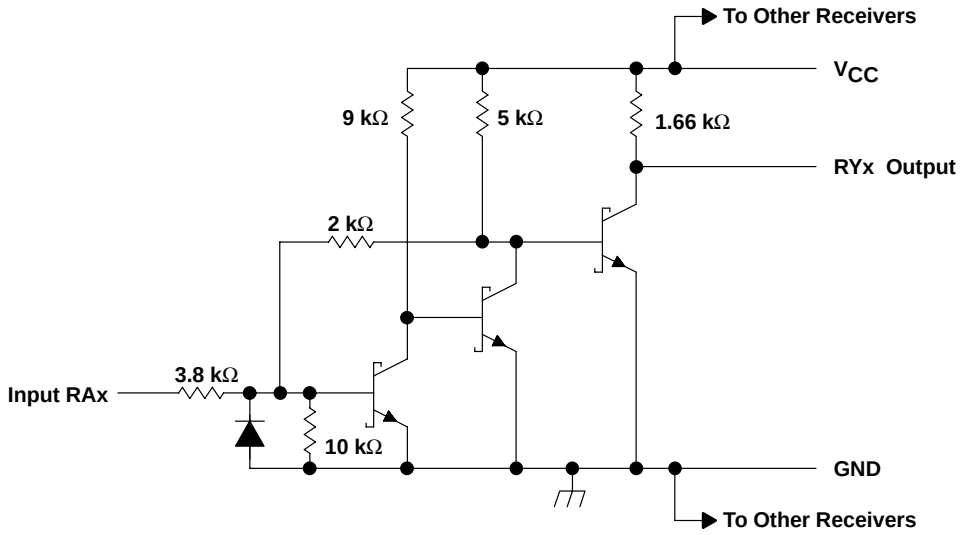
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

schematic (each driver)



Resistor values shown are nominal.

schematic (each receiver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 10 V
Supply voltage, V_{DD} (see Note 1) . . . . . 15 V
Supply voltage, V_{SS} (see Note 1) . . . . . –15 V
Input voltage range, V_I: Driver . . . . . –15 V to 7 V
Receiver . . . . . –30 V to 30 V
Output voltage range, V_O (Driver) . . . . . – 15 V to 15 V
Low-level output current, I_{OL} (Receiver) . . . . . 20 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

‡ This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		7.5	9	13.5	V
Supply voltage, V_{SS}		–7.5	–9	–13.5	V
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	Driver	1.9			V
Low-level input voltage, V_{IL}	Driver			0.8	V
High-level output current, I_{OH}	Driver			–6	mA
	Receiver			–0.5	
High-level output current, I_{OL}	Driver			6	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

supply currents over operating free-air temperature range

PARAMETER		TEST CONDITIONS				MIN	MAX	UNIT
I_{DD}	Supply current from V_{DD}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = –9 V		25	mA
				V_{DD} = 12 V,	V_{SS} = –12 V		32	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = –9 V		7.5	mA
				V_{DD} = 12 V,	V_{SS} = –12 V		9.5	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = –9 V		–25	mA
				V_{DD} = 12 V,	V_{SS} = –12 V		–32	mA
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = –9 V		–5.3	mA
				V_{DD} = 12 V,	V_{SS} = –12 V		–5.3	mA
I_{CC}	Supply current from V_{CC}	V_{DD} = 5 V,	All inputs at 5 V,		No load		20	mA

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 9 V, V_{SS} = –9 V, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	R_L = 3 kΩ,	See Figure 1	6	7.5		V
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 1.9 V,	R_L = 3 kΩ,	See Figure 1		–7.5	–6	V
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				10	μA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				–1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (see Note 3)	V_{IL} = 0.8 V,	V_O = 0,	See Figure 1	–4.5	–9	–19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_{IH} = 2 V,	V_O = 0,	See Figure 1	4.5	9	19	mA
r_o	Output resistance (see Note 4)	V_{CC} = V_{DD} = V_{SS} = 0,		V_O = –2 V to 2 V	300			Ω

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if –10 V is maximum, the typical value is a more negative voltage.
3. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
4. Test conditions are those specified by EIA/TIA-232-E and as listed above.

switching characteristics, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ±10%, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF, See Figure 3		315	500	ns
t_{PHL}	Propagation delay time, high- to low-level output				75	175	ns
t_{TLH}	Transition time, low- to high-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF, See Figure 3		60	100	ns
		R_L = 3 kΩ to 7 kΩ,	C_L = 2500 pF, See Figure 3 and Note 5		1.7	2.5	μs
t_{THL}	Transition time, high- to low-level output (see Note 5)	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF, See Figure 3		40	75	ns
		R_L = 3 kΩ to 7 kΩ,	C_L = 2500 pF, See Figure 3 and Note 6		1.5	2.5	μs

NOTES: 5. Measured between –3-V and 3 V points of the output waveform (EIA/TIA-232-E conditions), all unused inputs are tied either high or low.
6. Measured between 3-V and –3 V points of the output waveform (EIA/TIA-232-E conditions), all unused inputs are tied either high or low.

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Figure 5	T_A = 25°C	1.75	1.9	2.3	V
			T_A = 0°C to 70 °C	1.55		2.3	
V_{IT-}	Negative-going input threshold voltage	See Figure 5		0.75	0.97	1.25	
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)			0.5			
V_{OH}	High-level output voltage	I_{OH} = –0.5 mA	V_{IH} = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V_{OL}	Low-level output voltage	I_{OL} = 10 mA,	V_I = 3 V		0.2	0.45	V
I_{IH}	High-level input current	V_I = 25 V,	See Figure 5	3.6		8.3	mA
		V_I = 3 V,	See Figure 5	0.43			
I_{IL}	Low-level input current	V_I = –25 V,	See Figure 5	–3.6		–8.3	mA
		V_I = –3 V,	See Figure 5	–0.43			
I_{OS}	Short-circuit output current	See Figure 4			–3.4	–12	mA

† All typical values are at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 9 V, and V_{SS} = –9 V.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF, See Figure 6	R_L = 5 kΩ,		107	500	ns
t_{PHL}	Propagation delay time, high- to low-level output				42	150	ns
t_{TLH}	Transition time, low- to high-level output				175	525	ns
t_{THL}	Transition time, high- to low-level output				16	60	ns

PARAMETER MEASUREMENT INFORMATION

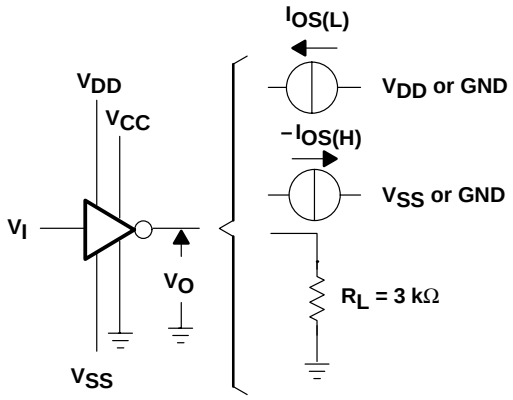


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

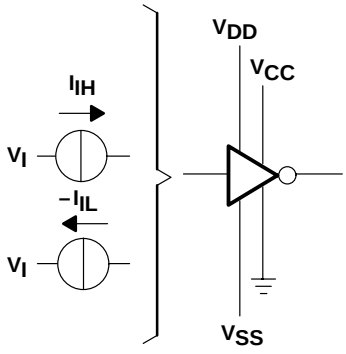
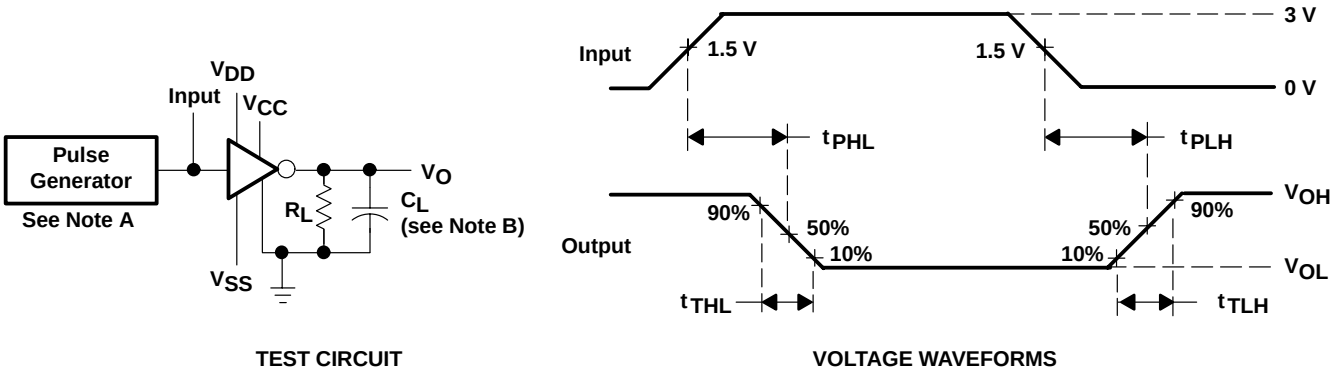


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

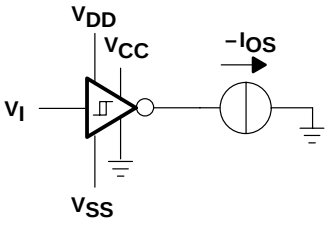


Figure 4. Receiver Test Circuit for I_{OS}

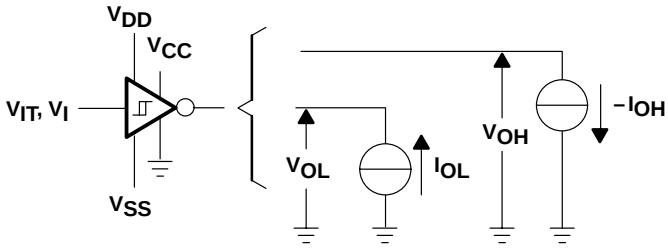
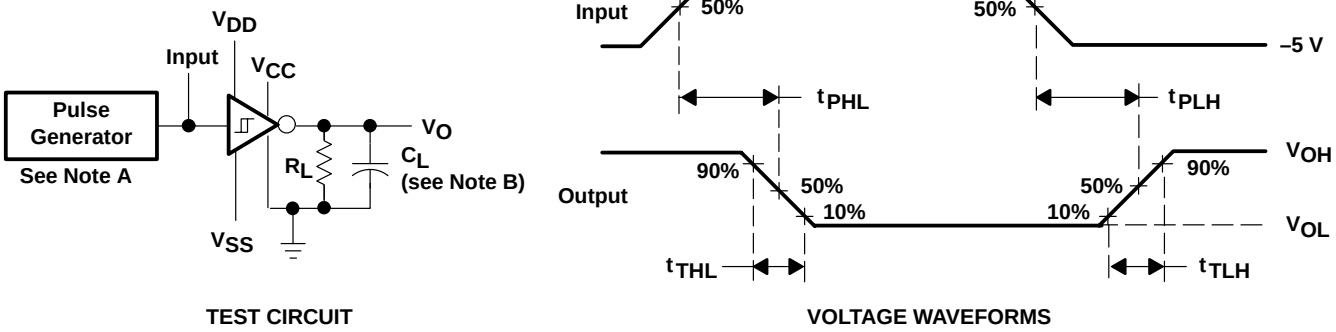


Figure 5. Receiver Test Circuit for V_{IT}, V_{OH}, and V_{OL}



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

VOLTAGE TRANSFER CHARACTERISTICS

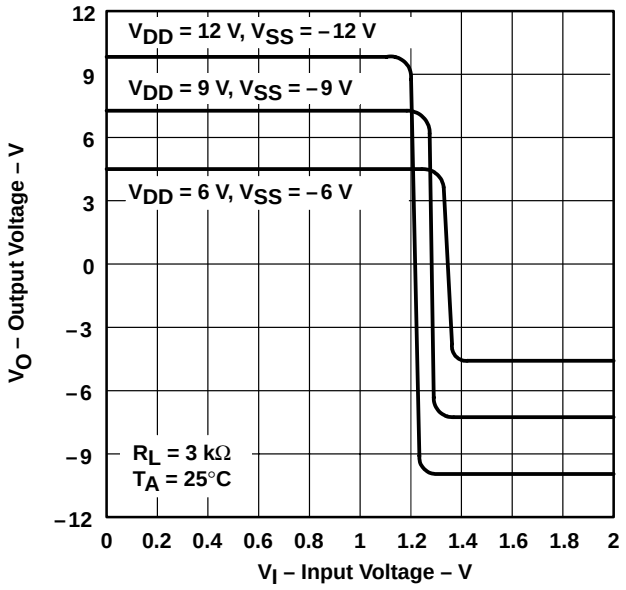


Figure 7

OUTPUT CURRENT vs OUTPUT VOLTAGE

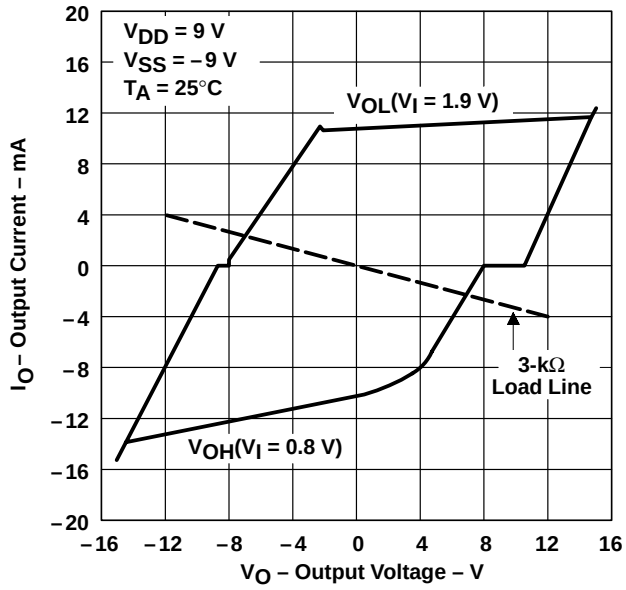


Figure 8

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

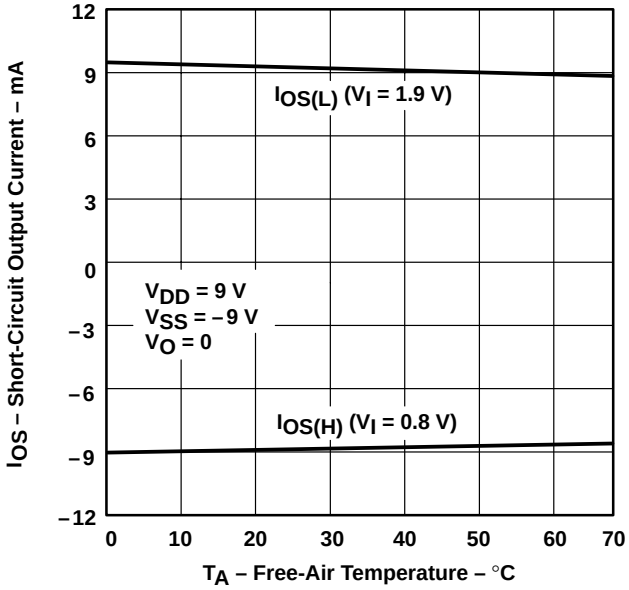


Figure 9

SLEW RATE vs LOAD CAPACITANCE

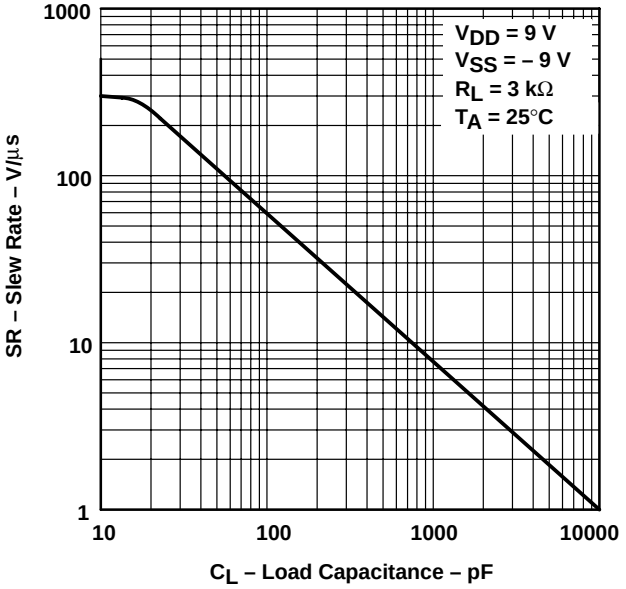


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER SECTION

INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

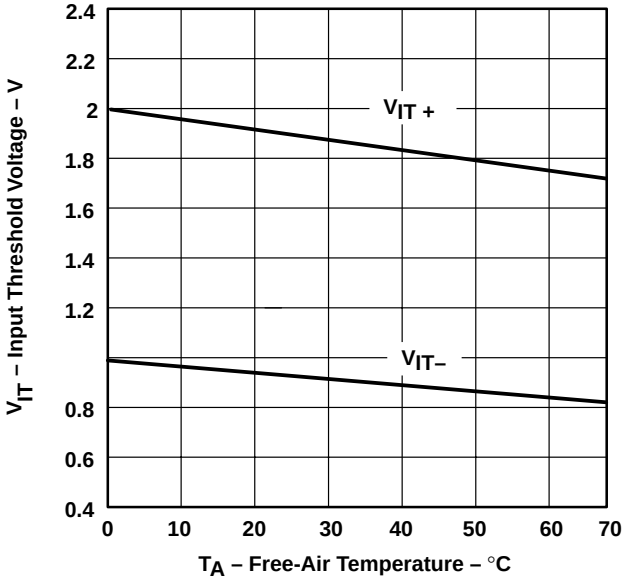


Figure 11

INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

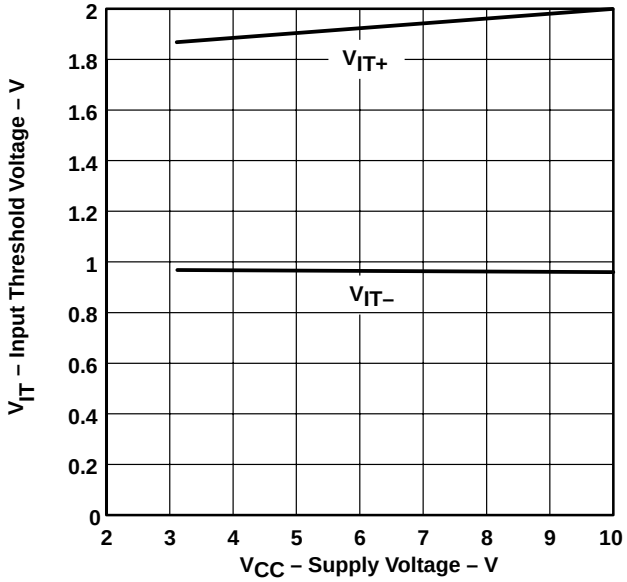
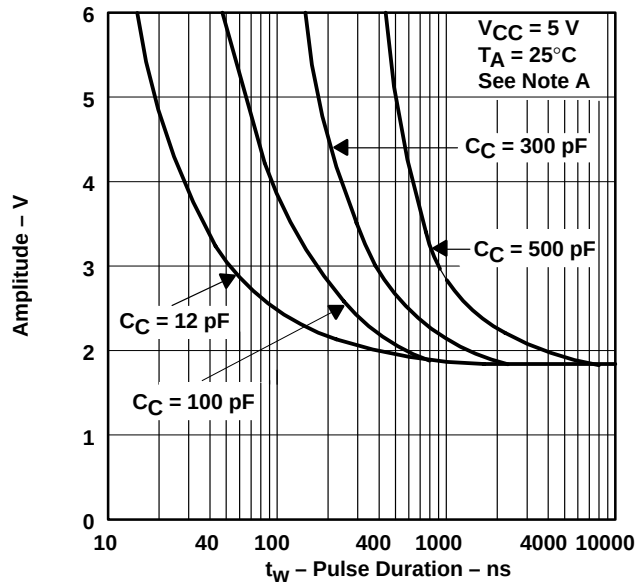


Figure 12

NOISE REJECTION



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, does not cause a change of the output level.

Figure 13

MAXIMUM SUPPLY VOLTAGE vs FREE-AIR TEMPERATURE

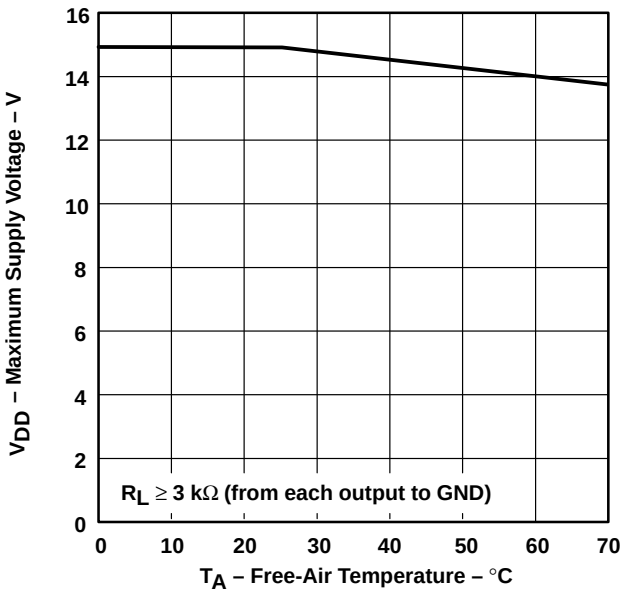


Figure 14

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the GD75323 in the fault condition in which the device outputs are shorted to V_{DD} or V_{SS}, and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

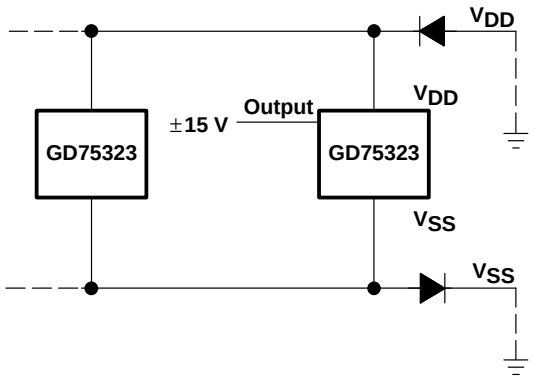
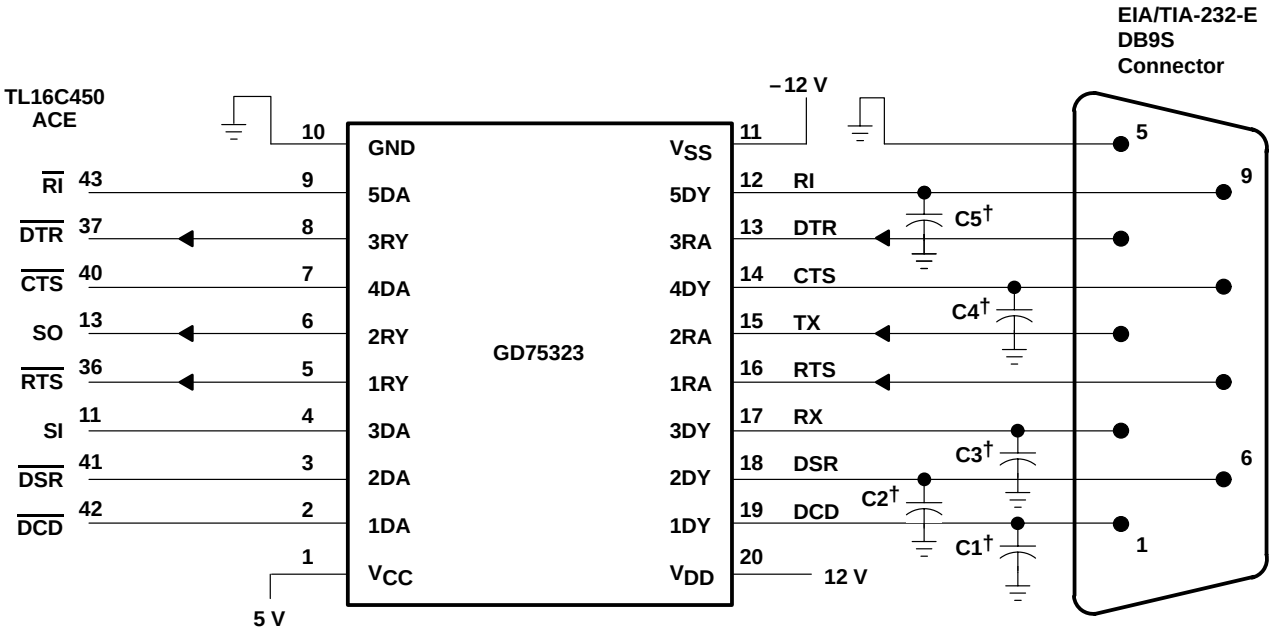


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of EIA/TIA-232-E



† See Figure 10 to select the correct values for the loading capacitors (C1, C2, C3, C4, and C5), which may be required to meet the RS-232 maximum slew-rate requirement of 30 V/μs. The value of the loading capacitors required depends upon the line length and desired slew rate, but is typically 330 pF.

NOTE C: To use the receivers only, V_{DD} and V_{SS} must both be powered or tied to ground.

Figure 16. Typical Connection

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