ERRATA
TO THE TSB11LV01 DATA SHEET
(TEXAS INSTRUMENTS LITERATURE NO. SLLS232B, MAY 1997)

This document contains corrections and additions to information in the TSB11LV01 data sheet (TI Literature Number SLLS232B, May 1997), also included in *IEEE 1394 Circuits Data Book*, 1997 (TI Literature Number SLLD004).

a. The TSB11LV01 device reports itself as a 3-port phy in the NP field of Register address 2 with ports 2 and 3 not connected. TI plans to correct this in a future revision.

b. Electrical isolation as described in Appendix J of IEEE 1394–1995 is not currently recommended by TI. The TSB11LV01 device is not tested to a level that would be required to implement the isolation in Appendix J of the standard. TI has an improved isolation technique, which is the recommended isolation solution. In a future revision, TI plans to add internal bus holders to support its new isolation scheme.

   – Please see *Galvanic Isolation of the IEEE 1394–1995 Serial Bus* (TI Literature Number SLLA011).

c. If CTRL 0 and CTRL 1 are high when LPS is switched from low to high, the phy-link interface hangs in the high-impedance state. TI plans to correct this in a future revision.

d. The twisted-pair output terminals do not meet current source specifications at high common-mode signal voltages and low supply voltages. Minimum supply voltage for a single-port power sourcing implementation is 3.3 V. TI plans to correct this in a future revision.

e. The TSB11LV01 transmits data_end for 220 ns to 225 ns, while the IEEE 1394–1995 standard calls for 240 ns to 260 ns. There are currently no plans to change this in the future.

f. The current revision of the TSB11LV01 device has gap times set to:

   – subaction-gap = ((gap_count $\times$ 16) + state_machine_delay) $\times$ BASE_RATE_PERIOD

   – arb-reset-gap = ((gap_count $\times$ 32) + state_machine_delay) $\times$ BASE_RATE_PERIOD

   where the BASE_RATE_PERIOD is 10 ns and the state_machine_delay for the TSB11LV01 is 8 ns for both subaction gap and arb-reset gap. This varies from the standard in that the state_machine_delay does not match the specification values of 28 and 52 for the respective gaps.

   All phys have a hysteresis time (arbitration delay time) built in, which is set to:

   – delay time = ((gap_count $\times$ 4) + state_machine_delay) $\times$ BASE_RATE_PERIOD

   After a subaction-gap or arb-reset-gap has been detected, the phy sends the appropriate status to the link. The TSB11LV01 waits for the delay-time period and then services any bus requests made to the link.

g. The received data prefix (data prefix time + speed signal length) for the TSB11LV01 has a minimum time of 180 ns. If the node transmitting to the 11LV01 does not provide 180 ns of data prefix, the first few bits of the packet may be missed. The remainder of the packet will be transferred to the link where it will fail the CRC checks and be ignored. If the node is repeating data, only that portion of the packet recognized (after the missed bits) will be repeated.

   All TI physical layers provide at least 180 ns of data prefix.

h. Deleted — replaced by item I below.

i. The following replaces previous errata item ***h***.

The datapacket_separation_time is defined as the total time from the end of the last bit sent in a packet to the beginning of the first bit sent in the next packet. This includes the data end time of the first packet, the bus idle time between the two packets, the arbitration time for the next packet, and the data prefix time of the second packet. Note that this is the same as the packet turn-around time mentioned in previous errata item ***h*** plus the data end time of the first packet.

The digital core in the TSB11LV01 PHY may not always correctly process received back-to-back packets that are spaced too closely together. For the packets to be processed correctly, the datapacket_separation_time must be approximately 690 ns or greater (the 450 ns from previous errata item ***h*** + 240 ns min data_end_time). A symptom of this problem is if a node communicating with the TSB11LV01 sends two packets to the TSB11LV01 too quickly, the initial bits of the second packet will not be received correctly. This causes a header CRC error and the packet to be discarded.

An example of this case is if a node is root (so it sources the cycle start packets), and the same node is also sending isochronous packets to an TSB11LV01 node. Since the root does not need to arbitrate for the bus, it will transmit the isochronous packet with a minimal datapacket separation time after the cycle start packet. This is an example of back-to-back packets that may not be processed properly. Any combination of production TI TSB21LV03 or TI's 400 Mbps Physical Layer devices with TI's current OHCILynx, PCILynx, GPLynx, MPEGLynx, DVLynx, or 12C01A link layer devices or future link layer devices will interoperate correctly when directly connected to the TSB11LV01 PHY or its derivatives.

Workaround:

A workaround to this problem for combinations of links and PHYs that have a datapacket separation time that is too short is to make the node that has the TSB11LV01 the root. This will ensure that every node transmitting to the TSB11LV01 must first arbitrate to send a packet. The arbitration time has been shown to be enough extra time to keep the problem from occurring (when using TI PHYs). Note that the only requirement is that the node sending the isochronous data to the TSB11LV01 must not be root. One method of ensuring this is to make the TSB11LV01 the root, and this can be accomplished using a PHY configuration packet.

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