

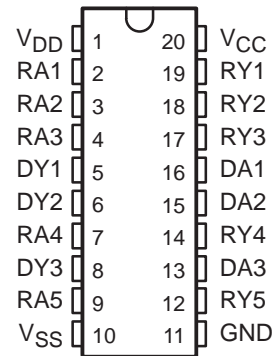
# SN75LP185A

## LOW-POWER MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS257G – AUGUST 1996 – REVISED SEPTEMBER 1998

- **Single-Chip TIA/EIA-232-F Interface for IBM™ PC/AT™ Serial Port**
- **Designed to Transmit and Receive 4- $\mu$ s Pulses (Equivalent to 256 kbit/s)**
- **Less Than 21-mW Power Consumption**
- **Wide Supply-Voltage Range, 4.75 V to 15 V**
- **Driver Output Slew Rates Are Internally Controlled to 30 V/ $\mu$ s Max**
- **Receiver Input Hysteresis, 1000 mV Typ**
- **TIA/EIA-232-F Bus-Pin ESD Protection Exceeds:**
  - 15-kV, Human-Body Model
  - 15-kV IEC1000-4-2, Air Gap
  - 8-kV IEC1000-4-2, Contact
- **Three Drivers and Five Receivers Meet or Exceed the Requirements of TIA/EIA-232-F and ITU V.28**
- **Complements the SN75LP196**
- **Designed to Replace the Industry-Standard SN75185 and SN75C185 With the Same Flow-Through Pinout**
- **Packaged in Plastic Small-Outline Package**

**DW PACKAGE  
(TOP VIEW)**



### description

The SN75LP185A is a low-power bipolar device containing three drivers and five receivers with 15 kV of ESD protection on the bus pins with respect to each other. Bus pins are defined as those pins that tie directly to the serial-port connector, including GND. The pinout matches the flow-through design of the industry-standard SN75185 and SN75C185. The flow-through pinout of the SN75LP185A allows easy interconnection of the UART and serial-port connector of the IBM PC/AT and compatibles. The SN75LP185A provides a rugged, low-cost solution for this function with the combination of the bipolar processing and 15 kV of ESD protection.

The SN75LP185A has internal slew-rate control to provide a maximum rate of change in the output signal of 30 V/ $\mu$ s. The driver output swing is nominally clamped at  $\pm 6$  V to enable the higher data rates associated with this device and to reduce EMI emissions. Even though the driver outputs are clamped, they can handle voltages up to  $\pm 15$  V without damage. All the logic inputs can accept 3.3-V or 5-V input signals.

The SN75LP185A complies with the requirements of TIA/EIA-232-F and ITU V.28. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20 kbit/s. The switching speeds of the SN75LP185A support rates up to 256 kbit/s.

The SN75LP185A is characterized for operation from 0°C to 70°C.



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## Function Tables

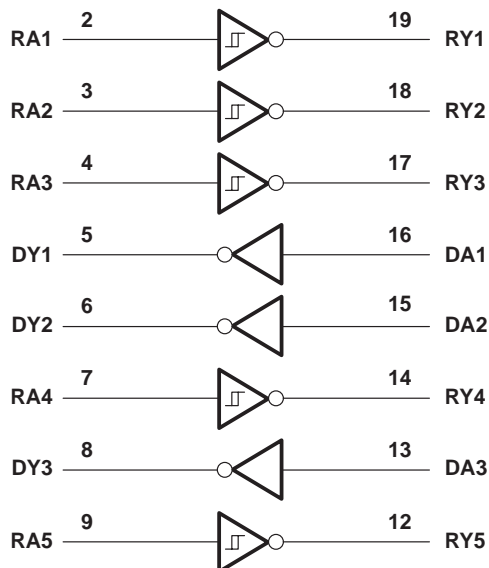
### DRIVER

INPUT DA	OUTPUT DY
H	L
L	H
Open	L

### RECEIVER

INPUT RA	OUTPUT RY
H	L
L	H
Open	H

## logic diagram (positive logic)



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply-voltage range (see Note 1): $V_{CC}$ .....	–0.5 V to 7 V
$V_{DD}$ (see Note 1) .....	–0.5 V to 15 V
Negative supply-voltage range, $V_{SS}$ (see Note 1) .....	0.5 V to –15 V
Input-voltage range, $V_I$ : Receiver (RA) .....	–30 V to 30 V
Driver (DA) .....	–0.5 V to $V_{CC}+0.4$ V
Output-voltage range, $V_O$ : Receiver (RY) .....	–0.5 V to 6 V
Driver (DY) .....	–15 V to 15 V
Electrostatic discharge (see Note 2): Bus pins (human-body model) .....	Class 3, A: 15 kV
Bus pins (machine model) .....	Class 3, B: 500 V
Bus pins (IEC1000-4-2, contact) .....	Class 3, C: 8 kV
Bus pins (IEC1000-4-2, air gap) .....	Class 3, D: 15 kV
All pins (human-body model) .....	Class 3, A: 5 kV
All pins (machine model) .....	Class 3, B: 400 V
Package thermal impedance, $\theta_{JA}$ (see Note 3) .....	97°C/W
Storage temperature range, $T_{stg}$ .....	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to network ground terminal, unless otherwise noted.  
 2. Per MIL-STD-883 Method 3015.7  
 3. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage (see Note 4)	4.75	5	5.25	V
$V_{DD}$	Supply voltage (see Note 5)	9	12	15	V
$V_{SS}$	Supply voltage (see Note 5)	–9	–12	–15	V
$V_{IH}$	High-level input voltage		2		V
$V_{IL}$	Low-level input voltage			0.8	V
$V_I$	Receiver input voltage		–25	25	V
$I_{OH}$	High-level output current			–1	mA
$I_{OL}$	Low-level output current			2	mA
$T_A$	Operating free-air temperature	0		70	°C

- NOTES: 4.  $V_{CC}$  cannot be greater than  $V_{DD}$ .  
 5. The device operates down to  $V_{DD} = V_{CC}$  and  $|V_{SS}| = V_{CC}$ , but supply currents increase and other parameters may vary slightly from the data-sheet limits.



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## LOW-POWER MULTIPLE RS-232 DRIVERS AND RECEIVERS

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### supply currents over the recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current for $V_{CC}$ , $I_{CC}$	$V_{DD} = 9\text{ V}$ , $V_{SS} = -9\text{ V}$			1000	$\mu\text{A}$
	$V_{DD} = 12\text{ V}$ , $V_{SS} = -12\text{ V}$			1000	
Supply current for $V_{DD}$ , $I_{DD}$	No load, All inputs at minimum $V_{OH}$ or maximum $V_{OL}$	$V_{DD} = 9\text{ V}$ , $V_{SS} = -9\text{ V}$		450	
		$V_{DD} = 12\text{ V}$ , $V_{SS} = -12\text{ V}$		450	
Supply current for $V_{SS}$ , $I_{SS}$		$V_{DD} = 9\text{ V}$ , $V_{SS} = -9\text{ V}$		-625	
		$V_{DD} = 12\text{ V}$ , $V_{SS} = -12\text{ V}$		-625	

### driver electrical characteristics over the recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
$V_{OH}$ High-level output voltage	$V_{IL} = 0.8\text{ V}$ , $R_L = 3\text{ k}\Omega$ , See Figure 1	$V_{DD} = 9\text{ V}$ , $V_{SS} = -9\text{ V}$	5	5.8	6.6	V
		$V_{DD} = 12\text{ V}$ , $V_{SS} = -12\text{ V}$ , See Note 6	5	5.8	6.6	
$V_{OL}$ Low-level output voltage	$V_{IH} = 2\text{ V}$ , $R_L = 3\text{ k}\Omega$ , See Figure 1	$V_{DD} = 9\text{ V}$ , $V_{SS} = -9\text{ V}$	-5	-5.8	-6.9	V
		$V_{DD} = 12\text{ V}$ , $V_{SS} = -12\text{ V}$ , See Note 6	-5	-5.9	-6.9	
$I_{IH}$ High-level input current	$V_I$ at $V_{CC}$			1	$\mu\text{A}$	
$I_{IL}$ Low-level input current	$V_I$ at GND			-1	$\mu\text{A}$	
$I_{OS(H)}$ Short-circuit high-level output current	$V_O = \text{GND}$ or $V_{SS}$ . See Figure 2 and Note 7		-30	-55	mA	
$I_{OS(L)}$ Short-circuit low-level output current	$V_O = \text{GND}$ or $V_{DD}$ . See Figure 2 and Note 7		30	55	mA	
$r_o$ Output resistance	$V_{DD} = V_{SS} = V_{CC} = 0$ , $V_O = 2\text{ V}$	300			$\Omega$	

NOTES: 6. Maximum output swing is nominally clamped at  $\pm 6\text{ V}$  to enable the higher data rates associated with this device and to reduce EMI emissions. The driver outputs may slightly exceed the maximum output voltage over the full  $V_{CC}$  and temperature ranges.  
7. Not more than one output should be shorted at one time.



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## LOW-POWER MULTIPLE RS-232 DRIVERS AND RECEIVERS

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### driver switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
$t_{PHL}$	Propagation delay time, high- to low-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , See Figure 1	300	800	1600	ns		
$t_{PLH}$	Propagation delay time, low- to high-level output	$R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , See Figure 1	300	800	1600	ns		
$t_{TLH}$	Transition time, low- to high-level output	$V_{CC} = 5\text{ V}$ , $V_{DD} = 12\text{ V}$ , $V_{SS} = -12\text{ V}$ , $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , See Figure 1 and Note 9	Using $V_{TR} = 10\%$ -to- $90\%$ transition region, Driver speed = 250 kbit/s, $C_L = 15\text{ pF}$ , See Note 8		375	2240	ns	
			Using $V_{TR} = \pm 3\text{ V}$ transition region, Driver speed = 250 kbit/s, $C_L = 15\text{ pF}$		200	1500		
			Using $V_{TR} = \pm 2\text{ V}$ transition region, Driver speed = 250 kbit/s, $C_L = 15\text{ pF}$		133	1000		
			Using $V_{TR} = \pm 3\text{ V}$ transition region, Driver speed = 125 kbit/s, $C_L = 2500\text{ pF}$			2750		
$t_{THL}$	Transition time, high- to low-level output	$V_{CC} = 5\text{ V}$ , $V_{DD} = 12\text{ V}$ , $V_{SS} = -12\text{ V}$ , $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , See Figure 1 and Note 9	Using $V_{TR} = 10\%$ -to- $90\%$ transition region, Driver speed = 250 kbit/s, $C_L = 15\text{ pF}$ , See Note 8		375	2240	ns	
			Using $V_{TR} = \pm 3\text{ V}$ transition region, Driver speed = 250 kbit/s, $C_L = 15\text{ pF}$		200	1500		
			Using $V_{TR} = \pm 2\text{ V}$ transition region, Driver speed = 250 kbit/s, $C_L = 15\text{ pF}$		133	1000		
			Using $V_{TR} = \pm 3\text{ V}$ transition region, Driver speed = 125 kbit/s, $C_L = 2500\text{ pF}$			2750		
SR	Output slew rate	$V_{CC} = 5\text{ V}$ , $V_{DD} = 12\text{ V}$ , $V_{SS} = -12\text{ V}$	Using $V_{TR} = \pm 3\text{ V}$ transition region, Driver speed = 0 to 250 kbit/s, $C_L = 15\text{ pF}$		4	20	30	V/us

NOTES: 8. Equivalent to the SN75C185. The SN75LP185A output-voltage swing is clamped to about 70% of the typical SN75C185 output-voltage swing, and the specified limits reflect the reduced output swing.

9. Maximum output swing is limited to  $\pm 6\text{ V}$  to enable the higher data rates associated with this device and to reduce EMI emissions.

### receiver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+}$	Positive-going input threshold voltage	See Figure 3	1.6	2	2.55	V
$V_{IT-}$	Negative-going input threshold voltage	See Figure 3	0.6	1	1.45	V
$V_{HYS}$	Input hysteresis, $V_{IT+}$ $V_{IT-}$	See Figure 3	600	1000		mV
$V_{OH}$	High-level output voltage	$I_{OH} = -1\text{ mA}$	2.5	3.9		V
$V_{OL}$	Low-level output voltage	$I_{OL} = 2\text{ mA}$		0.33	0.5	V
$I_{IH}$	High-level input current	$V_I = 3\text{ V}$	0.43	0.6	1	mA
		$V_I = 25\text{ V}$	3.6	5.1	8.3	
$I_{IL}$	Low-level input current	$V_I = -3\text{ V}$	-0.43	-0.6	-1	mA
		$V_I = -25\text{ V}$	-3.6	-5.1	-8.3	
$I_{OS(H)}$	Short-circuit high-level output current	$V_O = 0$ , See Figure 5 and Note 7			-20	mA
$I_{OS(L)}$	Short-circuit low-level output current	$V_O = V_{CC}$ , See Figure 5 and Note 7			20	mA
$R_{IN}$	Input resistance	$V_I = \pm 3\text{ V}$ to $\pm 25\text{ V}$	3	5	7	k $\Omega$

NOTE 7: Not more than one output should be shorted at one time.



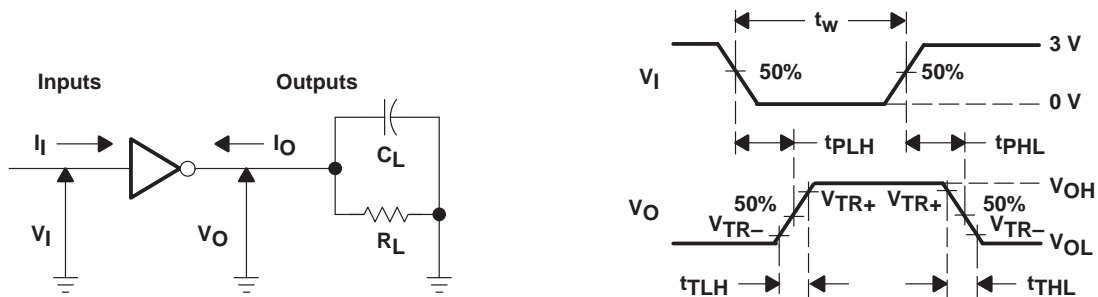
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receiver switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 4)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{PHL}$	Propagation delay time, high- to low-level output		400	900	ns
$t_{PLH}$	Propagation delay time, low- to high-level output		400	900	ns
$t_{TLH}$	Transition time, low- to high-level output		200	500	ns
$t_{THL}$	Transition time, high- to low-level output		200	400	ns
$t_{SK(p)}$	Pulse skew $ t_{PLH} - t_{PHL} $		200	425	ns

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics:  
 For  $C_L < 1000$  pF:  $t_w = 4$   $\mu$ s, PRR = 250 kbit/s,  $Z_O = 50$   $\Omega$ ,  $t_r = t_f < 50$  ns.  
 For  $C_L = 2500$  pF:  $t_w = 8$   $\mu$ s, PRR = 125 kbit/s,  $Z_O = 50$   $\Omega$ ,  $t_r = t_f < 50$  ns.  
 B.  $C_L$  includes probe and jig capacitance.

Figure 1. Driver Parameter Test Circuit and Waveform

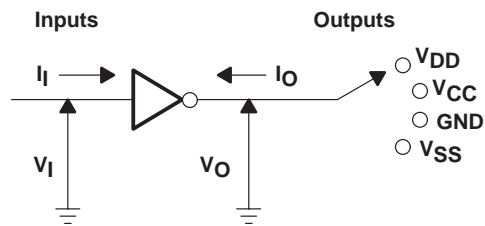


Figure 2. Driver  $I_{OS}$  Test

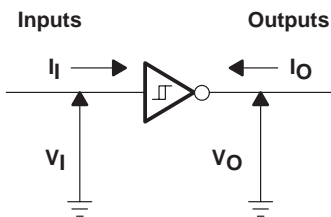
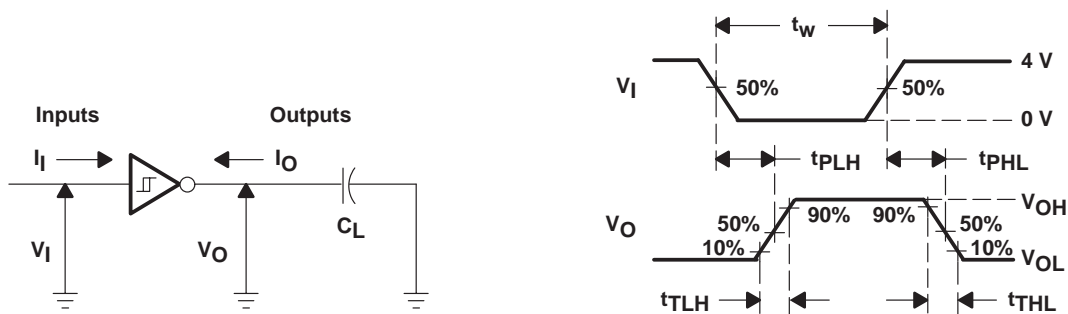


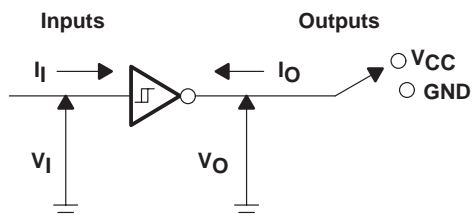
Figure 3. Receiver  $V_{IT}$  Test

**PARAMETER MEASUREMENT INFORMATION**



NOTES: A. The pulse generator has the following characteristics:  $t_w = 4 \mu\text{s}$ , PRR = 250 kbit/s,  $Z_O = 50 \Omega$ ,  $t_r = t_f < 50 \text{ ns}$ .  
 B.  $C_L$  includes probe and jig capacitance.

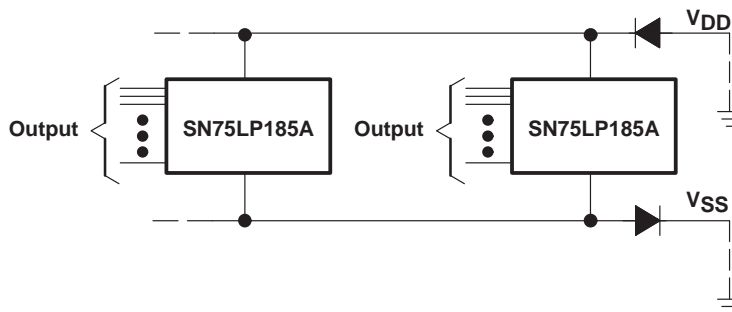
**Figure 4. Receiver Parameter Test Circuit and Waveform**



**Figure 5. Receiver  $I_{OS}$  Test**

**APPLICATION INFORMATION**

Diodes placed in series with the  $V_{DD}$  and  $V_{SS}$  leads protect the SN75LP185A in the fault condition when the device outputs are shorted to  $\pm 15 \text{ V}$  and the power supplies are at low voltage and provide low-impedance paths to ground (see Figure 6).



**Figure 6. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F**

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