ERRATA TO THE TSB21LV03A DATA SHEET

(TEXAS INSTRUMENTS LITERATURE NO. SLLS278, NOVEMBER 1997)

This document contains corrections and additions to information in the TSB21LV03A data sheet (TI Literature Number SLLS278, November 1997). Information on circuit modifications required when changing from the TSB21LV03 to the TSB21LV03A is also included.

Application notes:

a. If a network of 5 or more TSB21LV03As is connected, upon bus reset the TSB21LV03A network may not initially issue the correct number of self–ID packets. If this occurs, the TSB21LV03As that did not issue a self–ID packet will cause another bus reset. This bus reset process will continue until the correct number of self–ID packets are issued unless the process is interrupted by receipt of a non-self–ID packet. With 4 or fewer nodes the problem does not occur. The occurrences are greater at higher operating voltages. The average frequency of occurrence (number of resets before multiple self–ID packages occur) at room temperature with a supply voltage of 3.3 V is shown below:

5 nodes	28 resets
6 nodes	21 resets
7 nodes	14 resets
8 nodes	6 resets
9 nodes	8 resets
10 nodes	4 resets
11 nodes	2 resets
12 nodes	0 resets

With 12 or more nodes, every initiation of a reset will generate at least 1 more reset.

Workaround:

To allow the bus reset sequence described above to complete, it must not be interrupted by cycle start packets, PHY configuration packets, or asynchronous packets. It is recommended that upon bus reset, the isochronous resource manager node (and/or the bus manager node) should wait for 450 microseconds after the start of the initial bus reset and then check to see if another bus reset indication has been sent to the link. If another bus reset has been indicated, repeat the wait. If another bus reset has not been indicated, then resume cycle start packets and asynchronous packets. The bus manager should use the final package of self–IDs received.

Note that if multiple bus resets occur, all nodes will have their gap counts reset to 3F hex (2 bus resets in a row set all gap counts to the default 3F hex). If operating in a larger network (5 or more TSB21LV03A PHYs in a branching configuration, or more than 7 in a daisy chain configuration), setting the gap counts to any value other than 3F may require multiple attempts and is not recommended. With more than 11 nodes, setting the gap count to any value other than 3F typically will not work.

b. Due to an erroneous arbitration state when in a large network, there is a possibility that the TSB21LV03A may not leave the bus reset state. This will be seen as the network never successfully issuing any self–ID packets and repeating the bus initialization and tree–ID phases of bus reset. One method to stop this state is to power cycle the PHY device causing the resets.

This will not occur to a leaf node, but may occur in a branch node.

Workaround:

To minimize the chance of this occurring (but not prevent the occurrence), the following supply voltages are recommended, depending on whether a node sources cable power, and whether a node may be a branch or only a leaf node.

– If a node may only be a leaf node, the recommended supply voltage is the normal data sheet values.

– If a node may be a branch and also sources cable power, the recommended supply voltage range for the TSB21LV03A is 3.1 V ± 0.1 V (3.1 V ± 3.2%). A maximum of 2 ports utilized is recommended.

– If a node may be a branch but does not source cable power, the recommended supply voltage range is 2.8 V ± 0.1 V (2.8 V ± 3.6%).

This problem will be fixed in a new release of the TSB21LV03.

Application changes for device production revision A (TSB21LV03*A*):

When replacing TSB21LV03 devices with production revision A devices (TSB21LV03A) in applications, the following items are applicable:

aa. Bus holder functionality was added to the following TSB21LV03A terminals:

– phy/link interface data terminals D0 – D3 (pins 13, 14, 15, and 16)

– phy/link interface control terminals CTL0 and CTL1 (pins 11 and 12)

– phy/link interface link power status terminal LPS (pin 2)

– phy/link interface link request terminal LREQ (pin 3)

– phy/link interface power down terminal PD (pin 7)

Consequently:

- If any of these pins are to be tied to a fixed state through a resistor, the resistor must be sized to provide enough current to overcome the bus hold function. The recommended value is 1 kΩ.
- If pulldown resistors are used on the control 0 and control 1 pins (CTL0 and CTL1), these resistors should also be 1 kΩ.
- The LPS pin (pin 2) is a special case. If the LPS pin is tied to the link power plane directly, it must be connected through a 1-kΩ resistor to avoid problems in the case of the phy being powered down and the link being powered up. The 1-kΩ resistor prevents the link power plane from supplying power via the LPS connection to the phy when the phy is powered down.

bb. The TSB21LV03***A*** SYSCLK output is active when chip reset is active (low).

The TSB21LV03 SYSCLK output was *NOT* active when chip reset was low.

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