- **9 Channels for the Data and Control Paths of the Small Computer Systems Interface (SCSI)**
- **Supports Single-Ended and Low-Voltage Differential (LVD) SCSI**
- **Includes DIFFSENS Comparators on CDE0**
- **Receivers Include Noise Pulse Rejection Circuitry**
- **Packaged in Thin Shrink Small-Outline Package with 20-Mil Terminal Pitch**
- **Low Disabled Supply Current 7 mA Maximum**
- **Power-Up/Down Glitch Protection**
- **Bus is High-Impedance with $V_{CC} = 0$**
- **Pin-Compatible with the SN75976ADGG High-Voltage Differential Transceiver**

DGG PACKAGE
(TOP VIEW)

INV/$\overline{\text{NON}}$	1	56	CDE2
GND	2	55	CDE1
GND	3	54	CDE0
1A	4	53	9B+
1DE/$\overline{\text{RE}}$	5	52	9B–
2A	6	51	8B+
2DE/$\overline{\text{RE}}$	7	50	8B–
3A	8	49	7B+
3DE/$\overline{\text{RE}}$	9	48	7B–
4A	10	47	6B+
4DE/$\overline{\text{RE}}$	11	46	6B–
V_{CC}	12	45	V_{CC}
GND	13	44	GND
GND	14	43	GND
GND	15	42	GND
GND	16	41	GND
GND	17	40	GND
V_{CC}	18	39	V_{CC}
5A	19	38	5B+
5DE/$\overline{\text{RE}}$	20	37	5B–
6A	21	36	4B+
6DE/$\overline{\text{RE}}$	22	35	4B–
7A	23	34	3B+
7DE/$\overline{\text{RE}}$	24	33	3B–
8A	25	32	2B+
8DE/$\overline{\text{RE}}$	26	31	2B–
9A	27	30	1B+
9DE/$\overline{\text{RE}}$	28	29	1B–

description

The SN75LVDM976 has nine transceivers for transmitting or receiving the signals to or from a SCSI data bus. It offers electrical compatibility to both the single-ended signaling of X3.277:1996– SCSI–3 Parallel Interface (Fast–20) and the new low-voltage differential signaling method of proposed standard 1142–D SCSI Parallel Interface – 2 (SPI–2).

The 'LVDM976 differential drivers are non-symmetrical. The SCSI bus uses a dc bias on the line to allow terminated fail safe and wired-OR signalling. This bias can be as high as 125 mV and induces a difference in the high-to-low and low-to-high transition times of a symmetrical driver. In order to reduce pulse skew, a LVD SCSI driver's output characteristics become non-symmetrical. In other words, there is more assertion current to or from the driver than negation current. This allows the actual differential signal voltage on the bus to be symmetrical about 0 V. Even though the driver output characteristics are non-symmetrical, the design of the 'LVDM976 drivers maintain balanced signalling. Balanced means that the current that flows in each signal line is nearly equal but opposite in direction and is one of the keys to the low-noise performance of a differential bus.
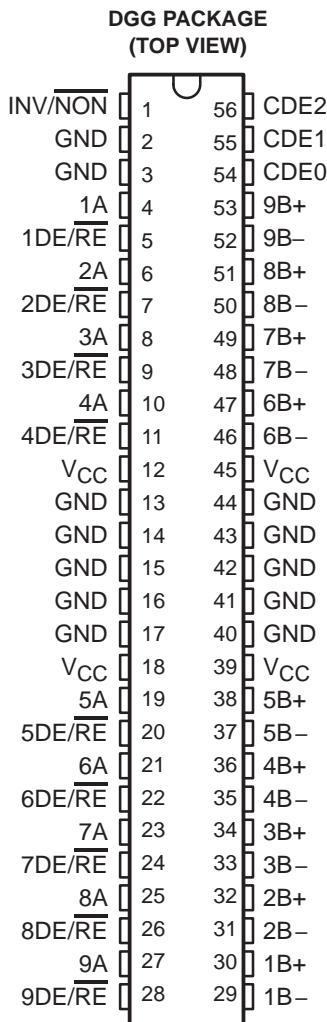
AVAILABLE OPTIONS

	PACKAGE
T_A	**TSSOP (DGG)**
0°C to 70°C	SN75LVDM976DGG SN75LVDM976DGGR†

† The R suffix designates a taped and reeled package.

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TEXAS INSTRUMENTS

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description (continued)

The signal symmetry requirements of the LVD-SCSI bus means you can no longer obtain logical inversion of a signal by simply reversing the differential signal connections. This requires the ability to invert the logic convention through the INV/$\overline{\text{NON}}$ terminal. This input would be a low for SCSI controllers with active-high data and high for active-low data. In either case, the B+ signals of the transceiver must be connected to the SIGNAL+ line of the SCSI bus and the B– of the transceiver to the SIGNAL– line.

The CDE0 input to the 'LVDM976 incorporates a window comparator to detect the status of the DIFFSENS line of a SCSI bus. This line is below 0.4 V, when using single-ended signals, is between 1.8 V and 2.4 V, when using low-voltage differential, and is above 2.4 V, when using high-voltage differential. The outputs assume the characteristics of single-ended or LVD accordingly or place the outputs into high-impedance, when HVD is detected. This, and the INV/$\overline{\text{NON}}$ input, are the only difference to the trade standard function of the SN75976A HVD transceiver.

The SN75LVDM976 is characterized for operation over an free-air temperature range of $T_A = 0°C$ to $70°C$.

logic diagram (positive logic)

CDE1

INV/$\overline{\text{NON}}$

LVD

2.4 V

CDE0

SE

0.5 V

1DE/$\overline{\text{RE}}$

1A

1DEb
1DEa

1REb
1REa

1DEb

1REb

1DEa

1REa

1B−

1B+

2A
2DE/$\overline{\text{RE}}$
Channel 2
2B−
2B+

3A
3DE/$\overline{\text{RE}}$
Channel 3
3B−
3B+

4A
4DE/$\overline{\text{RE}}$
Channel 4
4B−
4B+

INV/$\overline{\text{NON}}$

SE   LVD

CDE2

5A
5DE/$\overline{\text{RE}}$
Channel 5
5B−
5B+

6A
6DE/$\overline{\text{RE}}$
Channel 6
6B−
6B+

7A
7DE/$\overline{\text{RE}}$
Channel 7
7B−
7B+

8A
8DE/$\overline{\text{RE}}$
Channel 8
8B−
8B+

INV/$\overline{\text{NON}}$

SE   LVD

9DE/$\overline{\text{RE}}$

9DEb

9REb

9A

9DEb
9DEa

9REb
9REa

9DEa

9REa

9B−

9B+

3
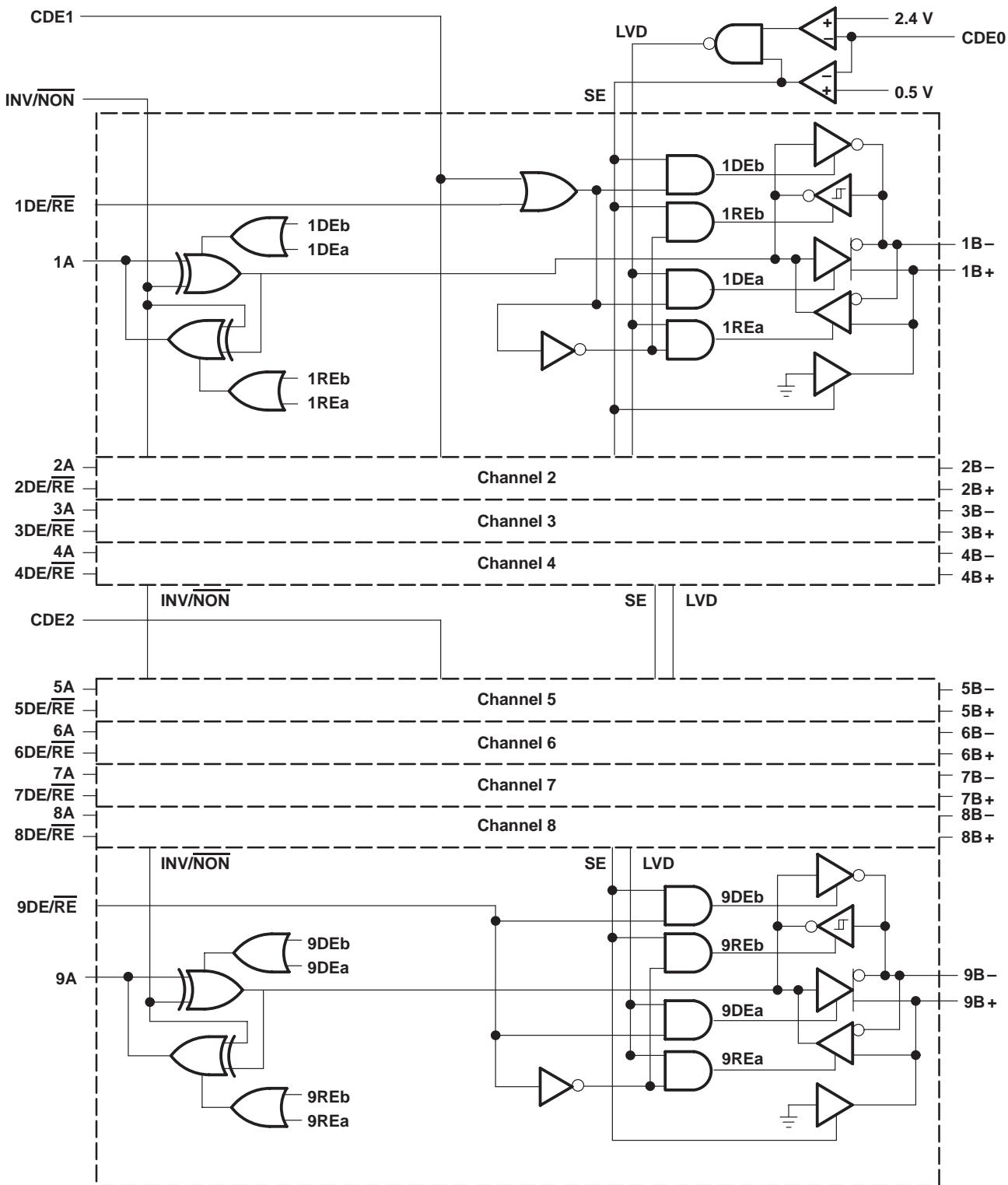
logic diagrams and function tables

Function Table

Inputs			Outputs		
(B+ – B–)	DE/$\overline{\text{RE}}$	A	B+	B–	A
$V_{ID} \geq 30$ mV	L	NA	Z	Z	L
-30 mV $< V_{ID} < 30$ mV	L	NA	Z	Z	?
V_{ID} -30 mV	L	NA	Z	Z	H
Open circuit	L	NA	Z	Z	?
NA	H	L	H	L	Z
NA	H	H	L	H	Z

Figure 1. Inverting LVD Transceiver
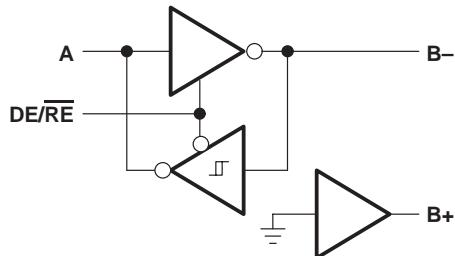
Function Table

Inputs			Outputs		
B–	DE/$\overline{\text{RE}}$	A	B+	B–	A
H	L	NA	L	Z	L
L	L	NA	L	Z	H
Open circuit	L	NA	L	Z	?
NA	H	L	L	H	Z
NA	H	H	L	L	Z

Figure 2. Inverting Single-Ended Transceiver
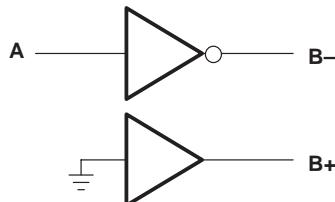
Function Table

Input	Outputs	
A	B+	B–
L	L	H
H	L	L

Figure 3. Inverting Single-Ended Driver
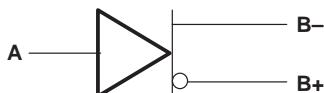
Function Table

Input	Outputs	
A	B+	B–
L	H	L
H	L	H

Figure 4. Inverting LVD Driver

TEXAS
INSTRUMENTS

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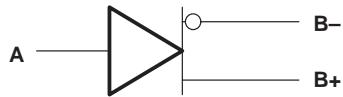
Function Table

Input	Outputs	
A	B+	B−
L	L	H
H	H	L

Figure 5. Non-Inverting LVD Driver
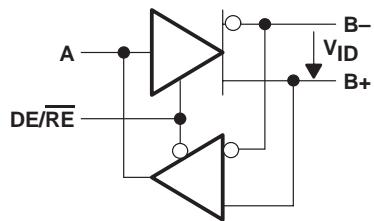
Function Table

Inputs			Outputs		
(B+ − B−)	DE/$\overline{\text{RE}}$	A	B+	B−	A
$V_{ID} \geq 30$ mV	L	NA	Z	Z	H
−30 mV < V_{ID} < 30 mV	L	NA	Z	Z	?
$V_{ID} \leq -30$ mV	L	NA	Z	Z	L
Open circuit	L	NA	Z	Z	?
NA	H	L	L	H	Z
NA	H	H	H	L	Z

Figure 6. Non-Inverting LVD Transceiver
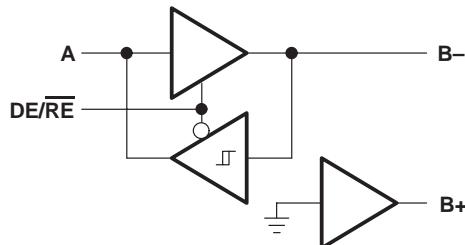
Function Table

Inputs			Outputs		
B−	DE/$\overline{\text{RE}}$	A	B+	B−	A
H	L	NA	L	Z	H
L	L	NA	L	Z	L
Open Circuit	L	NA	L	Z	?
NA	H	L	L	L	Z
NA	H	H	L	H	Z

Figure 7. Non-Inverting Single-Ended Transceiver
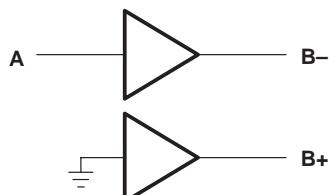
Function Table

Input	Outputs	
A	B+	B−
L	L	L
H	L	H

Figure 8. Non-Inverting Single-Ended Driver

Control Inputs	
CDE0	0.7 V < V_I < 1.9 V
INV/NON	L
CDE1	L
CDE2	L

(a)

Control Inputs	
CDE0	0.7 V < V_I < 1.9 V
INV/NON	L
CDE1	L
CDE2	H

(b)

Control Inputs	
CDE0	0.7 V < V_I < 1.9 V
INV/NON	L
CDE1	H
CDE2	L

(c)
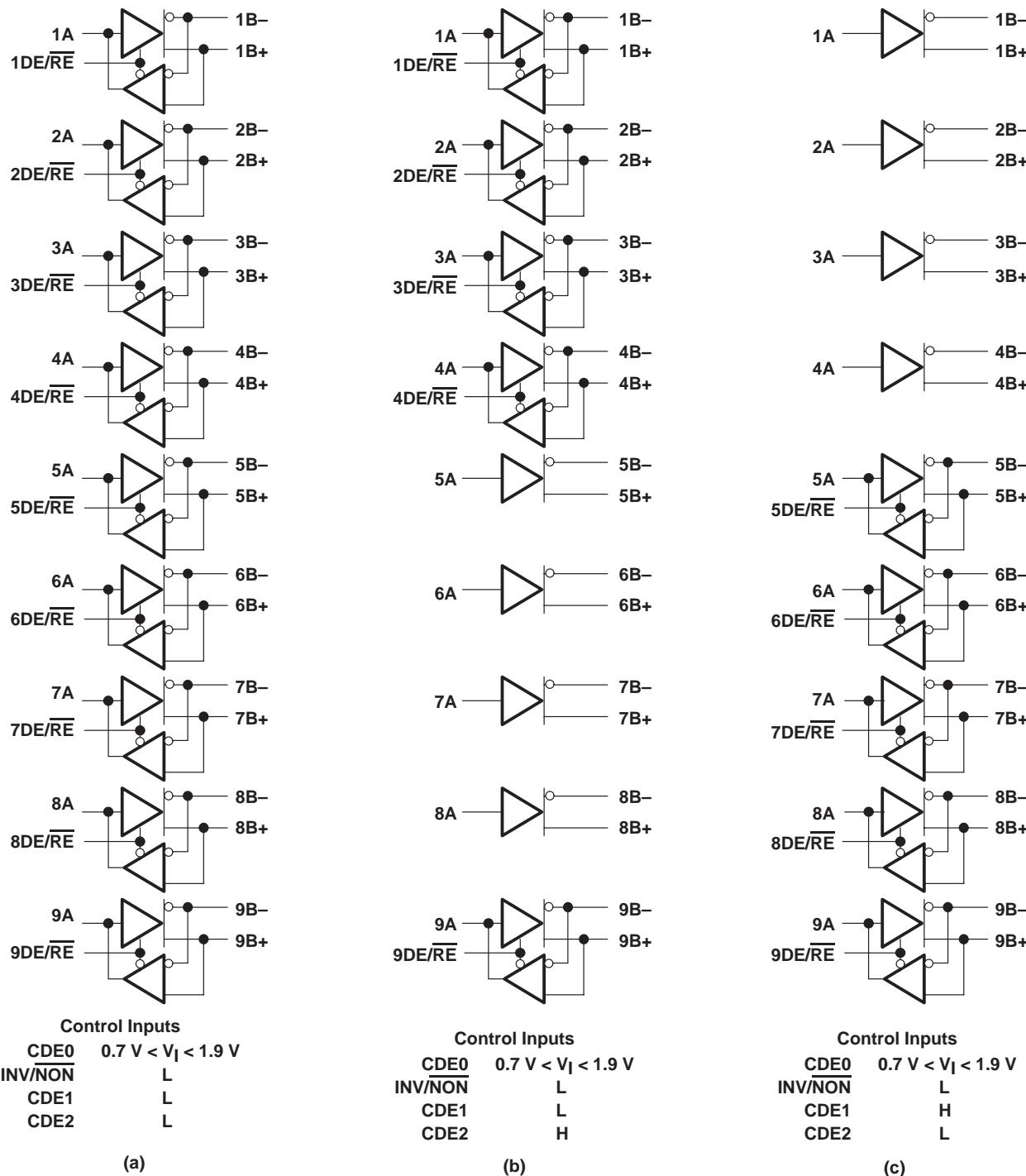
Figure 9. Logic Diagrams

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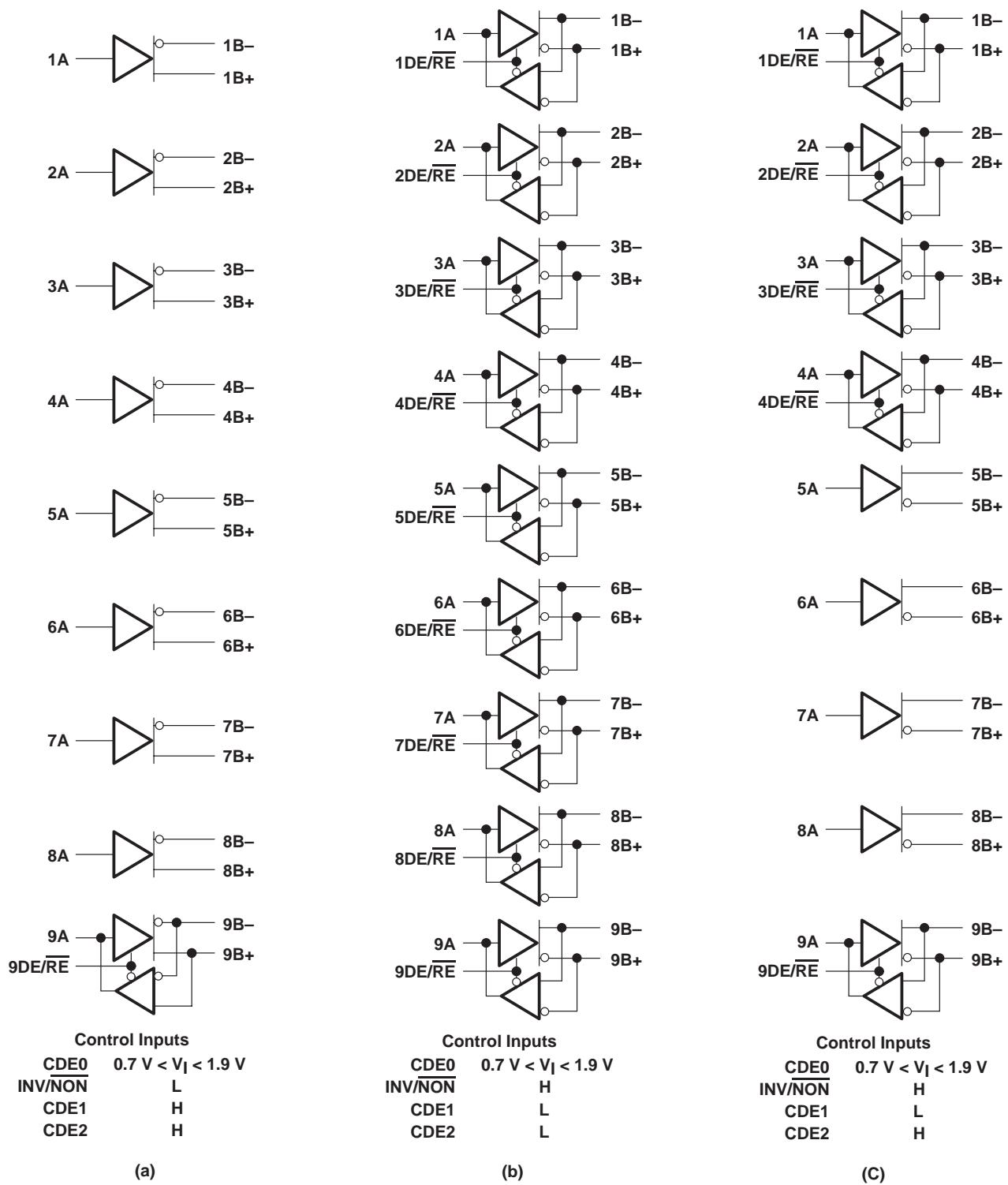
Figure 10. Logic Diagrams

7
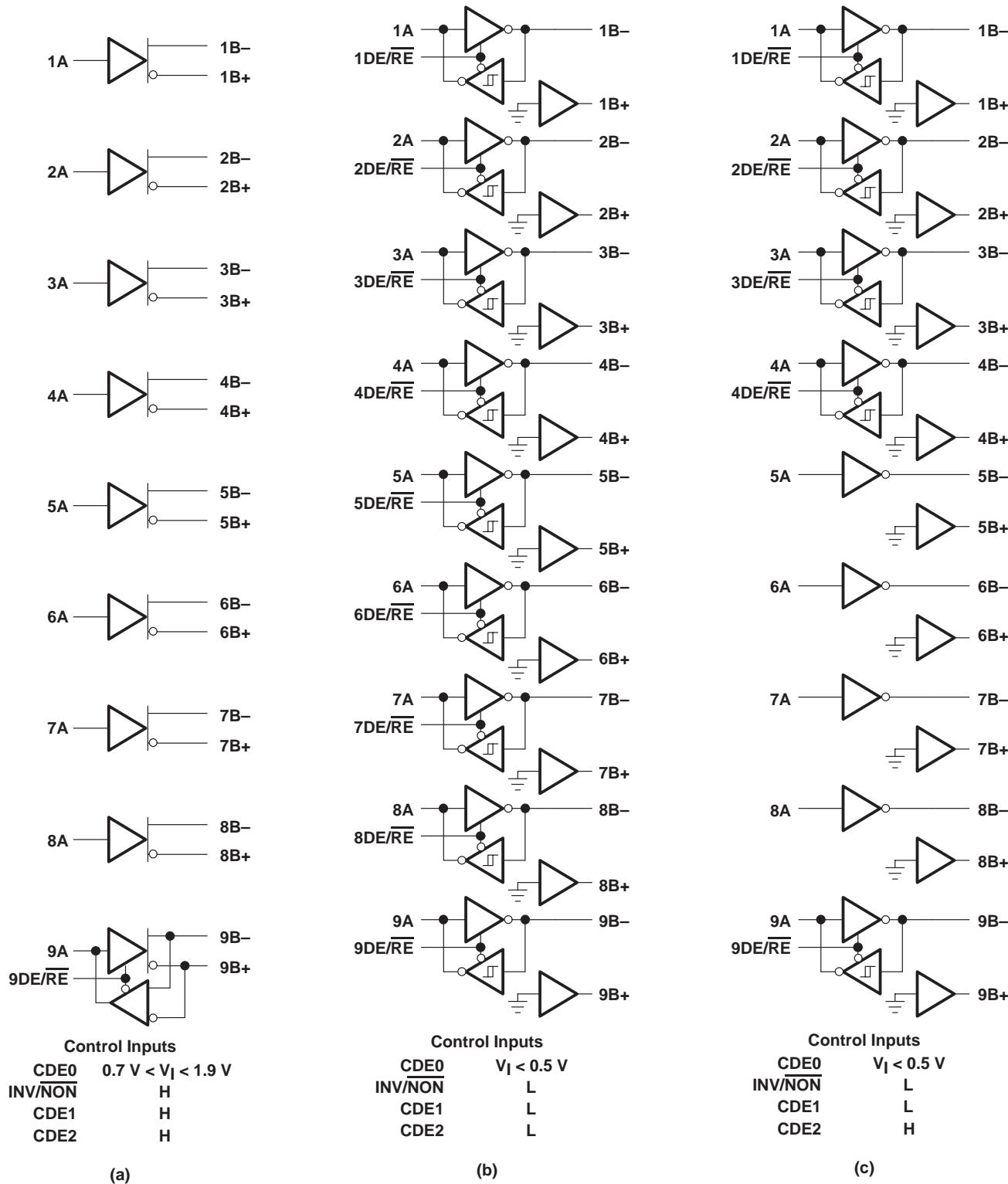
Figure 11. Logic Diagrams

Control Inputs (a)

CDE0	0.7 V < V_I < 1.9 V
INV/NON	H
CDE1	H
CDE2	H

Control Inputs (b)

CDE0	V_I < 0.5 V
INV/NON	L
CDE1	L
CDE2	L

Control Inputs (c)

CDE0	V_I < 0.5 V
INV/NON	L
CDE1	L
CDE2	H

Control Inputs

CDE0	$V_I < 0.5$ V
INV/$\overline{\text{NON}}$	L
CDE1	H
CDE2	L

(a)

Control Inputs

CDE0	$V_I < 0.5$ V
INV/$\overline{\text{NON}}$	L
CDE1	H
CDE2	H

(b)

Control Inputs

CDE0	$V_I < 0.5$ V
INV/$\overline{\text{NON}}$	H
CDE1	L
CDE2	L

(c)
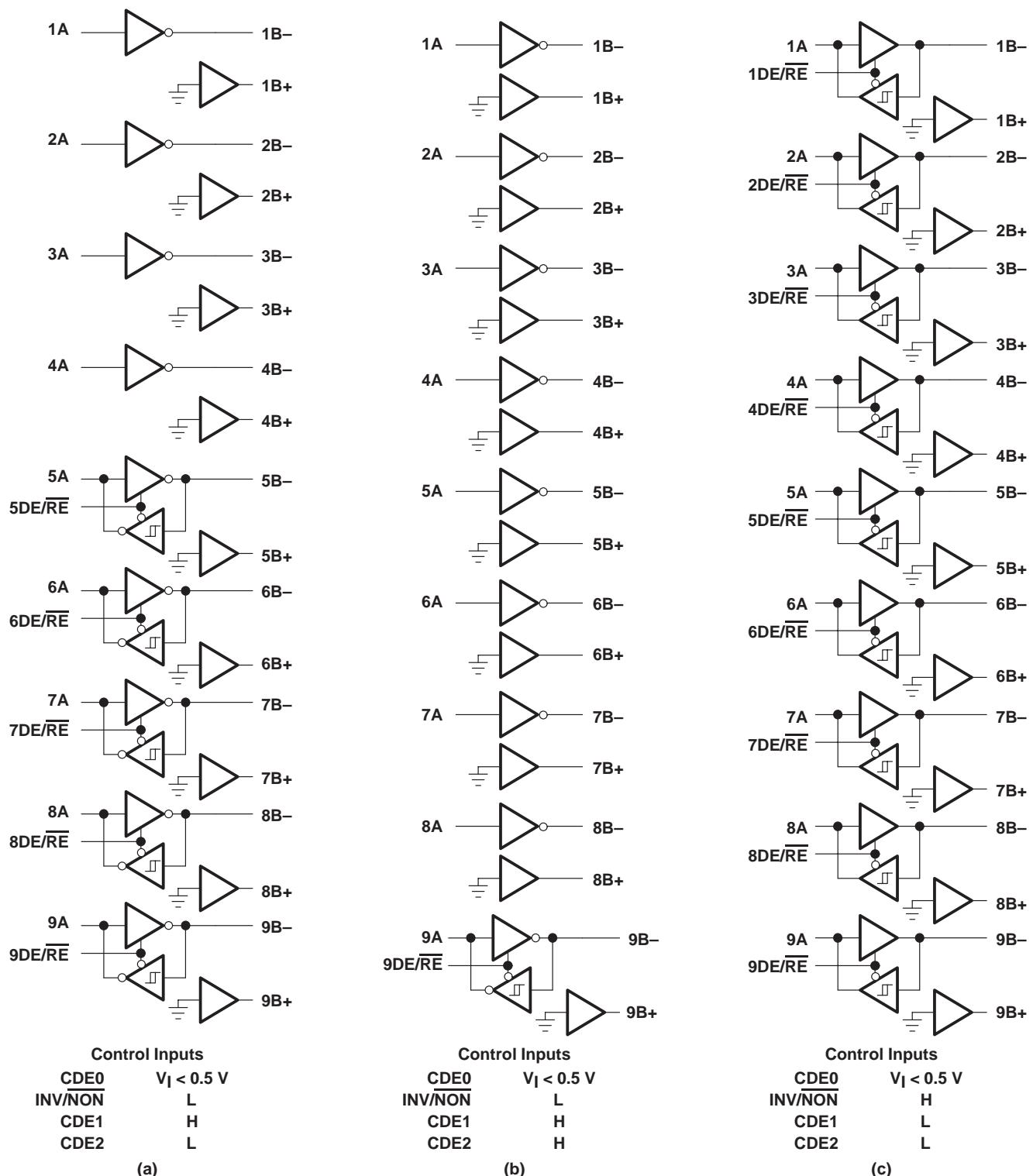
Figure 12. Logic Diagrams

Control Inputs (a)

CDE0	$V_I < 0.5\ V$
INV/NON	H
CDE1	L
CDE2	H

Control Inputs (b)

CDE0	$V_I < 0.5\ V$
INV/NON	H
CDE1	H
CDE2	L

Control Inputs (b)

CDE0	$V_I < 0.5\ V$
INV/NON	H
CDE1	H
CDE2	H
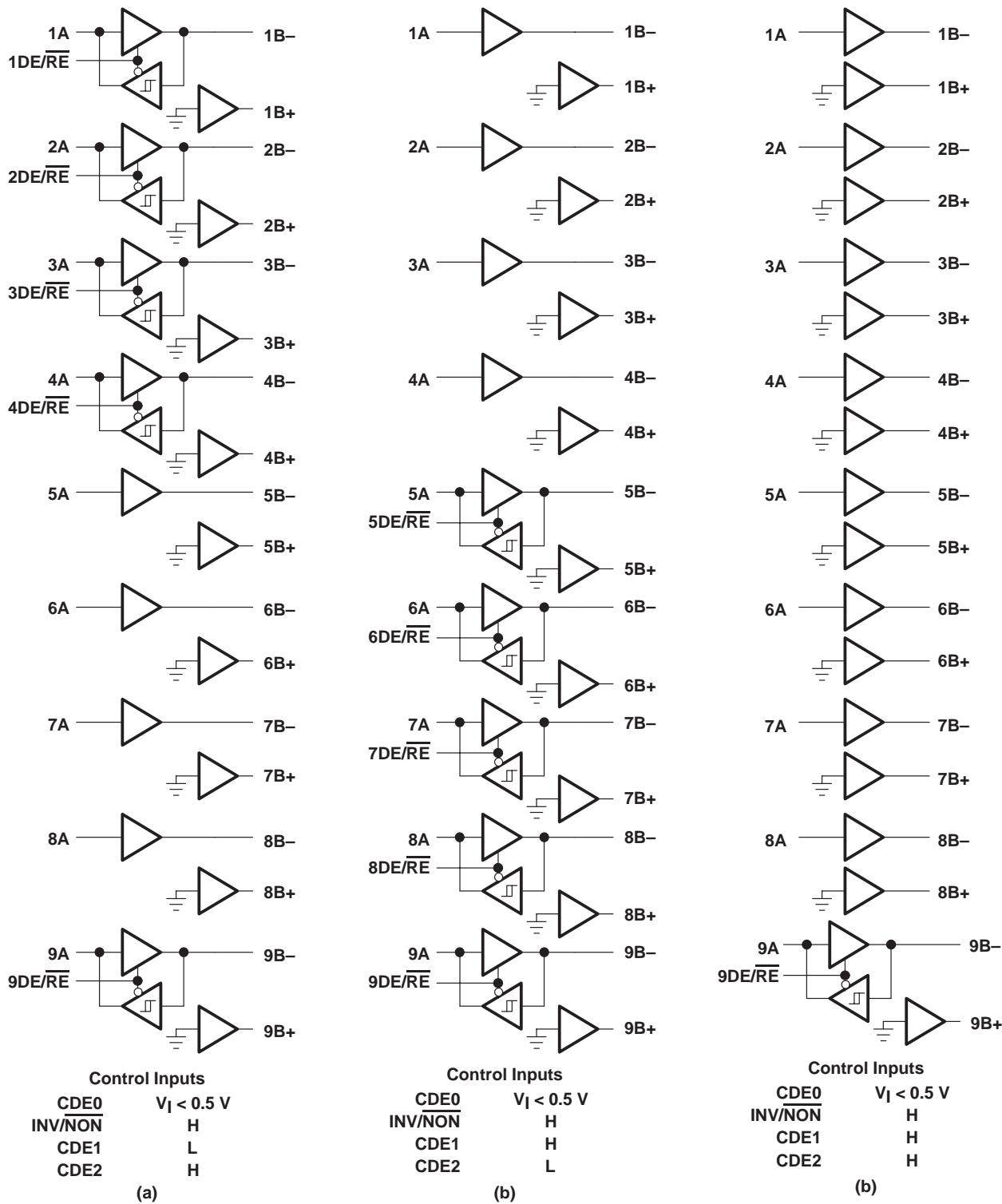
Figure 13. Logic Diagrams

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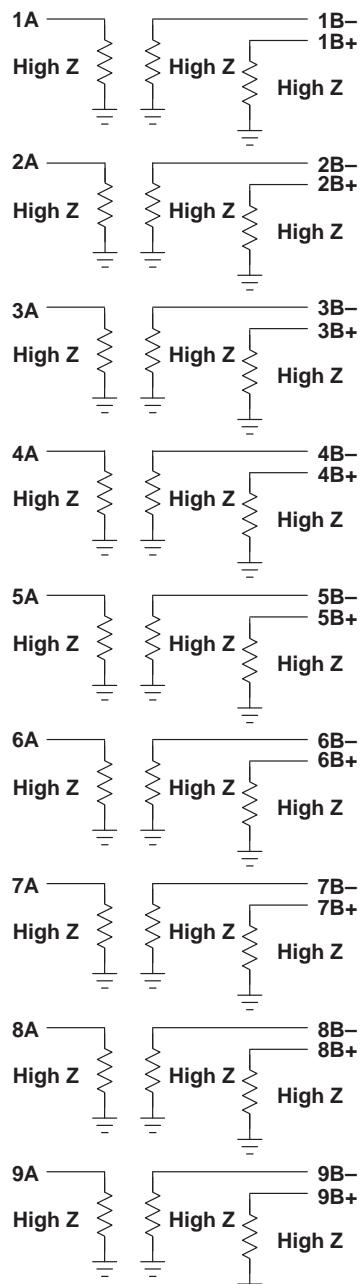
Figure 14. Logic Diagrams

input and output equivalent schematic diagrams

CDE1, CDE2, DE/$\overline{\text{RE}}$ Inputs

CDE0 and INV/$\overline{\text{NON}}$ Inputs

B+ Input

B– Input

A Input and Output
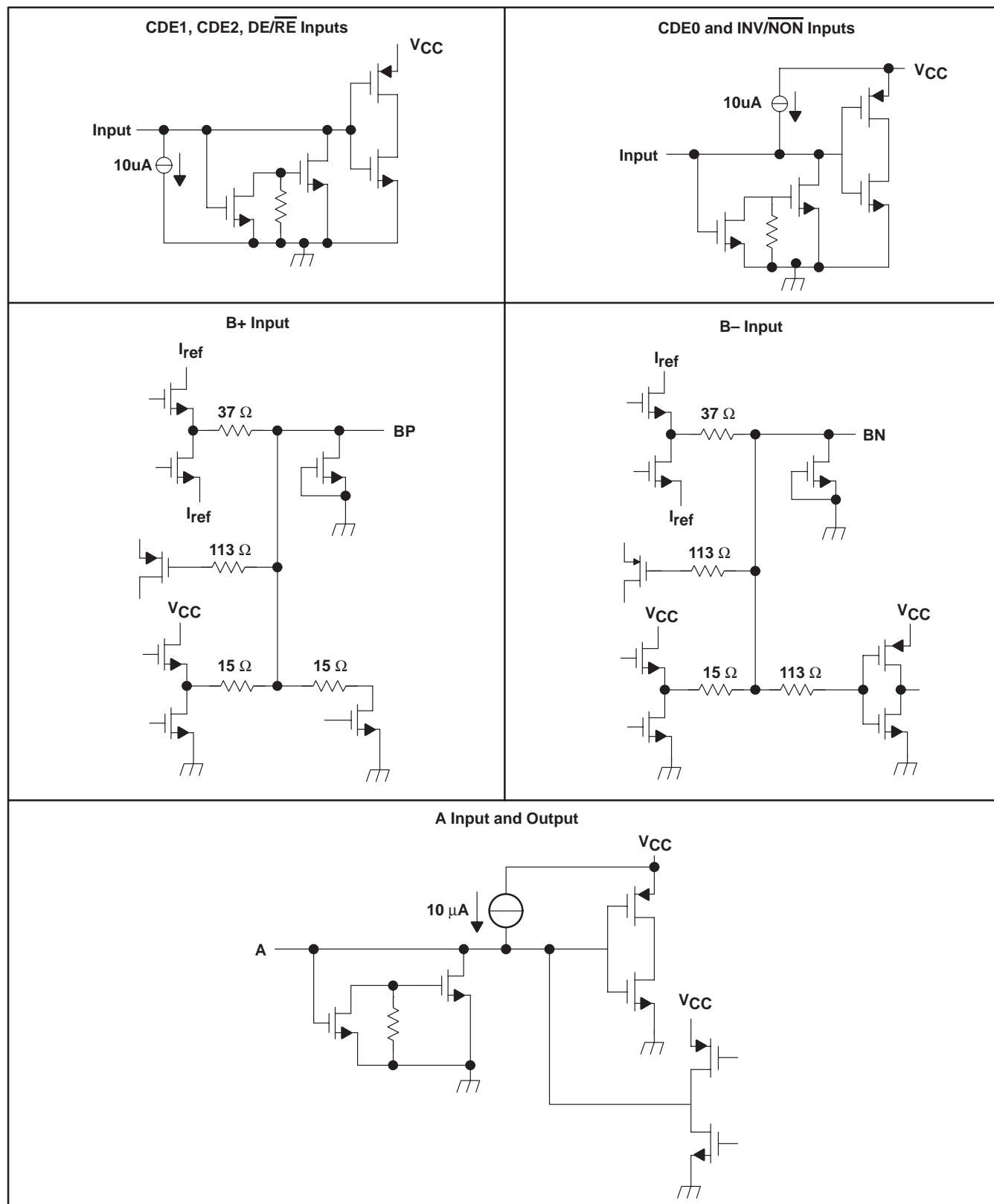
Terminal Functions

TERMINAL		Logic Level	I/O	Termination	DESCRIPTION
NAME	NO.				
1A – 9A	4,6,8,10, 19,21,23, 25,27	TTL	I/O	Pull up	1A – 9A carry data to and from the communication controller.
1B– – 9B–	29,31,33, 35,37,46,4 8,50,52	LVD or TTL	I/O	NA	1B– to 9B– are the digital signals to and from the data bus. When INV/$\overline{\text{NON}}$ is low, these terminals are inverting. When INV/$\overline{\text{NON}}$ is high, these terminals are non-inverting.
1B+ – 9B+	30,32,34, 36,38,47, 49,51,53	LVD or GND	I/O	NA	When in LVD mode, these terminals are inverting when INV/$\overline{\text{NON}}$ is low and non-inverting when INV/$\overline{\text{NON}}$ is high. When in single-ended mode, these terminals become a ground connection through a transistor.
CDE0	54	Trinary	Input	Pull up	CDE0 is the common driver enable 0. When nDE/$\overline{\text{RE}}$ is high and the input is less than 0.4 V, CDE0 input signal enables all drivers in single-ended mode. When nDE/$\overline{\text{RE}}$ is high and the input is between 0.7 V and 1.8 V, CDE0 input signal enables all drivers in LVD mode. All drivers are disabled when the input is greater than 2.4 V.
CDE1	55	TTL	Input	Pull down	CDE1 is the common driver enable 1. When CDE1 is high, drivers 1 – 4 are enabled
CDE2	56	TTL	Input	Pull down	CDE2 is the common driver enable 2. When CDE2 is high, drivers 5 to 8 are enabled.
1DE/$\overline{\text{RE}}$ – 9DE/$\overline{\text{RE}}$	5,7,9,11, 20,22,24, 26,28	TTL	Input	Pull down	1DE/$\overline{\text{RE}}$ – 9DE/$\overline{\text{RE}}$ are direction controls that transmit data to the bus when it is high and CDE0 is below 2.2 V. Data is received from the bus when 1DE/$\overline{\text{RE}}$ – 9DE/$\overline{\text{RE}}$, CDE1, and CDE2 are low.
GND	2,3,13,14, 15,16,17, 40,41,42, 43,44	NA	Power	NA	GND is the circuit ground.
INV/$\overline{\text{NON}}$	1	TTL	Input	Pull up	A high-level input to INV/$\overline{\text{NON}}$ inverts the logic to and from the A terminals. (i.e., the voltage at A terminal and the corresponding B– terminal are in phase.)
V$_{\text{CC}}$	12,18,39, 45	NA	Power	NA	Supply voltage

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . −0.5 V to 7 V
Input voltage range, V_I (A, INV/$\overline{NON}$, CDE0) . . . . −0.5 V to V_{CC} + 0.5 V
(DE/$\overline{RE}$, B+, B–, CDE1, CDE2) . . . . −0.5 V to 5.25 V
Continuous total power dissipation . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values are with respect to GND unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DGG	978 mW	10.8 mW/°C	492 mW

recommended operating conditions (see Figure 15)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}				0.7 V_{CC}	V
Low-level input voltage, V_{IL}		0.3 V_{CC}			V
Differential input voltage, $|V_{ID}|$	Differential receiver	0.03		3.6	V
Common-mode input voltage, V_{IC}		0.7		1.8	V
Differential output voltage bias, $V_{OD(bias)}$	Differential	−100		−125	mV
High-level output current, I_{OH}	Single-ended driver			−4	mA
	Receiver			−2	
Low-level output current, I_{OL}	Single-ended driver			48	mA
	Receiver			2	
Differential load impedance, Z_L		40		65	Ω
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	CDE1 and CDE2	V_{IH} = 3.3 V				50	μA
		INV/$\overline{NON}$					−50	
I_{IL}	Low-level input current	CDE1 and CDE2	V_{IL} = 1.6 V				−50	μA
		INV/$\overline{NON}$					−50	
I_{CC}	Supply current		Disabled				7	mA
			LVD drivers enabled,	No load			26	
			Single-ended drivers enabled,	No load			20	
			LVD receivers enabled,	No load			26	
			Singled-ended receivers enabled,	No load			7	
C_I	Input capacitance	Bus terminal	V_I = 0.2 sin (2 π (1E06)t) + 0.5 ± 0.01 V			9.5		pF
ΔC_I	Difference in input capacitance between B+ and B−						0.2	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

DIFFSENS (CDE0) receiver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT1}	Input threshold voltage		0.4	0.6	0.7	V
V_{IT2}	Input threshold voltage		1.8	2.1	2.4	
I_I	Input current	0 V ≤ V_I ≤ 2.7 V,			−50	μA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

LVD driver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
$V_{OD(H)}$	Driver differential high-level output voltage		$V_{I(1)} = 0.96$ V, $V_{I(2)} = 0.53$ V, See Figure 16	270	460	780	mV
				$0.69|V_{OD(L)}|+ 50$		$1.45|V_{OD(L)}|- 65$	
			$V_{I(1)} = 1.96$ V, $V_{I(2)} = 1.53$ V, See Figure 16	270	500	780	
				$0.69|V_{OD(L)}|+ 50$		$1.45|V_{OD(L)}|- 65$	
$V_{OD(L)}$	Driver differential low-level output voltage		$V_{I(1)} = 0.96$ V, $V_{I(2)} = 0.53$ V, See Figure 16	−260	−400	−640	mV
			$V_{I(1)} = 1.96$ V, $V_{I(2)} = 1.53$ V, See Figure 16	−260	−400	−640	
$V_{OC(SS)}$	Steady-state common-mode output voltage			1.1	1.2	1.5	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		$V_{I(1)} = 1.41$ V, $V_{I(2)} = 0.99$ V, See Figure 17		±50	±120	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				80	150	mV
I_{IH}	High-level input current	A	$V_{IH} = 3.3$ V	−7			µA
		DE/$\overline{RE}$	$V_{IH} = 3.3$ V			50	
I_{IL}	Low-level input current	A	$V_{IL} = 1.6$ V			−30	µA
		DE/$\overline{RE}$	$V_{IL} = 1.6$ V	8			
$I_{O(OFF)}$	Power-off output current		$V_{CC} = 0$, 0 V $\leq V_O \leq 2.5$ V			±1	µA
I_{OS}	Short-circuit output current		0 V $\leq V_O \leq 2.5$ V			±24	mA
I_{OZ}	High-impedance output current		$V_O = 0$ or 2.5 V			±1	µA

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

LVD driver switching characteristics over recommended operating conditions (unless otherwise noted) (See Figure 16)

PARAMETER		TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	$V_{CC}= 5$ V, $V_{I1}= 1.41$ V, $V_{I2}= 0.99$ V, $T_A = 25°C$	2.9	5.8	8.8	ns
t_{PHL}	Propagation delay time, high-to-low level output		4.4	5.5	6.5	ns
t_r	Differential output signal rise time		1	3	6	ns
t_f	Differential output signal fall time		1	3	6	ns
$t_{sk(p)}$	Pulse skew ($|t_{PHL} - t_{PLH}|$)			0.4		ns
$t_{sk(lim)}$	Skew limit[‡]				5.9	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output	$V_{I1}= 1.41$ V, $V_{I2}= 0.99$ V, See Figure 18			20	ns
t_{en}	Enable time, receiver to driver				33	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ $t_{sk(lim)}$ is the maximum delay time difference between any two drivers on any two devices operating at the same supply voltage and the same ambient temperature.

single-ended driver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	B– output	$I_{OH} = -4$ mA,	See Figure 19	2.5		3.24	V
			$I_{OH} = 0$ mA				3.7	V
V_{OL}	Low-level output voltage	B– output	$V_{CC} = 5$ V, $T_A = 25°C$	$I_{OL} = 48$ mA,			0.5	V
			$I_{OL} = 24$ mA				0.5	V
		B+	$I_{OL} = -3$ mA				−0.5	V
			$I_{OL} = 3$ mA				0.5	
I_{IH}	High-level input current	A	$V_{IH} = 3.3$ V		−7			μA
		DE/$\overline{RE}$					50	
I_{IL}	Low-level input current	A	$V_{IL} = 1.6$ V				−30	μA
		DE/$\overline{RE}$			8			
$I_{O(OFF)}$	Power-off output current	B–	$V_{CC} = 0$,	0 V $\leq V_O \leq 5.25$ V			±1	μA
I_{OZ}	High-impedance output current		$V_O = 0$ or V_{CC}				±1	μA

single-ended driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	$V_{CC} = 5$ V, $T_A = 25°C$, See Figure 19	9.6	12	14.2	ns
t_{PHL}	Propagation delay time, high-to-low level output		8.1	11.5	14.7	ns
t_r	Differential output signal rise time		3	4	6	ns
t_f	Differential output signal fall time		4.7	6.5	8.2	ns
$t_{sk(p)}$	Pulse skew ($|t_{pHL} - t_{pLH}|$)			0.5		ns
$t_{sk(lim)}$	Skew limit[‡]				5.1	ns
t_{en}	Enable time, receiver to driver	See Figure 20			50	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output				30	ns

[†] All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
[‡] $t_{sk(lim)}$ is the maximum delay time difference between any two drivers on any two devices operating at the same supply voltage and the same ambient temperature.

**LVD receiver electrical characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 21				30	mV
V_{IT-}	Negative-going differential input voltage threshold					−30	mV
V_{OH}	High-level output voltage	$I_{OH} = -2$ mA		3.7			V
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA				0.5	V
I_I	Input current, B+ or B–	$V_I = 0$ V to 2.5 V				±1	μA
$I_{I(OFF)}$	Power-off Input current, B+ or B–	$V_{CC} = 0$,	$V_I = 0$ V to 2.5 V			±1	μA
I_{IH}	High-level input current, DE/$\overline{RE}$	$V_{IH} = 3.3$ V				50	μA
I_{IL}	Low-level input current, DE/$\overline{RE}$	$V_{IL} = 1.6$ V		8			μA
I_{OZ}	High-impedance output current	$V_O = 0$ or V_{CC}				±30	μA

LVD receiver switching characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	V_{CC} = 5 V, T_A = 25°C, See Figure 21	6	8.9	11.8	ns
t_{PHL}	Propagation delay time, high-to-low level output		7.4	8.4	9.4	ns
$t_{sk(p)}$	Pulse skew ($|t_{pHL} - t_{pLH}|$)			0.5		ns
t_r	Output signal rise time			8.5		ns
t_f	Output signal fall time			3		ns
$t_{sk(lim)}$	Skew limit‡				5.8	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output	See Figure 18			42	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output				20	ns
t_{en}	Enable time, driver to receiver				26	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ $t_{sk(lim)}$ is the maximum delay time difference between any two drivers on any two devices operating at the same supply voltage and the same ambient temperature.

single-ended receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input voltage threshold	B–			1.6	1.9	V
V_{IT-}	Negative-going input voltage threshold	B–			1	1.1	V
V_{OH}	High-level output voltage		I_{OH} = −2 mA	3.7	4.6		V
V_{OL}	Low-level output voltage		I_{OL} = 2 mA		0.3	0.5	V
I_I	Input current	B–	V_I = 0 to V_{CC}			±1	μA
$I_{I(OFF)}$	Power-off Input current	B–	V_{CC} = 0 V, V_I = 0 to 5.25 V			±1	μA
I_{IH}	High-level input current	DE/$\overline{RE}$	V_{IH} = 3.3 V			50	μA
I_{IL}	Low-level input current	DE/$\overline{RE}$	V_{IL} = 1.6 V	8			μA
I_{OZ}	High-impedance output current		V_O = 0 or V_{CC}			−30	μA

single-ended receiver switching characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	$V_{CC} = 5$ V, $T_A = 25°C$, See Figure 22	7.8	8.8	9.8	ns
t_{PHL}	Propagation delay time, high-to-low level output		5.8	7.3	8.8	ns
$t_{sk(p)}$	Pulse skew ($|t_{pHL} - t_{pLH}|$)			1.5		ns
t_r	Output signal rise time			8.3		ns
t_f	Output signal fall time			3.3		ns
$t_{sk(lim)}$	Skew limit†				4	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output	See Figure 20			20	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output				30	ns
t_{en}	Enable time, driver to receiver				48	ns

† $t_{sk(lim)}$ is the maximum delay time difference between any two drivers on any two devices operating at the same supply voltage and the same ambient temperature.

PARAMETER MEASUREMENT INFORMATION
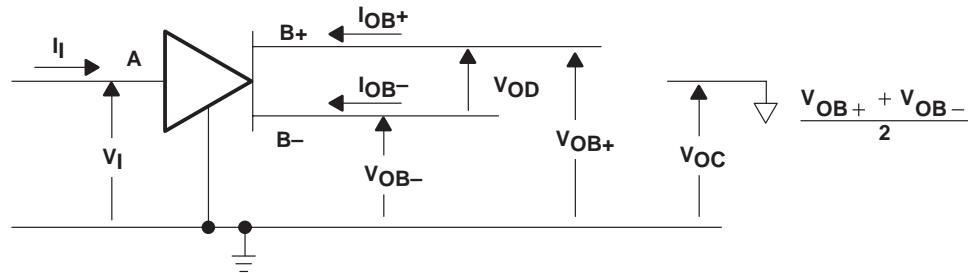
Figure 15. Voltage and Current Definitions
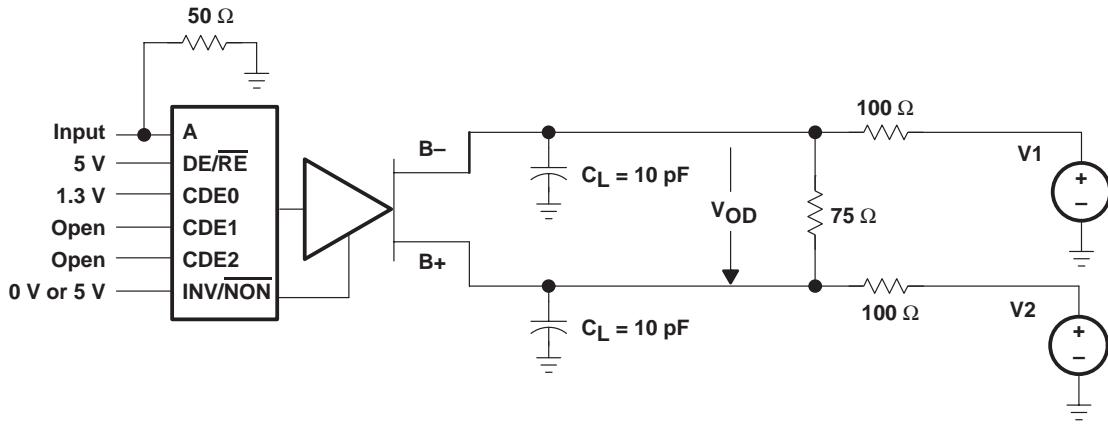
NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulsewidth = 50 ns ± 5 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 16. Differential Output Signal Test Circuit, Timing, and Voltage Definitions

PARAMETER MEASUREMENT INFORMATION
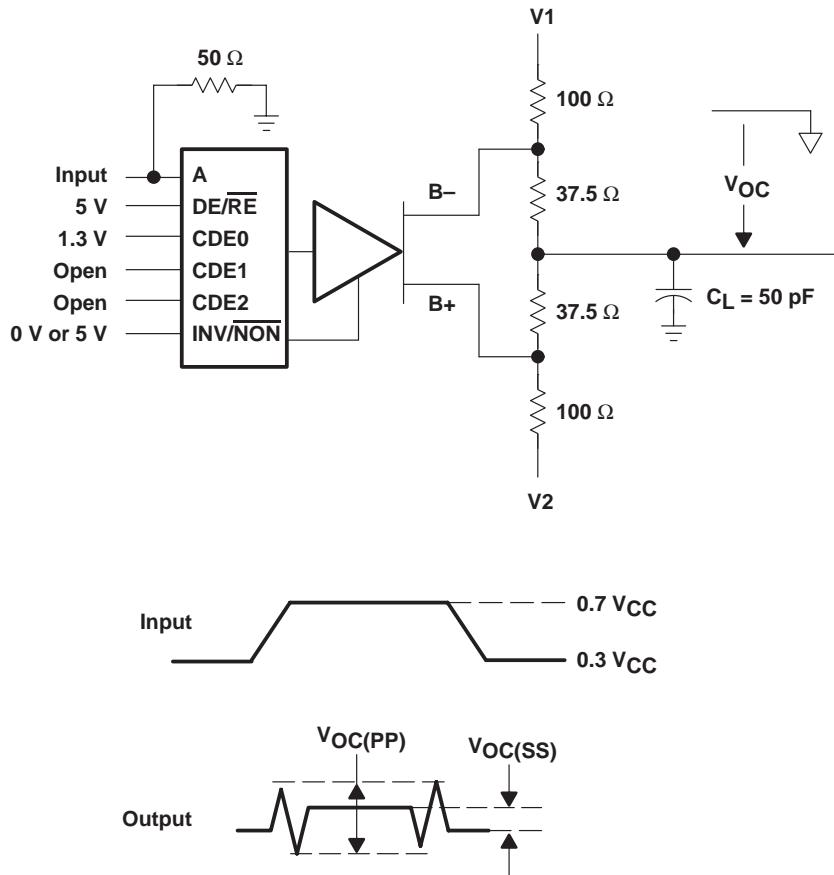
Figure 17. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulsewidth = 50 ns ±5 ns, Z_O = 50 Ω.
   B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.
   C. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS
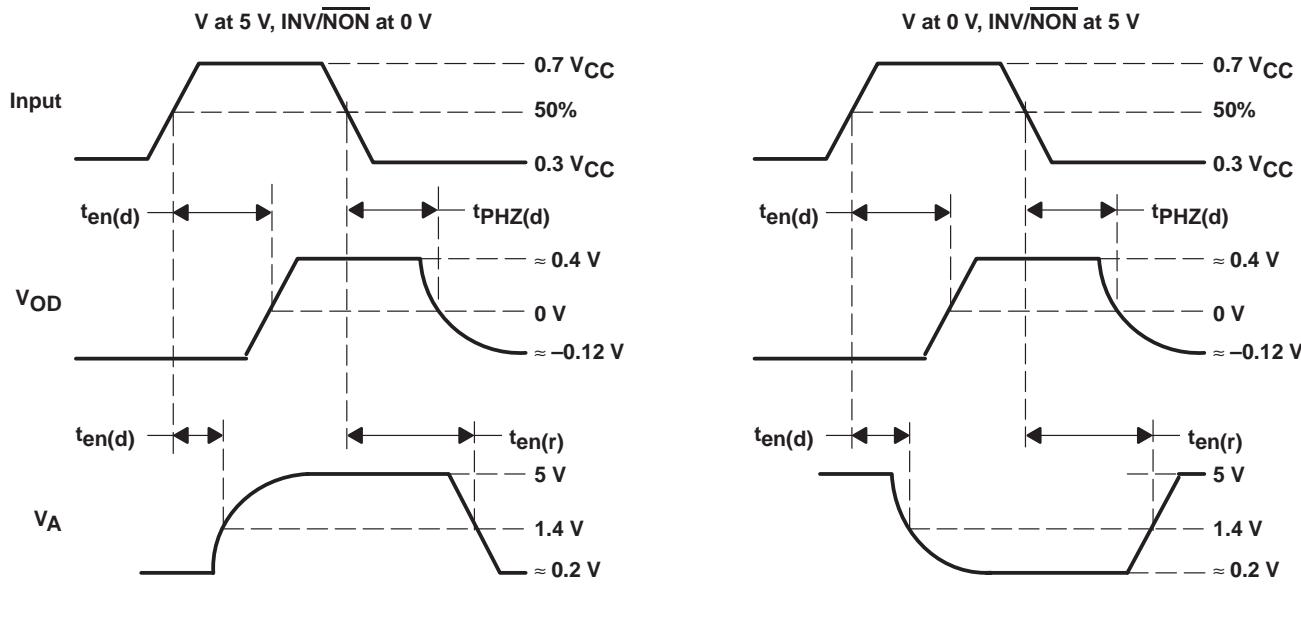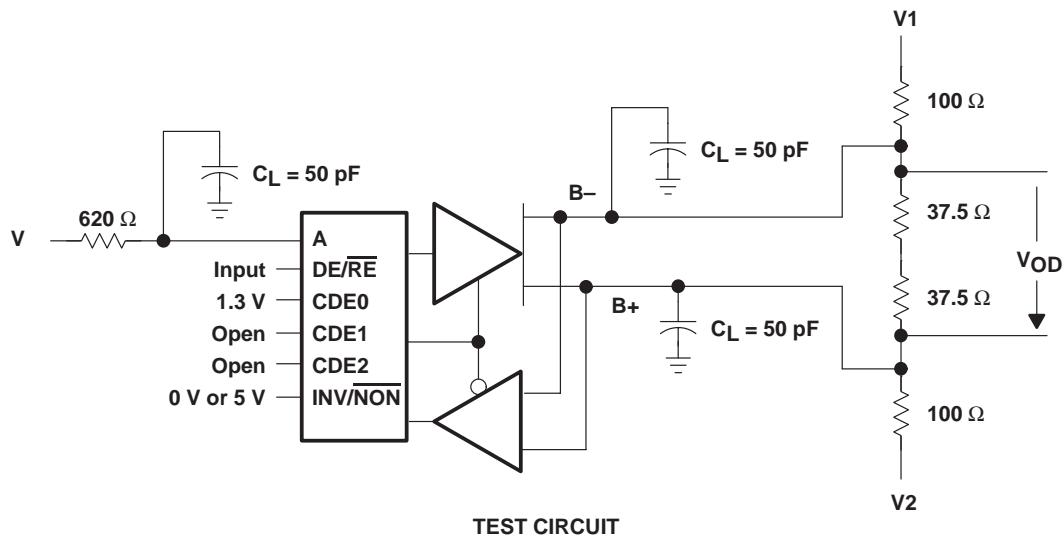
NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 1 Mpps, pulsewidth = 500 ns ±50 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 18. LVD Transceiver Enable and Disable Time Test Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION
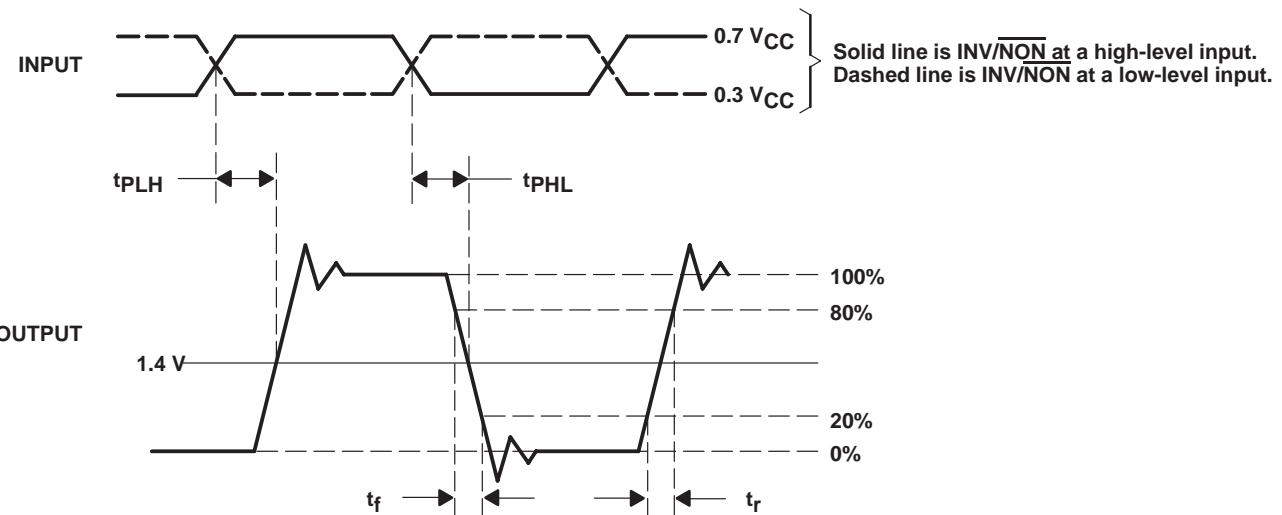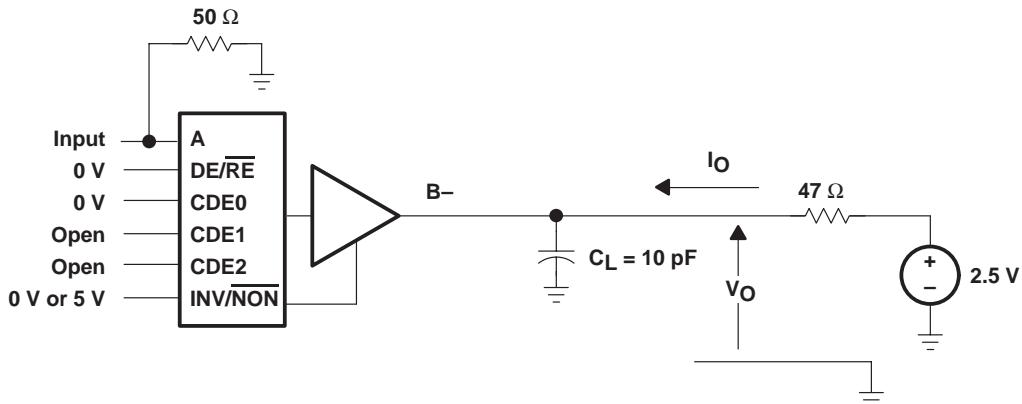
NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulsewidth = 50 ns ±5 ns, $Z_O = 50$ Ω.
B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 19. Single-Ended Driver Switching Test Circuit

PARAMETER MEASUREMENT INFORMATION
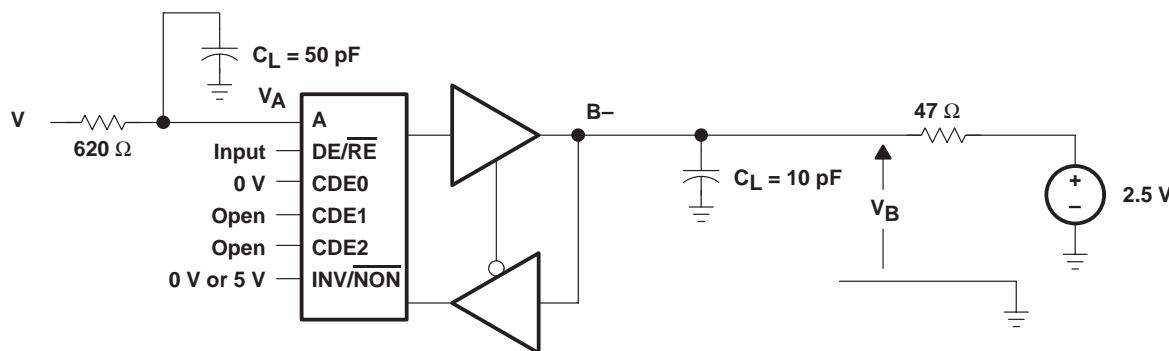
TEST CIRCUIT
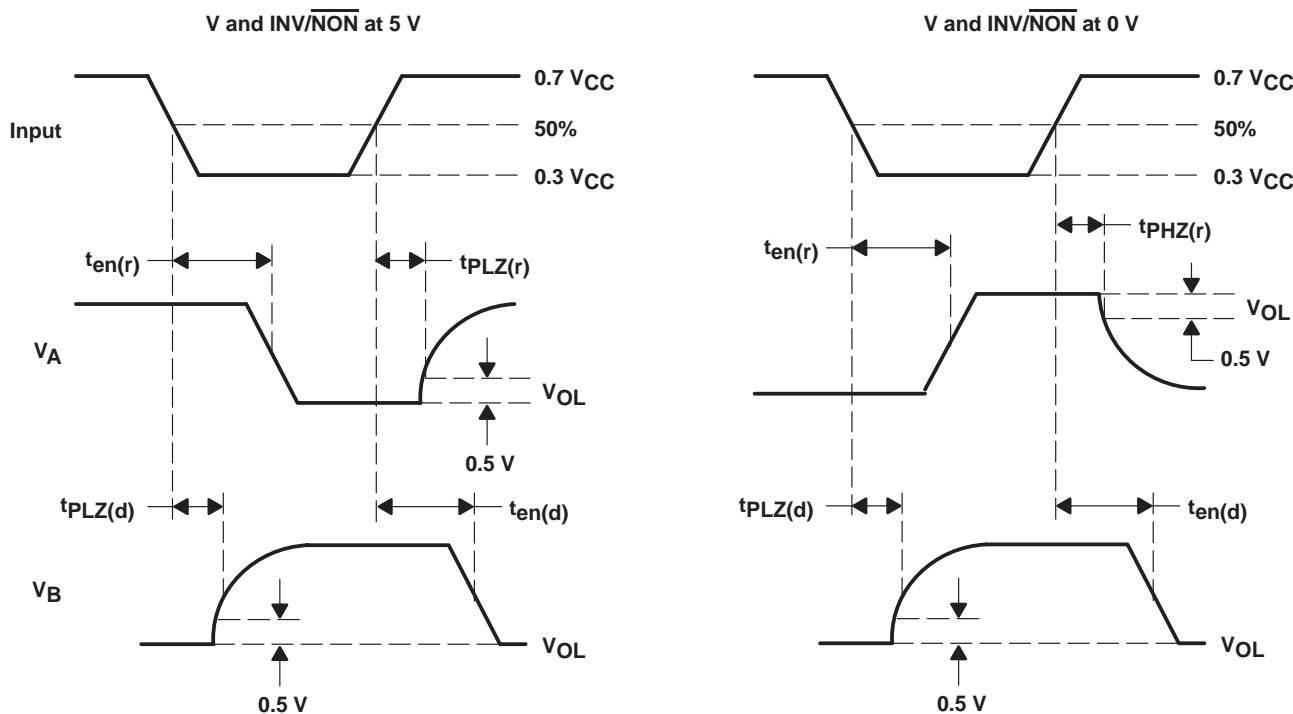
VOLTAGE WAVEFORMS

NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 1 Mpps, pulsewidth = 500 ns ± 50 ns, $Z_O = 50~\Omega$.

      B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 20. Single-Ended Transceiver Enable and Disable Timing Measurements

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PARAMETER MEASUREMENT INFORMATION
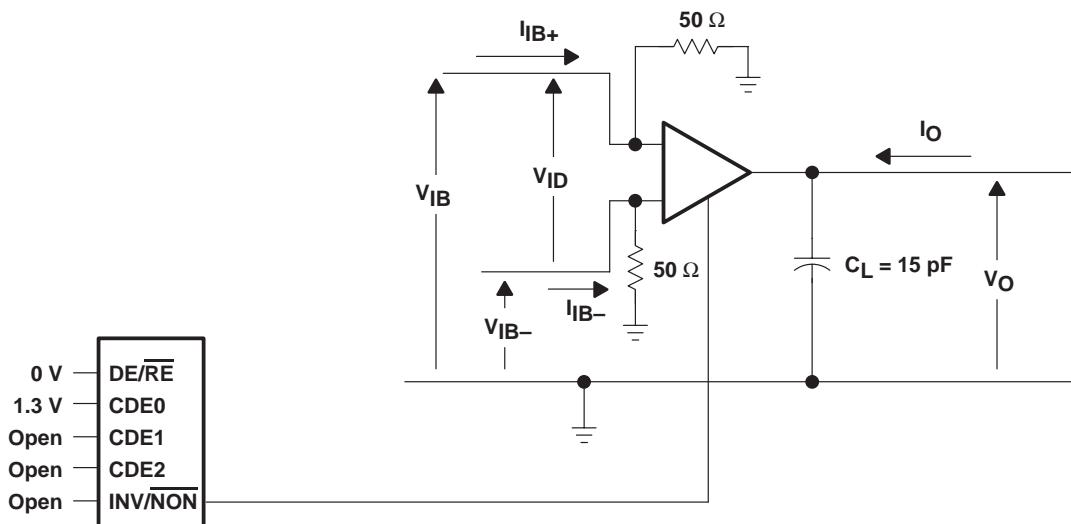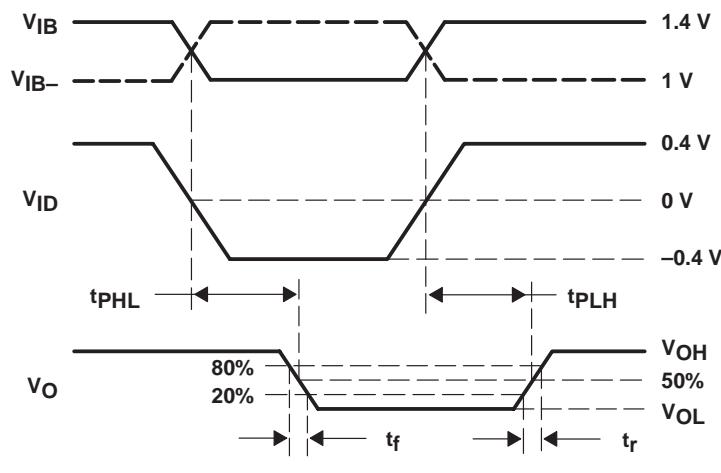
TEST CIRCUIT

VOLTAGE WAVEFORMS

Figure 21. LVD Receiver Switching Characteristic Test Circuit

NOTES: A. Note: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulsewidth = 50 ns ±5 ns, $Z_O = 50$ Ω.
B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

TYPICAL CHARACTERISTICS
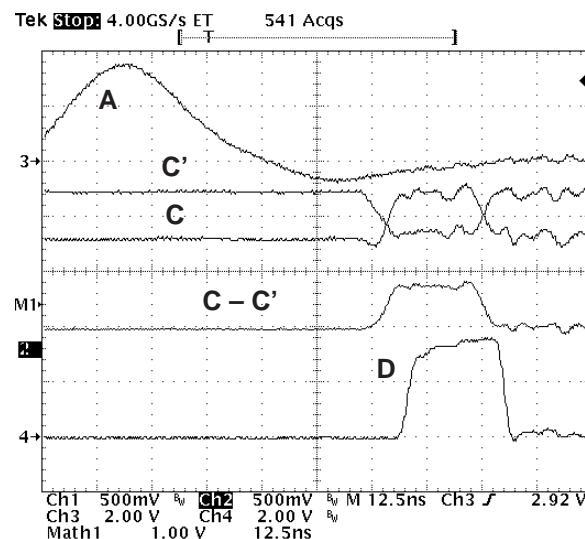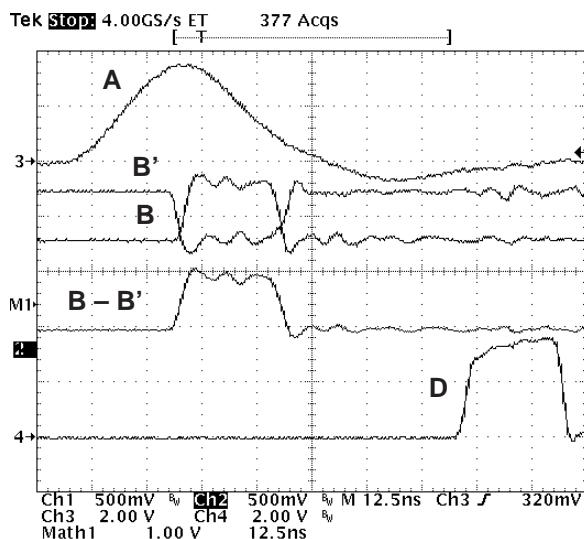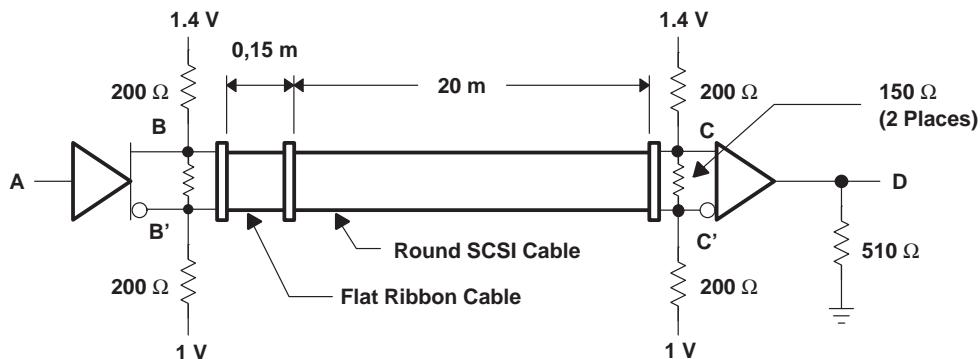
Figure 22. Typical LVD Signals

TYPICAL CHARACTERISTICS
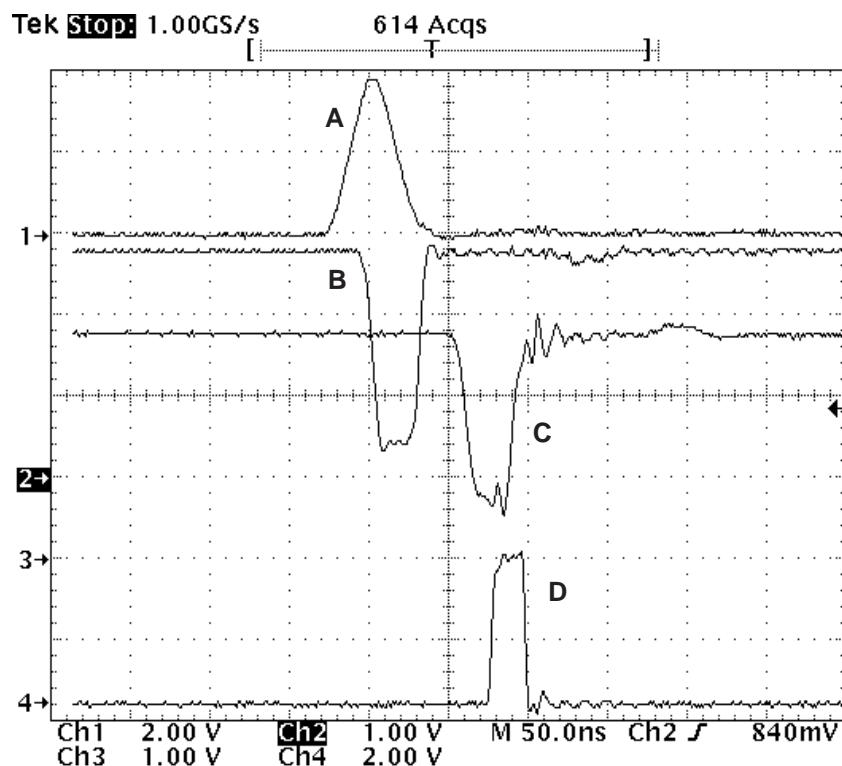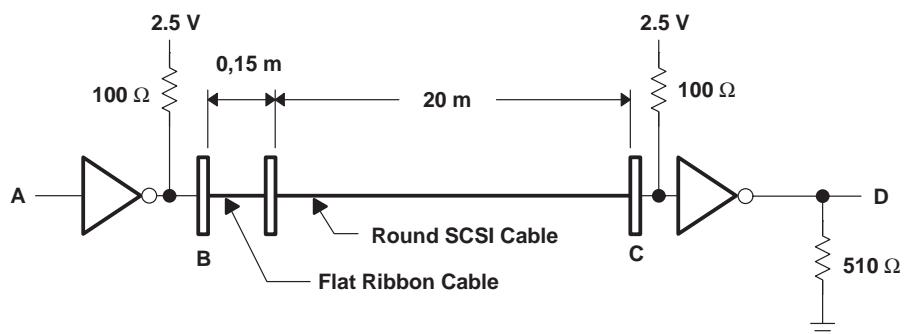
Figure 23. Typical Single-Ended Signals

TYPICAL CHARACTERISTICS

SINGLE-ENDED RECEIVER
HIGH-TO-LOW LEVEL
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 24

SINGLE-ENDED RECEIVER
LOW-TO-HIGH LEVEL
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 25

LVD RECEIVER
HIGH-TO-LOW LEVEL
PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

Figure 26

LVD RECEIVER
LOW-TO-HIGH LEVEL
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 27

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TYPICAL CHARACTERISTICS

SINGLE-ENDED DRIVER
HIGH-TO-LOW LEVEL
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 28

SINGLE-ENDED DRIVER
LOW-TO-HIGH LEVEL
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 29

LVD DRIVER
HIGH-TO-LOW LEVEL
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 30

LVD DRIVER
LOW-TO-HIGH LEVEL
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE
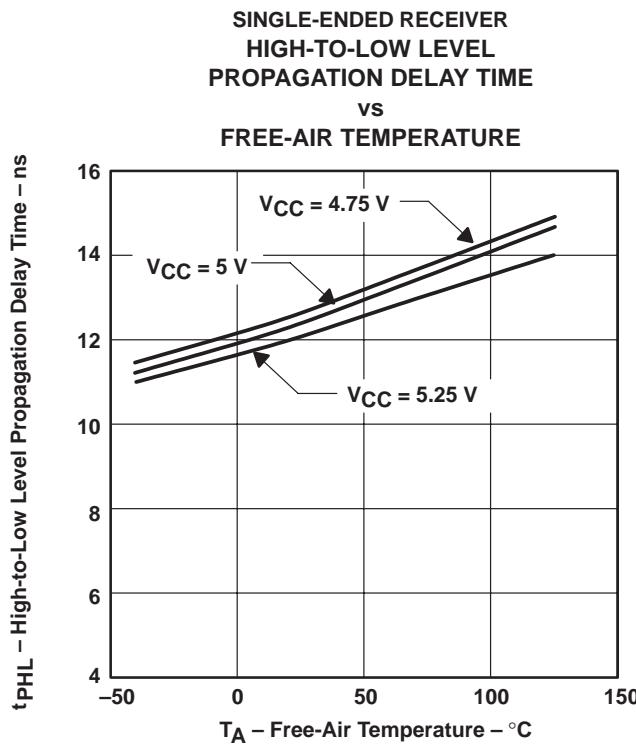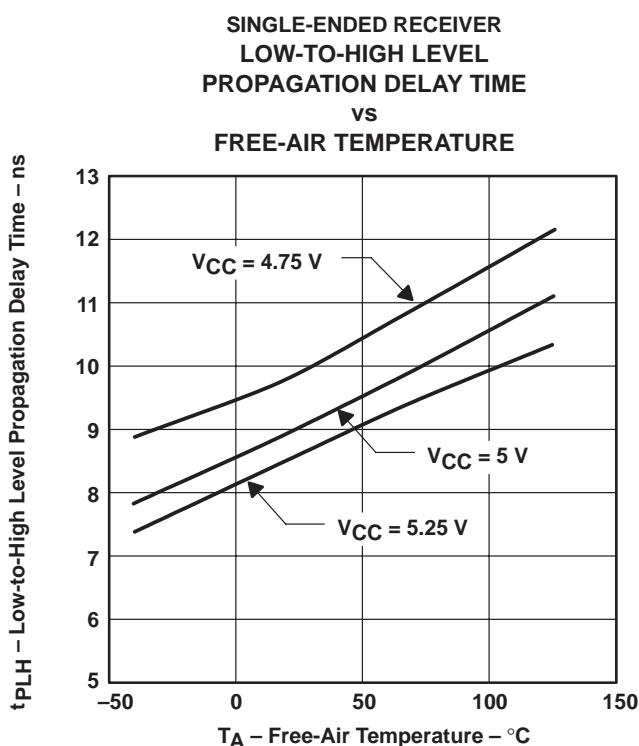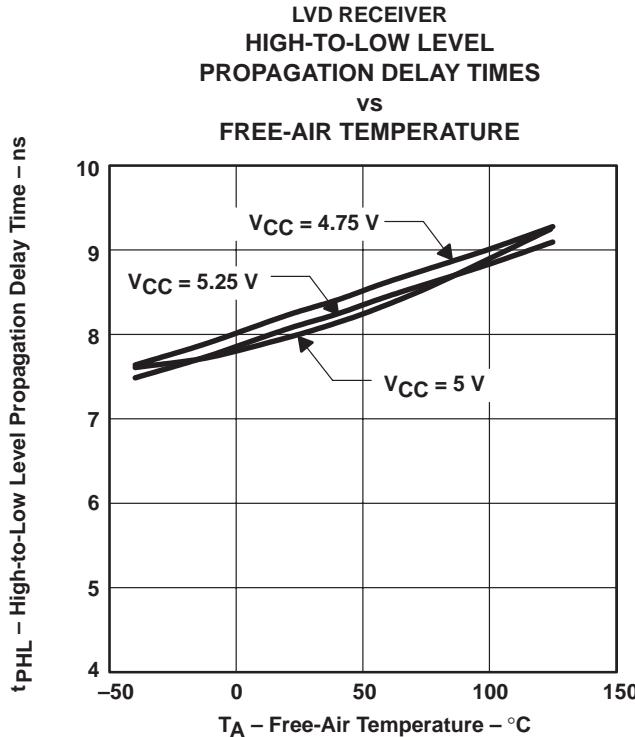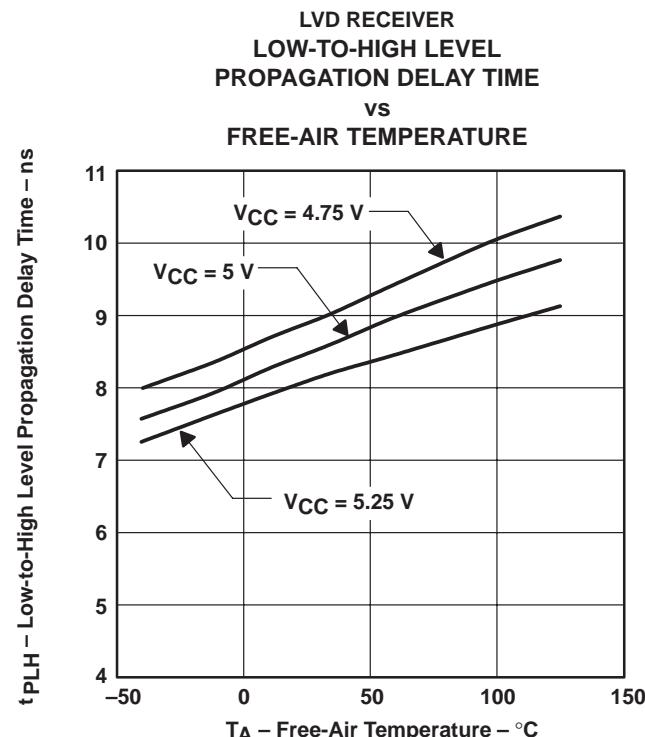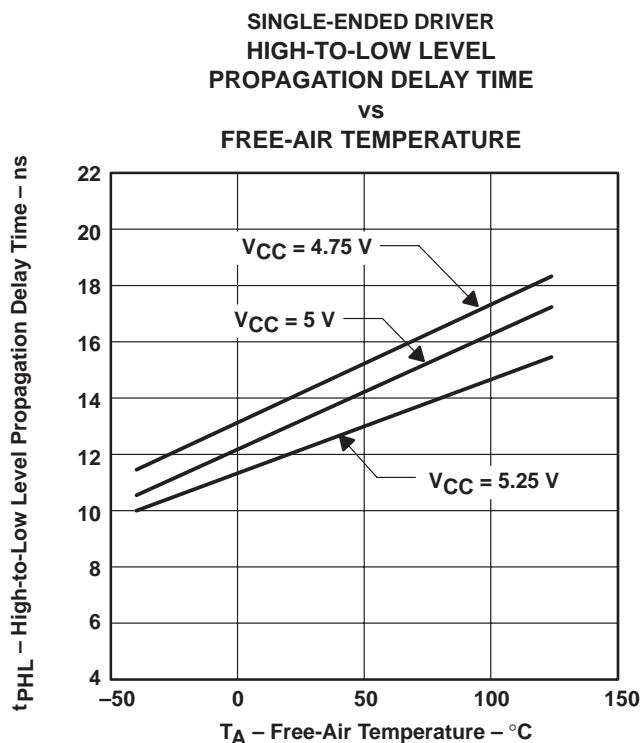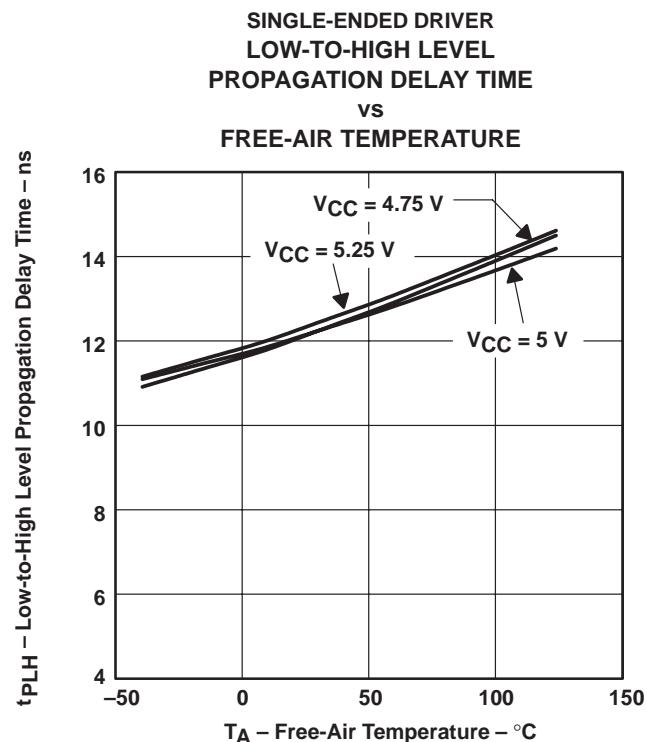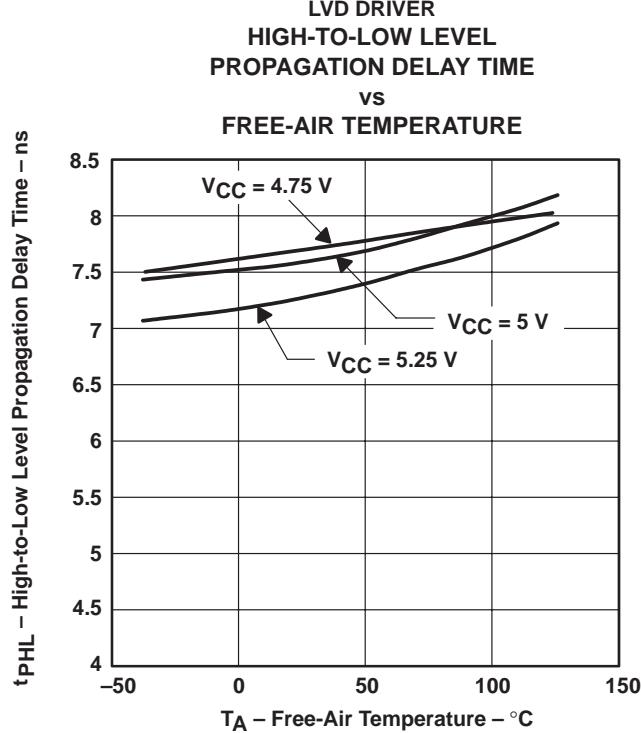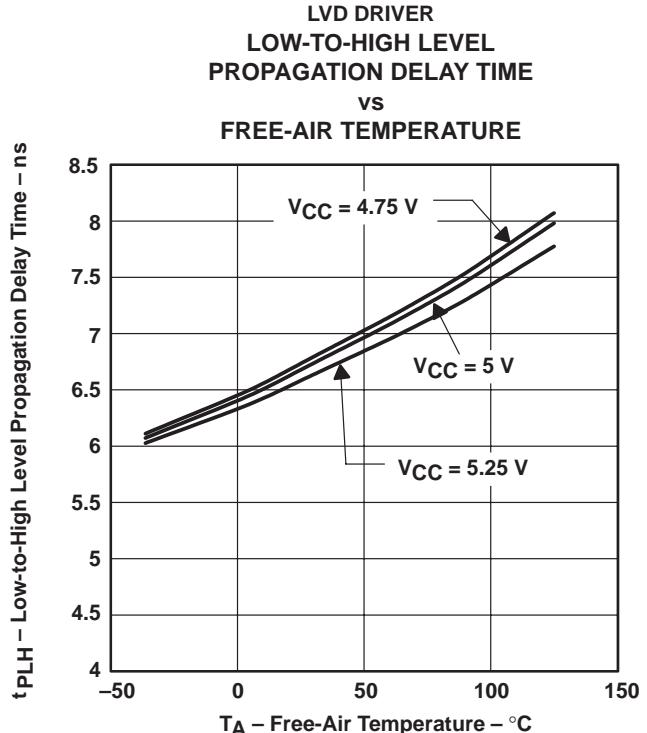
Figure 31

APPLICATION INFORMATION
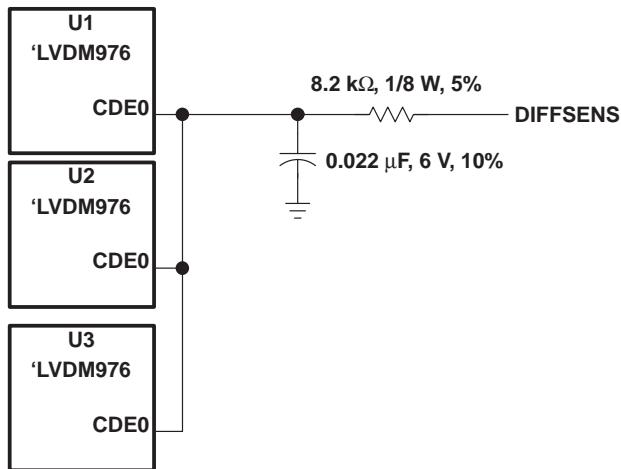
Figure 32. Low-Pass Filter for Connecting DIFFSENS to CDE0

MECHANICAL INFORMATION

DGG (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97
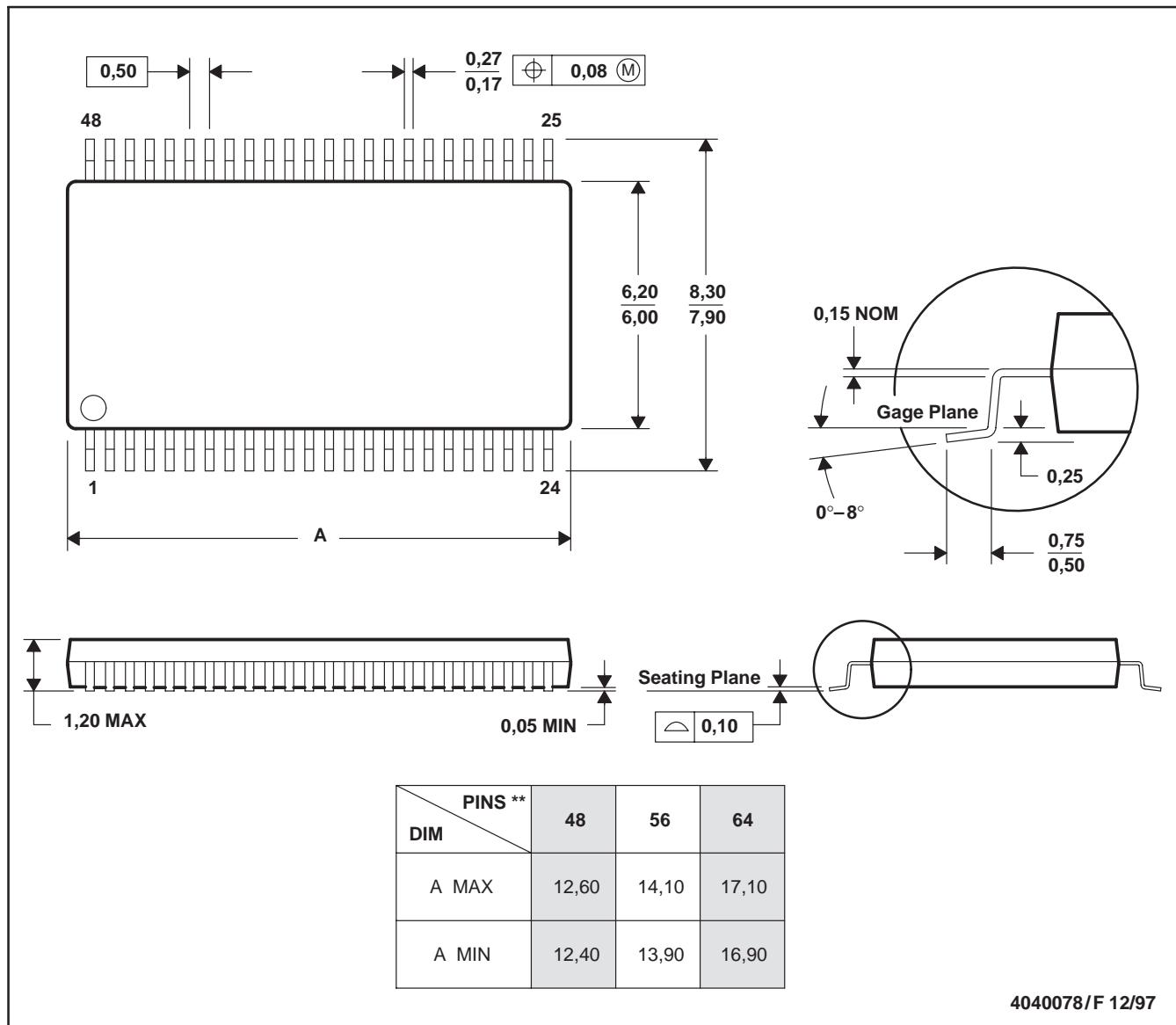
NOTES: C. All linear dimensions are in millimeters.
         D. This drawing is subject to change without notice.
         E. Body dimensions do not include mold protrusion not to exceed 0,15.
         F. Falls within JEDEC MO-153

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