PowerPAD Thermally Enhanced Package

TECHNICAL BRIEF: SLMA002

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TEXAS INSTRUMENTS

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PowerPAD Thermally Enhanced Package

Abstract

The PowerPAD thermally enhanced package provides greater design flexibility and increased thermal efficiency in a standard size IC package. PowerPAD's improved performance permits higher clock speeds, more compact systems and more aggressive design criteria.

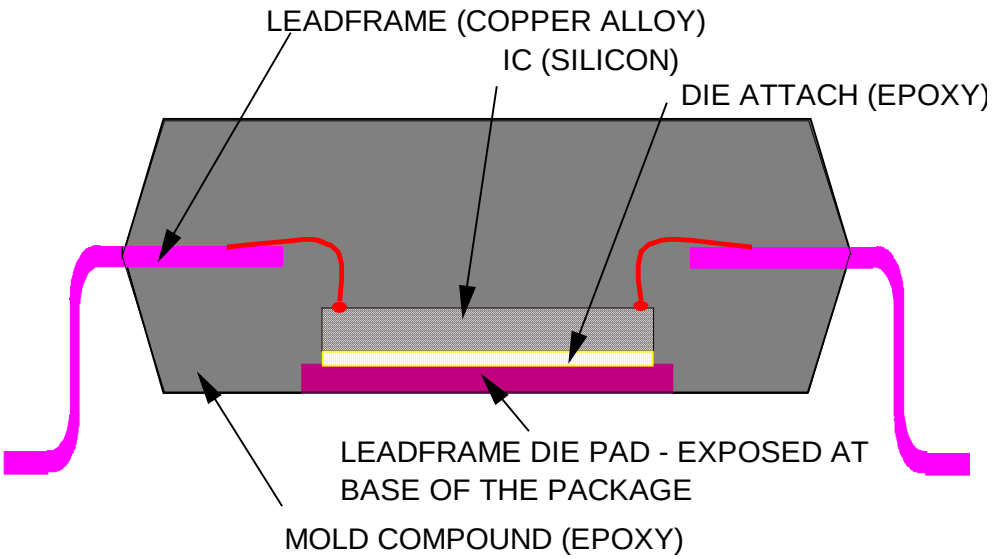
PowerPAD packages are available in several standard surface mount configurations. They can be mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

To make optimum use of the thermal efficiencies designed into the PowerPAD package, the PCB must be designed with this technology in mind. This document will focus on the specifics of integrating a PowerPAD package into the PCB design.

1. Introduction

The PowerPAD concept is implemented in a standard epoxy-resin package material. The integrated circuit die is attached to the leadframe die pad using a thermally conductive epoxy. The package is molded so that the leadframe die pad is exposed at a surface of the package. This provides an extremely low thermal resistance (Θ_{jc}) path between the IC junction and the exterior of the case. Because the external surface of the leadframe die pad is on the PCB side of the package, it can be attached to the board using standard flow soldering techniques. This allows efficient attachment to the board, and permits board structures to be used as heat sinks for the IC. Using vias, the leadframe die pad can be attached to a ground plane or special heat sink structure designed into the PCB. For the first time, the PCB designer can implement power packaging without the constraints of extra hardware, special assembly instructions, thermal grease or additional heat sinks.

Figure 1. Schematic Representation of the PowerPAD Package Components



Section View of a PowerPAD(tm)
PACKAGE

Because the exact thermal performance of any PCB is dependent on the details of the circuit design and component installation, exact performance figures cannot be given here. However, representative performance is very important in making design decisions. The data shown in Table 1 is typical of the performance that can be expected from the PowerPAD package.

Table 1. Typical Power Handling Capabilities of PowerPAD Packages

Package Type	Pin Count	Standard Package	PowerPAD Package
SSOP	20	0.75 W	3.25 W
TSSOP	24	0.55 W	2.32 W

Notes: 1) Assumes 150° C junction temperature and 80° C ambient temperature.
2) Values are calculated from Θ_{ja} figures shown in Appendix A.

For example, the user can expect 3.25 watts of power handling capability for the PowerPAD version of the 20-pin SSOP package. The standard version of this package can only handle 0.75 watts. Details for all package styles and sizes are given in Appendix A.

2. Installation and Use

2.1 PCB Attachment

Proper thermal management of the PowerPAD package requires PCB preparation. This preparation is not difficult, nor does it use any extraordinary PCB design techniques, however it is necessary for proper heat removal.

Figure 2. Bottom and Top View of the 20 pin TSSOP PowerPAD Package

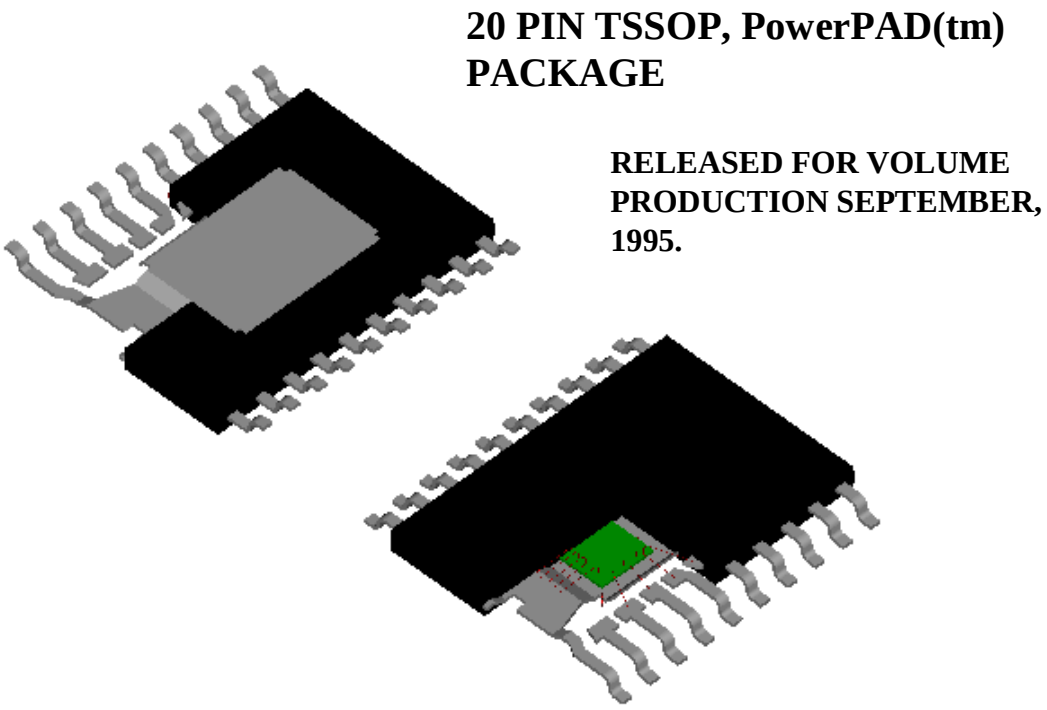
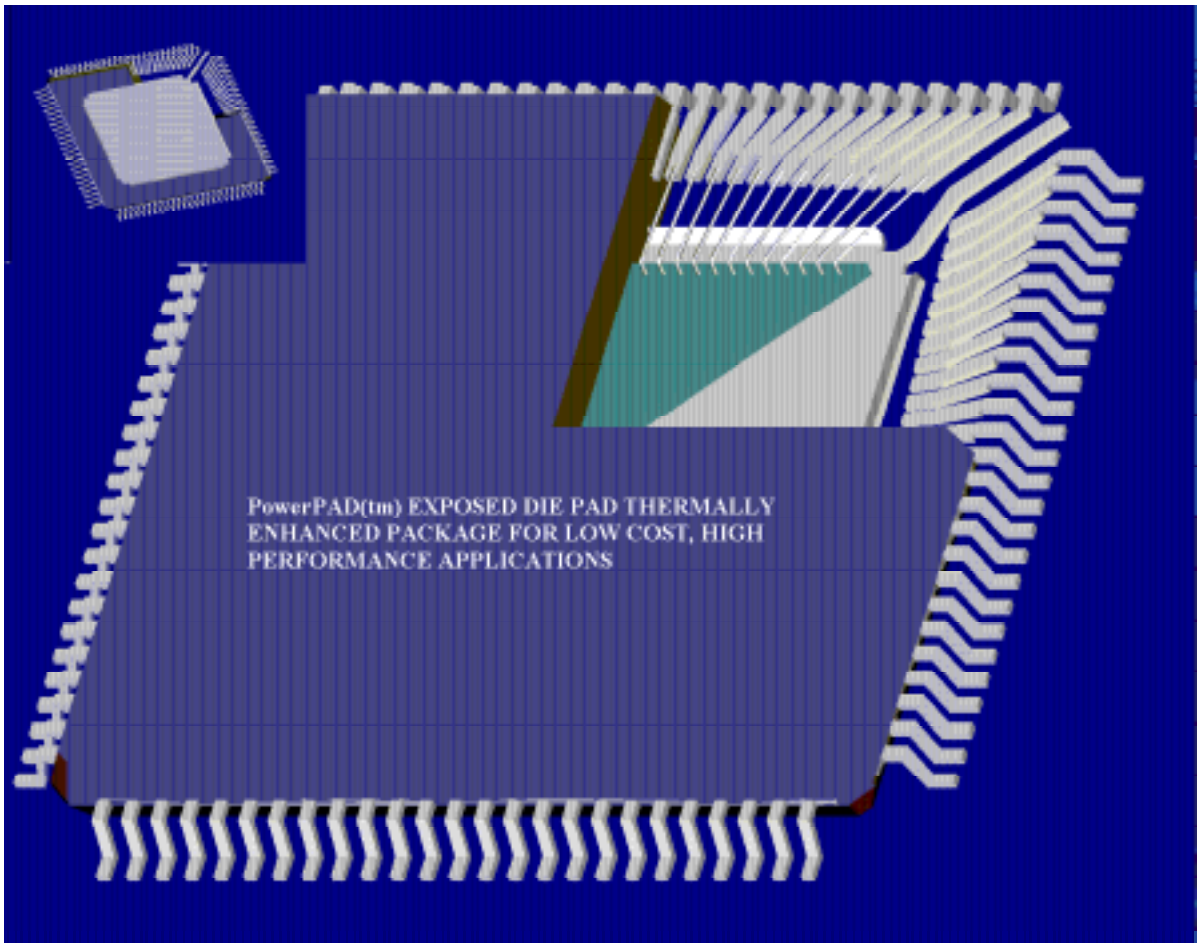


Figure 3. 64 Pin, 14 x 14 x 1.0mm Body TQFP PowerPAD Package



All of the thermally enhanced packages incorporate features that provide a very low thermal resistance path for heat removal from the integrated circuit - either to and through a printed circuit board (in the case of zero airflow environments), or to an external heatsink. The TI PowerPAD implementation does this by creating a leadframe where the bottom of the die pad is even with a surface of the package (as opposed to the case where a heat slug is embedded in the package body to create the thermal path). (See Figure 2 and Figure 3.)

2.2 PCB Design Considerations

The printed circuit board that will be used with PowerPAD packages must have features included in the design to remove the heat from the package efficiently.

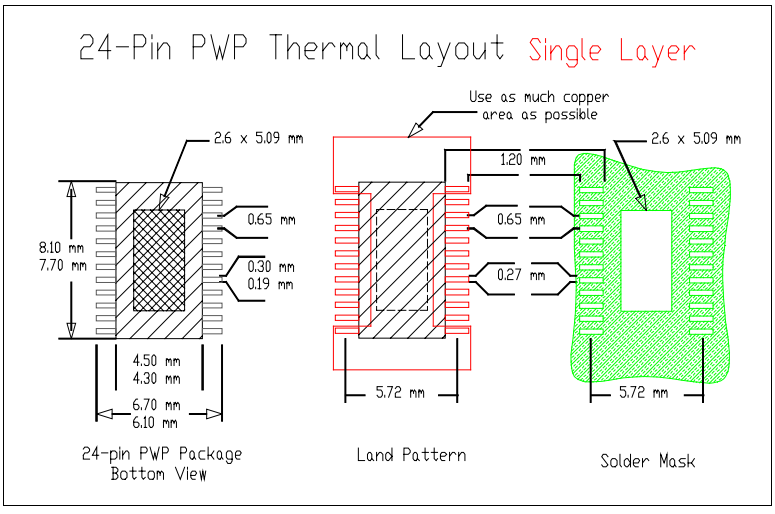
As a minimum, there must be an area of solder-tinned-copper underneath the PowerPAD package. This area is called the thermal land. As detailed below, the thermal land will vary in size depending on the PowerPAD package being used, the PCB construction and the amount of heat that needs to be removed. In addition, this thermal land may or may not contain thermal vias depending on PCB construction. The requirements for thermal lands and thermal vias are detailed below.

2.3 Thermal Lands

A thermal land is required on the surface of the PCB directly underneath the body of the PowerPAD package. During normal surface mount flow solder operations the leadframe on the underside of the package will be soldered to this thermal land creating a very efficient thermal path. Normally, the PCB thermal land will have a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. The size of the thermal land should be as large as needed to dissipate the required heat.

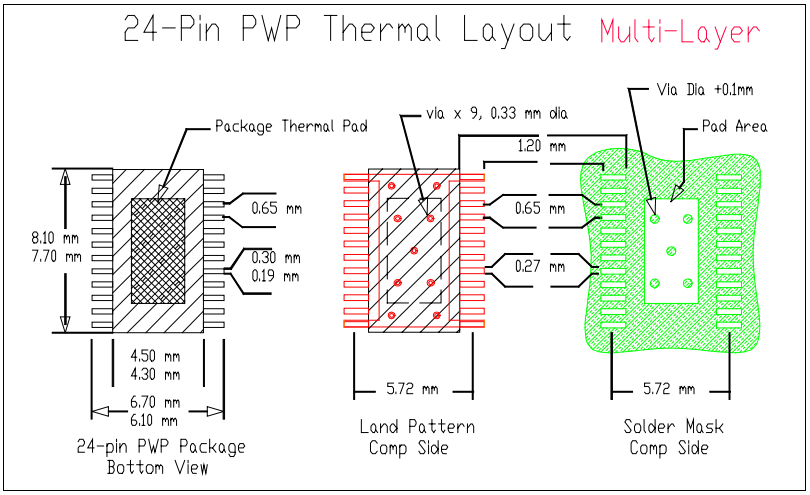
For simple, double-sided PCBs, where there are no internal layers, the surface layers must be used to remove heat. Shown in Figure 4 is an example of a thermal land for a 24-pin package. Details of the package, the thermal land and the required solder mask are shown. If the PCB copper area is not sufficient to remove the heat, the designer can also consider external means of heat conduction, such as attaching the copper planes to a convenient chassis member or other hardware connection.

Figure 4. Package and PCB Land Configuration for a Single Layer PCB



For multilayer PCBs, the designer can take advantage of internal copper layers (such as the ground plane) for heat removal. The external thermal land on the surface layer is still required, however the thermal vias can conduct heat out through the internal power or ground plane. Shown in Figure 5 is an example of a thermal land used for multilayer PCB construction. In this case, the primary method of heat removal is down through the thermal vias to an internal copper plane.

Figure 5. Package and PCB Land Configuration for a Multi-Layer PCB



Shown in Figure 6 are the details of a 64 pin TQFP PowerPAD package. The recommended PCB thermal land for this package is shown in Figure 7.

The maximum land size for TQFP packages is the package body size minus 2.0 mm. This land is normally attached to the PCB for heat removal, but can be configured to take the heat to an external heat sink. This is preferred when airflow is available.

Figure 6. 64 pin TQFP Package with PowerPAD Implemented, Bottom View

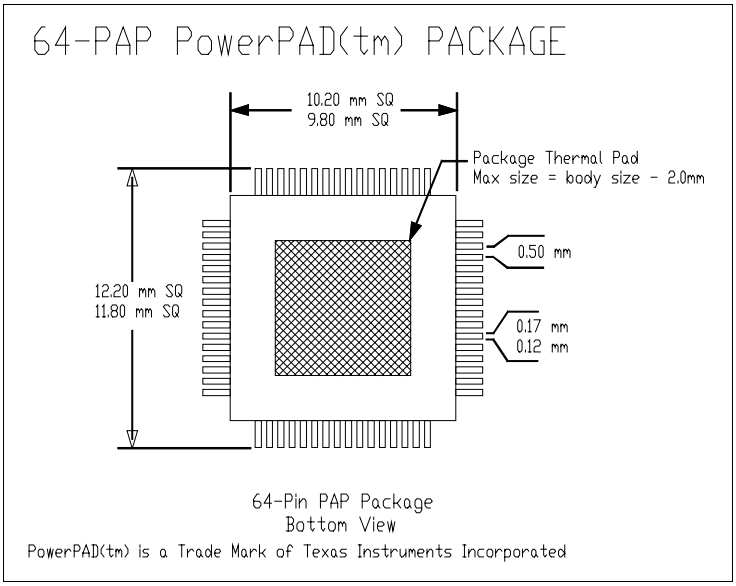
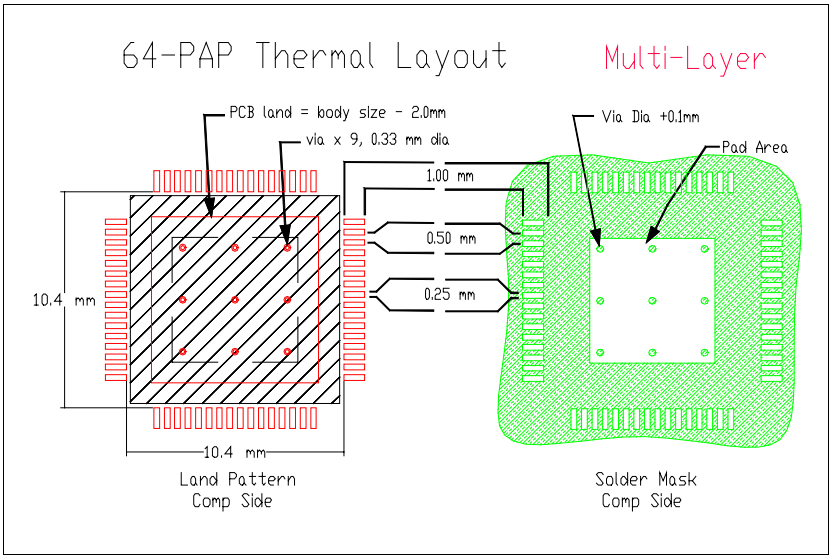


Figure 7. PCB Thermal Land Design Considerations for Thermally Enhanced TQFP Packages



2.4 Thermal Vias

Thermal vias are the primary method of heat transfer from the PCB thermal land to the internal copper planes or to other heat removal sources. The number of vias used, the size of the vias and the construction of the vias are all important factors in both the PowerPAD package thermal performance and the package-to-PCB assembly. Recommendations and guidelines for thermal vias follow.

Shown in Figure 8 and Figure 9 are the effects on PCB thermal resistance of varying the number of thermal vias for various sizes of die for 2- and 4-layer PCBs. As can be seen from the curves, there is a point of diminishing returns where additional vias will not significantly improve the thermal transfer through the board. For a small die, having from five to nine vias should prove adequate for most applications. For larger die, a higher number may be used simply because there is more space available under the larger package. Shown in Figure 10 are examples of ideal thermal land size and thermal via patterns for PowerPAD™ packages using 0.33mm (13 mil) diameter vias plated with 1 oz. copper. This thermal via pattern set represents a copper cross section in the barrel of the thermal via of approximately 1% of the total thermal land area. Fewer vias may be utilized and still attain a reasonable thermal transfer into and through the PCB as shown in Figures 8 and 9.

The number of thermal vias will vary with each product being assembled to the PCB, depending on the amount of heat that must be moved away from the package, and the efficiency of the system heat removal method. Characterization of the heat removal efficiency versus the thermal via copper surface area should be performed to arrive at an optimum value for a given board construction. Then the number of vias required can be determined for any new design to achieve the desired thermal removal value.

Figure 8. Impact of the Number of Thermal Vias versus Chip Area (Die Area)

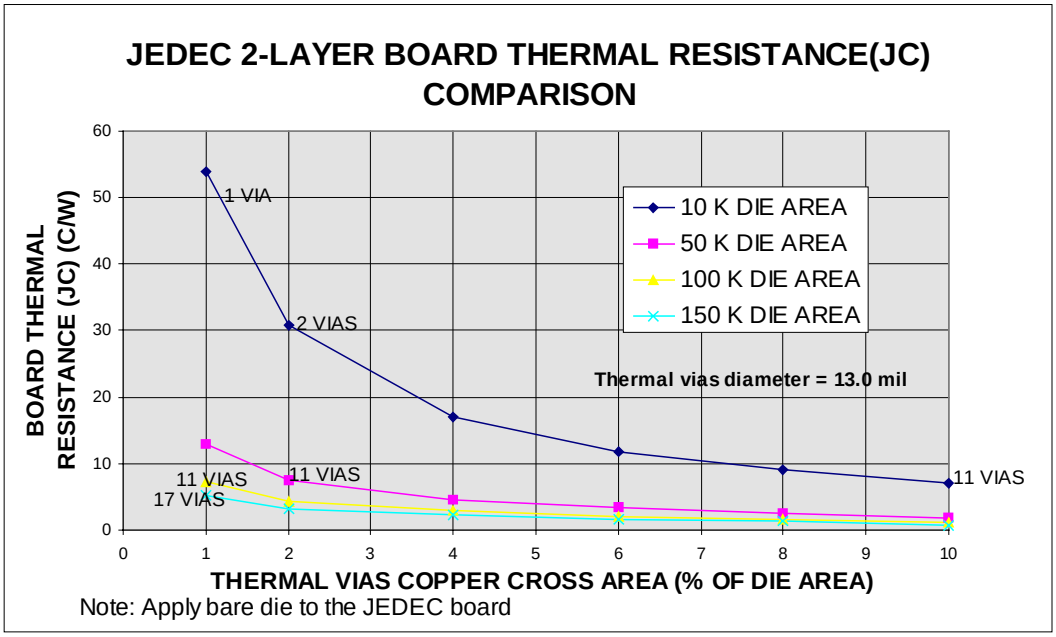


Figure 9. Impact of the Number of 0.33mm (0.013 inch) Diameter Thermal Vias versus Chip Area (Die Area)

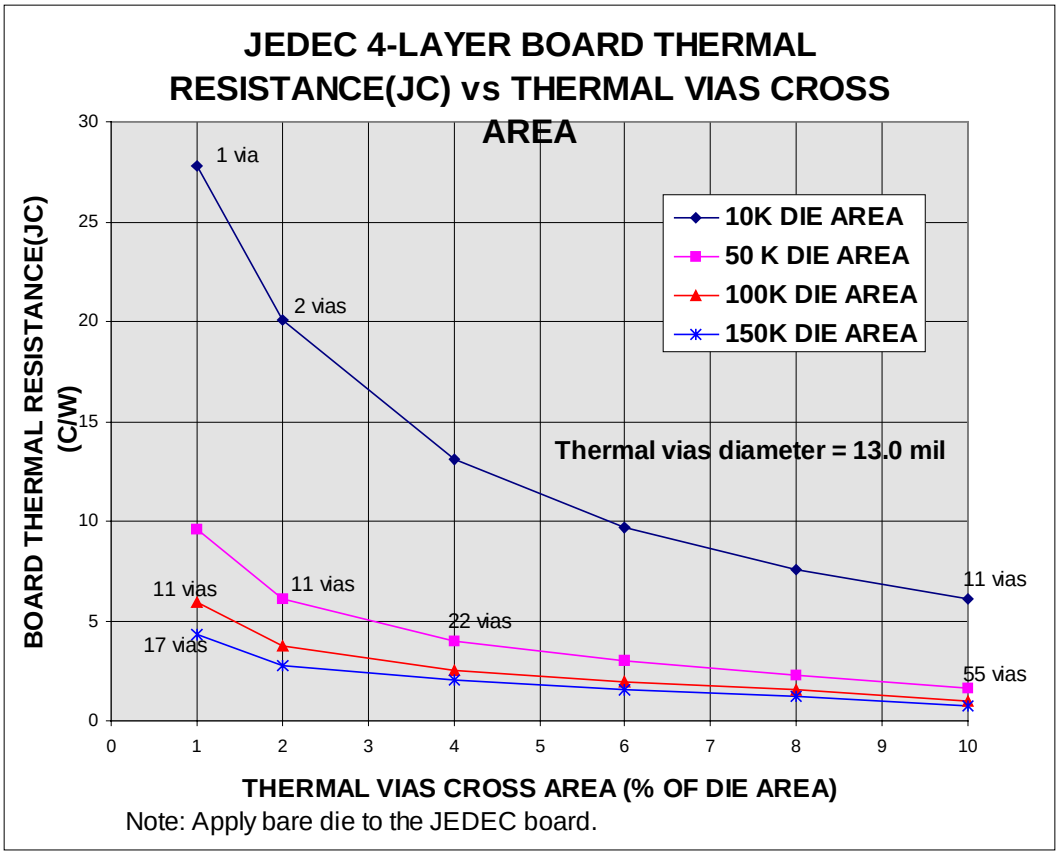
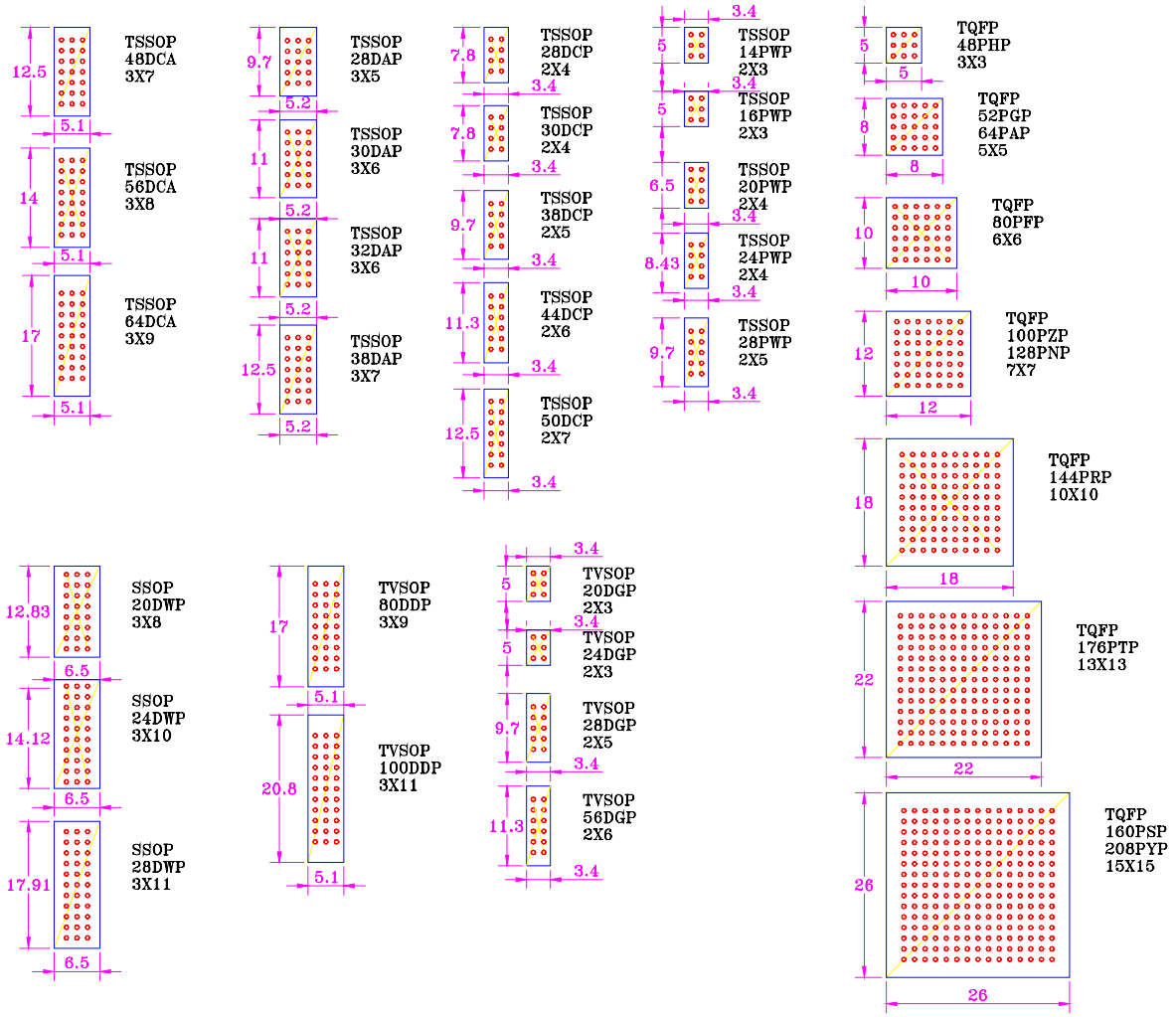


Figure 10. Ideal Thermal Land Size and Thermal Via Patterns for PowerPAD



Thermal vias connect the thermal land to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow. The experiments conducted jointly with Solectron Texas indicate that a via drill diameter of 0.33mm (13 mils) or smaller works well when 1 ounce copper is plated at the surface of the board and simultaneously plating the barrel of the via. If the thermal vias will not be plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a dimension equal to the via diameter + 0.1mm minimum. This will prevent the solder from being wicked through the thermal via and potentially creating a solder void in the region between the package bottom and the thermal land on the surface of the PCB.

To assure the optimum thermal transfer through the thermal vias to internal planes or the reverse side of the PCB, the thermal vias used in the thermal land should *not* use web construction techniques. Web construction on PCB vias is a standard technique used in most PCBs today to facilitate soldering, by constructing the via so that it has a high thermal resistance. This is *not* desirable for heat removal from the PowerPAD package. Therefore it is recommended that all vias used under the package make internal connections to the planes using a continuous connection completely around the hole diameter. Web construction for thermal vias is not recommended.

2.5 Solder Stencil Determination

A series of experiments were conducted at Solectron-Texas to determine the effects of solder stencil thickness on the quality of the solder joint between the thermal pad of a PowerPAD package and the thermal land on the surface of the PCB. Stencil thickness of 5, 6, and 7 mils were used in conjunction with a metal squeegee to deposit solder in the desired locations on the board. Note: 6 and 7 mil thick solder stencil is normally used with package lead pitch of 0.5 and 0.65mm respectively. A 5 mil thick stencil is normally used for packages with 0.4mm lead pitch to avoid solder bridging during reflow.

It was found that the standoff height for the package being attached to the PCB was critical in making good solder joints between the thermal pad of the package and the thermal land on the PCB. Note: during this series of experiments, a good solder joint was defined as a connection that joined at least 90% of the area of the smallest pattern to its intended connection point - such as the thermal pad of the package to the thermal land on the PCB. When the standoff height of the package (i.e., the distance between the bottom of the package leads and the bottom of the package body) was in the range of 0 to 2 mils, the package tended to float on the solder. This led to the possibility that all leads of the package would not be soldered to the lead traces on the board. This happened even when the 5 mil thick stencil was utilized. There were also cases when the solder was squeezed out from the desired land area, and then formed solder balls during the reflow process - an undesirable result that could cause shorting between package leads on the board surface, or short the thermal land on the PCB to the lead traces. A standoff height of 2.0 to 4.2 mils provided good solder joints for both the leads and the thermal pad for stencil thickness of 5, 6, and 7 mils. When the standoff height of the package was between 4.2 and 6.0 mils, only the 6 and 7 mil thick stencil provided consistently good solder joints for both the package leads and the thermal-pad to thermal-land bond. A general guideline would be to use the thickest solder stencil that works well for the products being assembled for the most process margin in assembling thermally enhanced parts to a PCB.

The Joint Electron Devices Engineering Council (JEDEC) specification for the standoff height of TSSOP and TQFP packages is the range of 0.05 to 0.15mm (1.97 to 5.91 mils), and is an acceptable range when the solder stencil thickness of 6 and 7 mils are used. Texas Instruments has elected to center the stand-off height of the PowerPAD packages at 3.5 mils (within the JEDEC specification range) to provide good package to PCB solder joint characteristics for standard solder stencil thickness of 5, 6, and 7 mils - the most common range within industry practice today.

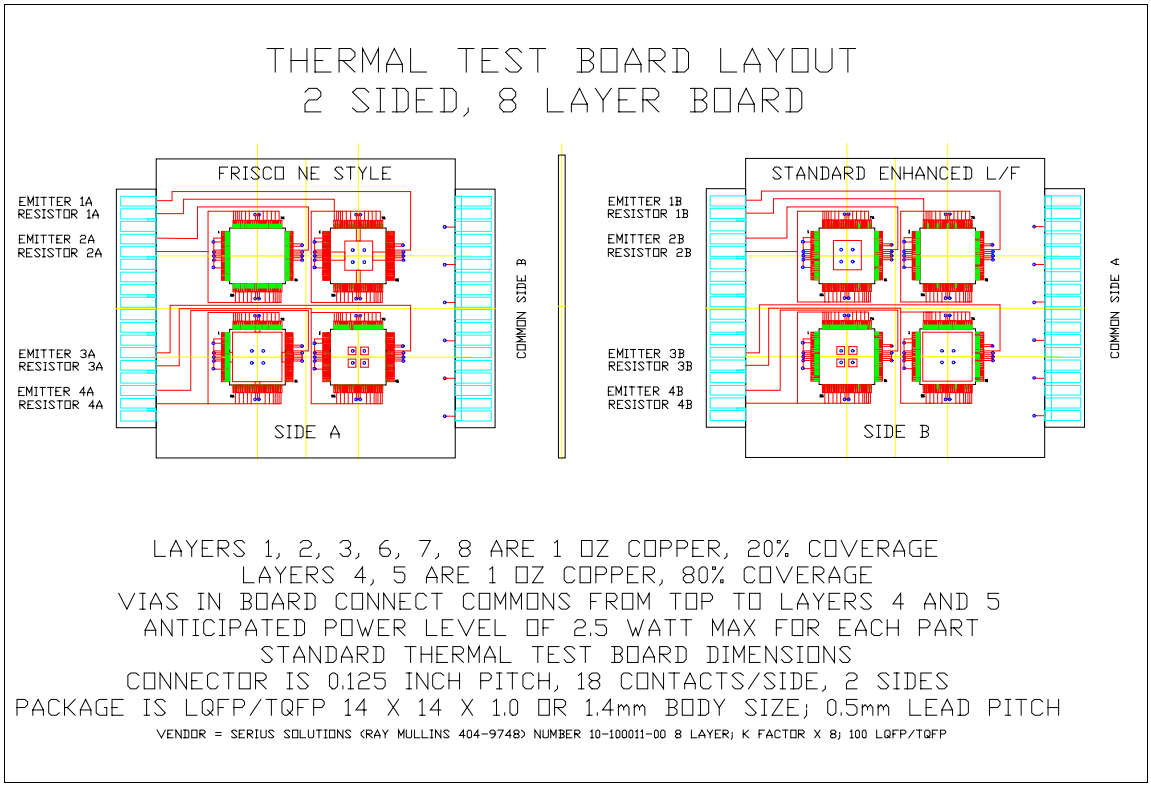
3. Assembly

Solder joint inspection in the attachment area of the thermal pad of the thermally enhanced packages to the thermal land on the PCB is difficult to perform with the best option to date being x-ray inspection. Tests performed within Texas Instruments and during the joint PCB experiments with Solectron-Texas indicate that x-ray inspection will allow detection of voiding within the solder joint and could be used either in a monitor mode, or for 100% inspection if required by the application. However, this is a slow and costly process so an effort was made to determine the minimum amount of solder required in this joint before degradation of the thermal performance became significant.

The experimental vehicle used in determining the amount of solder required was a 6S2P double sided test board with copper thermal lands on the surface of the board representing 0%, 7.5%, 22%, and 83% of the package body area. The package used was a 100 pin PowerPAD package (side B - standard enhanced l/f side of the PCB) as shown in Figure 11. There was additional copper area on the surface of the A side of the board due to connections between selected pins and the thermal land area. Four thermal vias were created in each thermal land area with connections to the internal power or ground plane, and continuing to make connection to the thermal land on the opposite side of the board.

A thermal test chip (Texas Instruments x-1158240) with dimensions of 6.1mm (0.240-inch) square was assembled in the test packages using die pad sizes of 6.0mm square, and 9.0mm square. The assembled units were then mounted to the PCB using either eutectic Sn63:Pb37 solder or thermally conductive epoxy adhesive. Measurement of the thermal resistance junction-to-case and thermal resistance junction-to-ambient with the individual packed parts powered at 2.5 watts was made using standard techniques for these measurements. Results are shown in Table 1 for tests with and without attachment between the package thermal pad and the board thermal land, as well as a comparison between solder and thermally conductive epoxy attachment. Table 2 provides the effective connection area obtained for each of the measurement points.

Figure 11. Test Board for Measurement of Θ_{jc} and Θ_{ja} Using 100 pin PowerPAD TQFP Packages



The relative thermal land size and location is shown along with the location of the thermal vias that connect the surface thermal land to the internal power or ground plane, and continuing to connect to the thermal land on the opposite side of the board. The board is approximately 82.5mm (3.25 inch) square.

Table 2 and Table 3 show the thermal resistance data for Θ_{jc} and Θ_{ja} (junction to case, and junction to ambient) for the 8 layer thermal test board, with the copper thermal land on the PCB shown as a percentage of the area of the package body.

Table 2. Measured Θ_{jc} from Test Board

MEASURED DATA						
		Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}
Part position on PCB	PCB Copper land as % of package body area	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**9.3**		**9.9**	**11.4**	
4B	7.5			**7.2**	**5.8**	**7.2**
2B	22	**6.8**		**6.3**	**7.2**	**7.5**
3B	83	**6.2**		**6.2**	**6.2**	**6.2**
2A	0	8.7	7.4	**9.1**	**7.8**	**7.8**
3A	7.5	7.6	8.3	**6.3**	**6.8**	**6.8**
1A	30		8		**6.6**	**6.5**
4A	85	7.5	7.3	**6.4**	**6.4**	**6.9**

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{jc} is measured in 1 cubic foot of liquid freon.

Table 3. Measured Θ_{ja} from Test Board

MEASURED DATA						
		Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}
Part position on PCB	PCB Copper land as % of package body area	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**33.8**		**40.6**	**44.3**	
4B	7.5			**27**	**23.1**	**25.5**
2B	22	**28.4**		**25.8**	**25**	**24.3**
3B	83	**24.2**		**26.9**	**24.6**	**24**
2A	0	34.4	34	**33.3**	**32.3**	**25.8**
3A	7.5	33.5	33	**24.4**	**24.9**	**25.2**
1A	30		31		**24.4**	**23.2**
4A	85	33.3	30	**25.5**	**24.6**	**24**

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{ja} is measured in 1 cubic foot of still air.

Small changes in the percentage of copper land area (between the “A” side of the PCB and the “B” side of the PCB) do not significantly affect the thermal resistance.

Table 4 and Table 5 show the relationship of the solder joint area between the thermal pad in the PowerPAD package and the thermal land of the PCB for the thermal resistance values obtained in Table 2 and Table 3.

Table 4. Relationship of the Solder Joint Area on Θ_{jc}, from Test Board Data

THERMAL PAD TO THERMAL LAND CONNECTION AREA ANALYSIS - %						
		Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}
Position on PCB	PCB Copper land size on PCB	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**0**	0	**0**	**0**	**0**
4B	4*(2x2)	**36**	16	**16**	**16**	**100**
2B	1*(6x6)	**80**	32	**32**	**32**	**100**
3B	1*(12x12)	**100**	100	**100**	**100**	**100**
2A	0	0	0	**0**	**0**	**0**
3A	4*(2x2)	80	16	**16**	**16**	**100**
1A	1*(6x6)+4*(5.7)	85	58	**58**	**58**	**100**
4A	1*(12x12)+4*(5.6)	100	100	**100**	**100**	**100**

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{jc} is measured in 1 cubic foot of liquid freon.

Table 5. Relationship of the Solder Joint Area on Θ_{ja}, from Test Board Data

THERMAL PAD TO THERMAL LAND CONNECTION AREA ANALYSIS - %						
		Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}
Position on PCB	PCB Copper land as % of package body area	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**0**	0	**0**	**0**	**0**
4B	4*(2x2)	**36**	16	**16**	**16**	**100**
2B	1*(6x6)	**80**	32	**32**	**32**	**100**
3B	1*(12x12)	**100**	100	**100**	**100**	**100**
2A	0	0	0	**0**	**0**	**0**
3A	4*(2x2)	80	16	**16**	**16**	**100**
1A	1*(6x6)+4*(5.7)	85	58	**58**	**58**	**100**
4A	1*(12x12)+4*(5.6)	100	100	**100**	**100**	**100**

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{ja} is measured in 1 cubic foot of still air.

In this example, there is significant improvement in thermal heat removal with solder joint areas as small as 16%, and the thermal removal efficiency as measured by Θ_{jc} and Θ_{ja} are within measurement error tolerance for all solder joint areas greater than 32%.

Based on the measured data for this test board configuration, Texas Instruments recommends a minimum solder joint area of 50% of the package thermal pad area when the part is assembled on a PCB. The results of the PCB assembly study conducted with Solectron-Texas indicate that standard board assembly processes and materials will normally achieve >80% solder joint area without any attempt to optimize the process for thermally enhanced packages. A characterization of the solder joint achieved with a given process should be conducted to assure that the results obtained during testing apply directly to the customer application, and that the thermal efficiency in the customer application is similar to the thermal test board results for the power level of the packaged component. If the heat removal is not at the efficiency desired, then either additional thermal via structures will have to be added to the PCB construction, or additional thermal removal paths will need to be defined (such as direct contact with the system chassis).

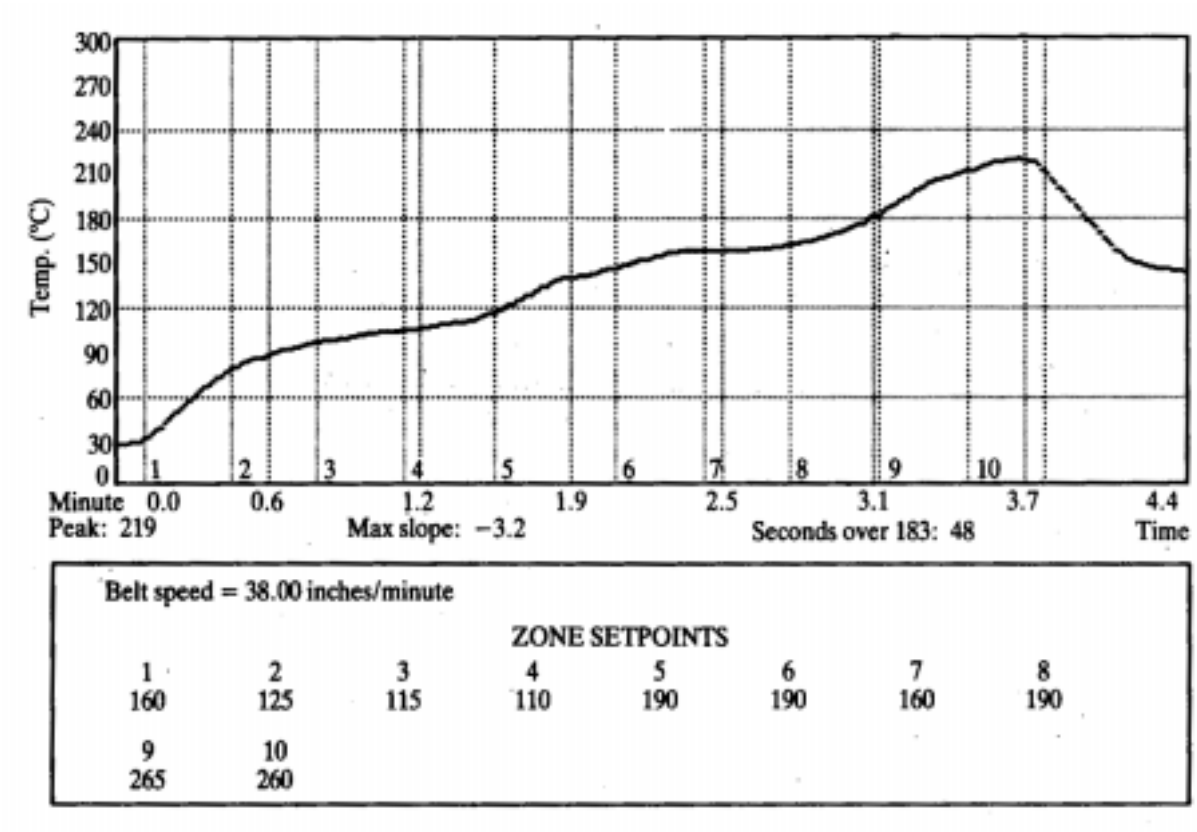
An alternative to attaching the thermal pad of the package to the thermal land of the PCB with solder is to use thermally conductive epoxy for the attachment. This epoxy can either be dispensed from the liquid form with a material that will cure during the reflow cycle, or a “B” staged preform that will receive the final cure during the reflow cycle. These materials can be the same as normally used with externally applied heat sinks. When epoxy is used as the attachment mechanism, then the effective attachment area is 100% of the die pad area, and there is some added benefit as thermal transfer to the PCB can occur, even with no copper thermal land at the surface of the PCB.

3.1 Solder Reflow Profile Suggestion

The reflow profile for IR board assembly using the Texas Instruments PowerPAD packages does not have to change from that used with conventional plastic packaged parts. The construction of the package does not add thermal mass, and the only new thermal load is due to the increased solder area between the package thermal pad and the thermal land on the PCB. A typical IR oven profile for fine pitch surface mount packages is shown in Figure 11. for eutectic Sn63:Pb37 solder. Nitrogen purged, convection IR reflow will be advantageous for this part to PCB assembly to minimize the possibility of solder ball formation under the package body.

Figure 12 shows a typical infrared (IR) oven profile for a fine pitch plastic package assembly mounted to an FR-4 PCB using eutectic Sn63:Pb37 solder.

Figure 12. Typical Infrared Oven Profile



Peak temperature should be approximately 220 degrees centigrade, and the exposure time should normally be less than 1 minute at temperatures above 183 degrees centigrade.

3.2 Installation and Assembly Summary

The PowerPAD package families can be attached to printed circuit boards using conventional Infrared solder reflow techniques that are standard in the industry today without changing the reflow process used for normal fine pitch surface mount package assembly. A minimum solder attachment area of 50% of the package thermal pad area is recommended to provide efficient heat removal from the semiconductor package, with the heat being carried into or through the PCB to the final thermal management system. This attachment can be achieved either by the use of solder for the joining material, or through the use of thermally conductive epoxy materials. Typical PCB thermal land pattern definitions have been provided that have been shown to work with 4 and 8 layer PCB test boards, and can be extended for use by other board structures.

4. Repair

Reworking thermally enhanced packaged semiconductors that have been attached to PCB assemblies through the use of solder or epoxy attachment can present significant challenges, depending on the point at which the re-work is to be accomplished. Tests of re-work procedures to date indicate that part removal from the PCB is successful with all of the conventional techniques used in the industry today. The challenge is part replacement on the board due to the combined thermal enhancement of the PCB itself, and the addition of thermal removal enhancement features to the semiconductor package. The traditional steps in the rework or repair process can be simply identified by the following steps for solder attached components:

1) Unsolder old component from the board
2) Remove any remaining solder from the part location
3) Clean the PCB assembly
4) Tin the lands on the PCB and leads, or apply solder paste to the lands on the PCB
5) Target, align, and place new component on the PCB
6) Reflow the new component on the PCB
7) Clean the PCB assembly

When thermally conductive epoxy has been used to attach the thermal pad of the package to the thermal land on the PCB, the same basic steps in the rework or repair procedure can be followed with only minor modifications:

1) Unsolder old component and torque package to remove from the board
2) Remove any remaining solder from the part location
3) Remove any remaining epoxy from the thermal land on the PCB
4) Clean the PCB assembly
5) Tin the lands on the PCB and leads, or apply solder paste to the lands on the PCB
6) Place new thermally conductive “B” staged epoxy preform or dispense epoxy on thermal land
7) Target, align, and place new component on the PCB
8) Reflow the new component on the PCB

9) Complete epoxy cure (if required as a separate step)

10) Clean the PCB assembly

4.1 Part Removal From PCBs

Almost any removal process will work to remove the device from the PCB, even with the thermal pad of the package soldered to the PCB. Heat is easily transferred to the area of the solder attachment either from the exposed surface thermal land of the PCB (single layer example), or through the thermal vias in the PCB (multi-layer example) from the backside of the PCB.

Re-work has been performed for both the TSSOP and TQFP PowerPAD style packages using METCAL removal irons and hot air. The specific example of a 20 pin TSSOP PowerPAD part removal is discussed in detail.

A 750-Watt METCAL removal iron was used in conjunction with hot air to verify the removal method efficiency to take 20 pin PowerPAD TSSOP packages off of assembly test boards. The hot air method is recommended as it subjects the PCB and surrounding components to less thermal and mechanical stress than other methods available, and has been proven to be much easier to control than some of the hot bar techniques. Use of the hot air method may require assemblers to acquire tools specifically for the smaller packages since most assemblers use a hot bar method for packages of this size. (Note: This same tool will also be needed for part re-attachment to the PCB when the hot air method is employed). A tool with an integrated vacuum pick up tip will be an advantage in the part removal process so the part can be physically removed from the board as soon as the solder reaches liquidus. Preheating of the local area of the PCB to a temperature of approximately 160 degrees centigrade can make the part removal easier. This is especially helpful in the case of larger packages such as 56 pin TSSOP or 100-pin TQFP style packages. This preheat will be required in the thermal removal method if the semiconductor package is a heat slug package rather than the TI PowerPAD package version. Some experimentation will be required to find the optimum procedure to use for any specific PCB construction and thermally enhanced package version.

After the part has been removed from the PCB, conventional techniques to clean the area of the part attachment - such as solder wicking - will be needed to prepare the location for subsequent attachment of a new component.

When thermally conductive epoxy has been used for attachment of the package thermal pad to the thermal land on the PCB, a slightly different approach to part removal must be used. This will require a tool that has dimensions that will allow contact with the sides of the package body directly above the leads, and will allow the package to be twisted or rotated horizontally when the solder joints of the package leads have reached liquidus. The temperature at the epoxy interface to the package thermal pad or the PCB thermal land must be above the glass transition temperature of the epoxy (typically less than 180 degrees centigrade) to break the adhesion between the epoxy and the attach location with the twisting or rotational method discussed above. In most cases, any remaining epoxy on the PCB after part removal can be removed by peeling it from the surface - occasionally, it will be necessary to apply heat to the epoxy location so it will peel away from the PCB cleanly.

4.2 Attachment of a Replacement Component to the PCB

Preparation of the PCB for attachment of a new component follows normal industry practice with respect to the lands on the board and the leads of the package. Both may be tinned, and/or solder paste applied to the lands for new component attachment. In addition, when solder will be used to re-attach the thermal pad of the package to the thermal land on the PCB, solder paste will need to be applied to the surface of the thermal land on the board. This may be in the form of stripes of solder paste with sufficient volume to achieve the desired solder coverage, or a solder preform may be applied to the location for attachment. In a factory environment, the component is then placed in the desired location and alignment, and processed through a reflow oven to re-establish the desired solder joints. This is the most desirable process and is normally the easiest to accomplish.

When a manual or off-line attachment and reflow procedure is to be used, the challenge of supplying sufficient heat to the components and solder becomes a greater concern. In most cases, the corner leads of the package being attached will be tack soldered to hold the component in alignment so the balance of the leads and the thermal pad to thermal land solder reflow can be accomplished without causing part movement from its desired location. As in the part removal case, it is advisable to pre-heat the board or the specific device location to a temperature below the melting point of the solder to minimize the amount of heat that must be provided by the reflow device as the part is being attached. A good starting point is to pre-heat to approximately 160 degrees centigrade. A hot gas reflow tool can then be used to complete the solder joint formation both at the leads and for the connection of the thermal pad to the thermal land of the PCB. Care must be taken at this operation to avoid blowing solder out from the thermal pad to thermal land interface and causing solder balling under the package or creating

lead to lead or thermal land to lead shorts. The thermal enhancement of the package and the PCB will require a higher temperature gas or higher gas flow to reach solder liquidus than would be needed with an assembly lacking these enhancements. The tool should be specifically sized to the part being reworked to minimize possible damage to surrounding components or the PCB itself.

If the re-attachment of the interface between the thermal pad of the package and the thermal land of the PCB using solder attachment is too difficult to control using hot gas methods, then the best approach is to use either a thermally conductive “B” staged epoxy preform cut to the shape of the thermal land on the PCB, or dispensing liquid thermally conductive epoxy in a pattern on the thermal land that will result in at least a 50% void free connection between the pad and the land. Virtually any epoxy material that is used for the attachment of external heat sinks to packaged components is suitable for this application, and cure time/temperature requirements can be matched to the product need (anywhere from 24 hours at room temperature to less than 1 hour at temperatures below 100 degrees centigrade). Care must be taken to choose a material with limited run-out to avoid the possibility of shorting adjacent package leads together or shorting the thermal land of the PCB to the package leads.

It should be noted that the Texas Instruments PowerPAD packages are easier to rework at the board level than other semiconductor packages utilizing metal slugs for the thermal path between the chip and the PCB. This is due to the additional requirement for heating the total mass of the slug to reflow temperatures versus heating the thermal pad of the PowerPAD package. The hot gas temperature and/or flow becomes critical for effective joining of the components without causing damage to the adjacent components or the PCB. In either case, the use of thermally conductive epoxy materials will make the rework task easier and more reliable to perform in a manual repair environment.

5. Summary

An overview of the design, use and performance of the Texas Instruments PowerPAD package has been presented. The package is simple to use and can be assembled and repaired using existing assembly and manufacturing tools and techniques. Package performance is outstanding. By exposing the leadframe on the package bottom, extremely efficient thermal transfer between the die and the PCB can be achieved.

The simplicity of the PowerPAD package not only makes for a low cost package, but there is no additional cost in labor or material for the customer using standard surface mount assembly techniques. The only preparation needed to implement a PowerPAD design is at the PCB design stage. Simply by including a thermal land and thermal vias on the PCB the design can use the PowerPAD package effectively.

Appendix A. Thermal Modeling of PowerPAD Packages

Table 6. Thermal Characteristics for Different Package and PCB Configurations

Package Description			2 oz. Trace and Copper Pad with Solder			2 oz. Trace and Copper Pad without Solder			Standard Package JEDEC Low Effect with 1 oz. trace		
Pkg Type	Pin Count	Package Designator	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)
SSOP	20	DWP	21.46	0.37	1.617	43.91	0.37	6.031	92.95	16.58	2.212
	24	DWP	20.77	0.27	1.507	38.43	0.27	4.88	80.49	13.49	1.959
	28	DWP	19.52	0.22	1.337	33.92	0.22	4.109	69.73	11.24	1.641
TVSOP	80	DDP	19.88	0.21	0.196	32.64	0.21	0.359	65.53	4.69	0.353
	100	DDP	18.35	0.17	0.182	28.45	0.17	0.313	54.55	3.73	0.297
	20	DGP	37.92	2.46	1.074	95.88	2.46	3.318	192.65	28.85	1.054
	24	DGP	36.87	2.46	1.056	89.50	2.46	3.176	179.91	28.41	0.999
	48	DGP	27.35	0.72	0.45	52.82	0.72	1.138	107.49	12.32	0.58
	56	DGP	25.42	0.58	0.406	46.69	0.58	0.98	95.48	10.40	0.526
TSSOP	48	DCA	22.30	0.32	0.22	40.27	0.32	0.443	84.04	6.63	0.434
	56	DCA	21.17	0.27	0.212	36.42	0.27	0.401	75.50	5.81	0.395
	64	DCA	19.89	0.21	0.196	32.52	0.21	0.357	65.70	4.69	0.35
	28	DAP	25.10	0.45	0.244	51.28	0.45	0.556	110.60	8.96	0.548
	30	DAP	24.20	0.45	0.233	48.34	0.45	0.551	103.45	8.73	0.486
	32	DAP	23.51	0.32	0.233	44.32	0.32	0.468	95.63	7.32	0.478
	38	DAP	22.41	0.31	0.219	41.18	0.31	0.444	87.32	6.57	0.454
	28	DCP	30.62	0.94	0.534	63.99	0.94	1.424	133.67	16.13	0.707
	30	DCP	30.55	0.94	0.532	63.32	0.94	1.408	131.23	16.05	0.695
	38	DCP	27.41	0.72	0.447	52.93	0.72	1.13	109.55	12.42	0.598
	44	DCP	25.57	0.58	0.406	47.18	0.58	0.982	97.13	10.47	0.538
	50	DCP	24.10	0.51	0.369	43.76	0.51	0.892	89.53	9.34	0.5
	14	PWP	37.47	2.07	0.851	97.65	2.07	2.711	195.35	26.86	1.047
	16	PWP	36.51	2.07	0.848	90.26	2.07	2.6	182.31	26.56	0.964
	20	PWP	32.63	1.40	0.607	74.41	1.40	1.777	151.89	19.90	0.77
	24	PWP	30.13	0.92	0.489	62.05	0.92	1.263	128.44	14.83	0.665
	28	PWP	27.87	0.72	0.446	56.21	0.72	1.169	115.82	12.41	0.623
TQFP	48	PHP	29.11	1.14	0.429	64.42	1.14	1.262	108.71	18.18	0.511
	52	PGP	21.61	0.38	0.192	42.58	0.38	0.391	77.15	7.83	0.353
	64	PBP	17.46	0.12	0.155	28.04	0.12	0.252	52.21	3.12	0.267
	64	PAP	21.47	0.38	0.19	42.20	0.38	0.386	75.83	7.80	0.347
	80	PFP	19.04	0.17	0.174	31.52	0.17	0.29	57.75	4.20	0.297
	100	PZP	17.28	0.12	0.154	27.32	0.12	0.247	49.17	3.11	0.252
	128	PNP	17.17	0.12	0.152	27.07	0.12	0.244	48.39	3.11	0.248
LQFP	144	PRP	15.68	0.13	0.199	27.52	0.13	0.346	47.34	4.62	0.288
	176	PTP	14.52	0.10	0.17	24.46	0.10	0.28	42.95	3.67	0.257
	160	PSP	11.14	0.10	0.14	22.40	0.10	0.266	43.93	3.70	0.262
	208	PYP	10.96	0.10	0.139	21.48	0.10	0.258	39.18	3.66	0.235

General

Thermal modeling is used to estimate the performance and capability of IC packages. From a thermal model, design changes can be made and thermally tested before any time is spent on manufacturing. It can also be determined what components have the most influence on the heat dissipation of a package. Models can give an approximation of the performance of a package under many different conditions. In this case, a thermal analysis was performed in order to approximate the improved performance of a PowerPAD thermally enhanced package to that of a standard package.

Modeling Considerations

There are only a few differences between the thermal models of the standard packages and models for PowerPAD. The geometry of both packages was essentially the same, except for the location of the lead frame bond pad. The pad for the thermally enhanced PowerPAD package is deep downset, so its location is further away from the lead fingers than a standard package lead frame pad. Both models used the maximum pad and die size possible for the package, as well as using a lead frame that had a gap of one lead frame thickness between the pad and the lead fingers. The lead frame thickness was:

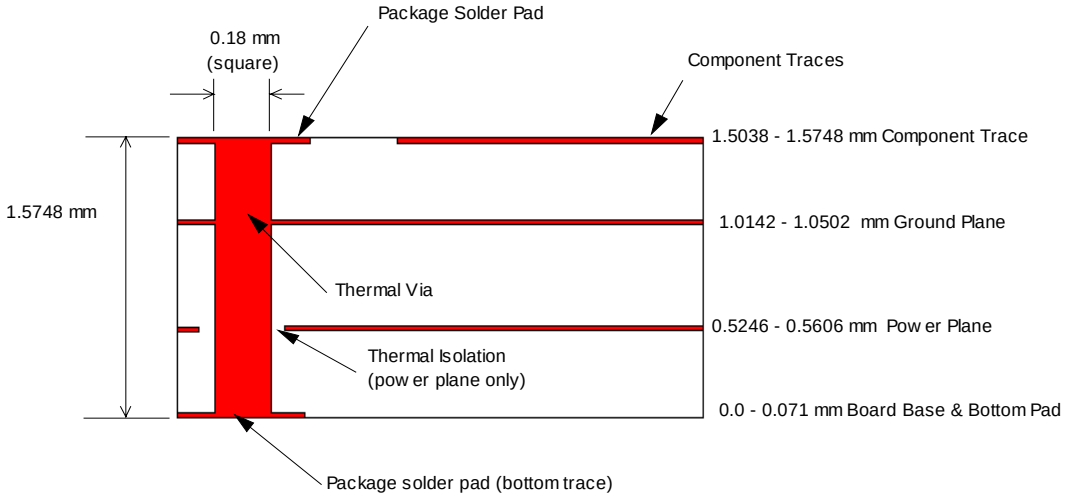
TQFP/LQFP: 0.127 mm, or 5 mils
TSSOP/TVSOP/SSOP: 0.147 mm, or 5.8 mils

In addition, the board design for the standard package is different than the PowerPAD. One of the most influential components on the performance of a package is board design. In order to take advantage of PowerPAD's heat dissipating abilities, a board must be used that acts similarly to a heat sink and allows for the use of the exposed (and solderable) deep downset pad. This is Texas Instruments' recommended board for PowerPAD (see Figure 13). A summary of the board geometry is included below.

Texas Instruments Recommended Board for PowerPAD

- 0.062" thick
- 3" x 3" (for packages <27 mm long)
- 4" x 4" (for packages >27 mm long)
- 2 oz. copper traces located on the top of the board (0.071 mm thick)
- Copper areas located on the top and bottom of the PCB for soldering
- Power and ground planes, 1 oz. copper (0.036 mm thick)
- Thermal vias, 0.3 mm diameter, 1.5 mm pitch
- Thermal isolation of power plane

Figure 13. Texas Instruments Recommended Board (Side View)



The standard packages were placed on a board that is commonly used in the industry today, following the JEDEC standard. It does not contain any of the thermal features that are found on the Texas Instruments recommended board. It only has component traces on the top of the board. A summary of the standard is located below:

JEDEC Low Effective Thermal Conductivity Board (Low-K)

- 0.062” thick
- 3” x 3” (for packages <27 mm long)
- 4” x 4” (for packages >27 mm long)
- 1 oz. copper traces located on the top of the board (0.036 mm thick)

These boards were used to estimate the thermal resistance for both PowerPAD and the standard packages under many different conditions. While the PowerPAD can be used on a JEDEC low-k board, in order to achieve the maximum thermal capability of the package, it is recommended that it be used on the Texas Instruments heat dissipating board design. It allows for the exposed pad to be directly soldered to the board, which creates an extremely low thermal resistance path for the heat to escape.

A general modeling template was used for each PowerPAD package, with variables dependent on the package size and type. The package dimensions and an example of the template used to model the packages are shown in Figure 14 and Table 7. While only 1/4 of the package was modeled (in order to simplify the model and to lessen the calculation time), the dimensions shown are those for a full model.

Figure 14. Thermal Pad and Lead Attachment to a PCB Using the PowerPAD Package

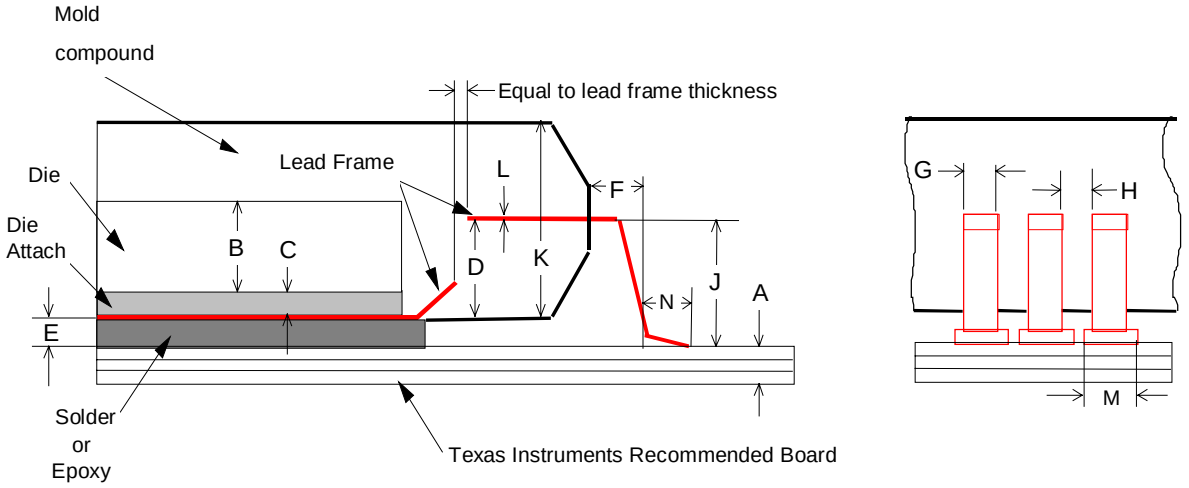


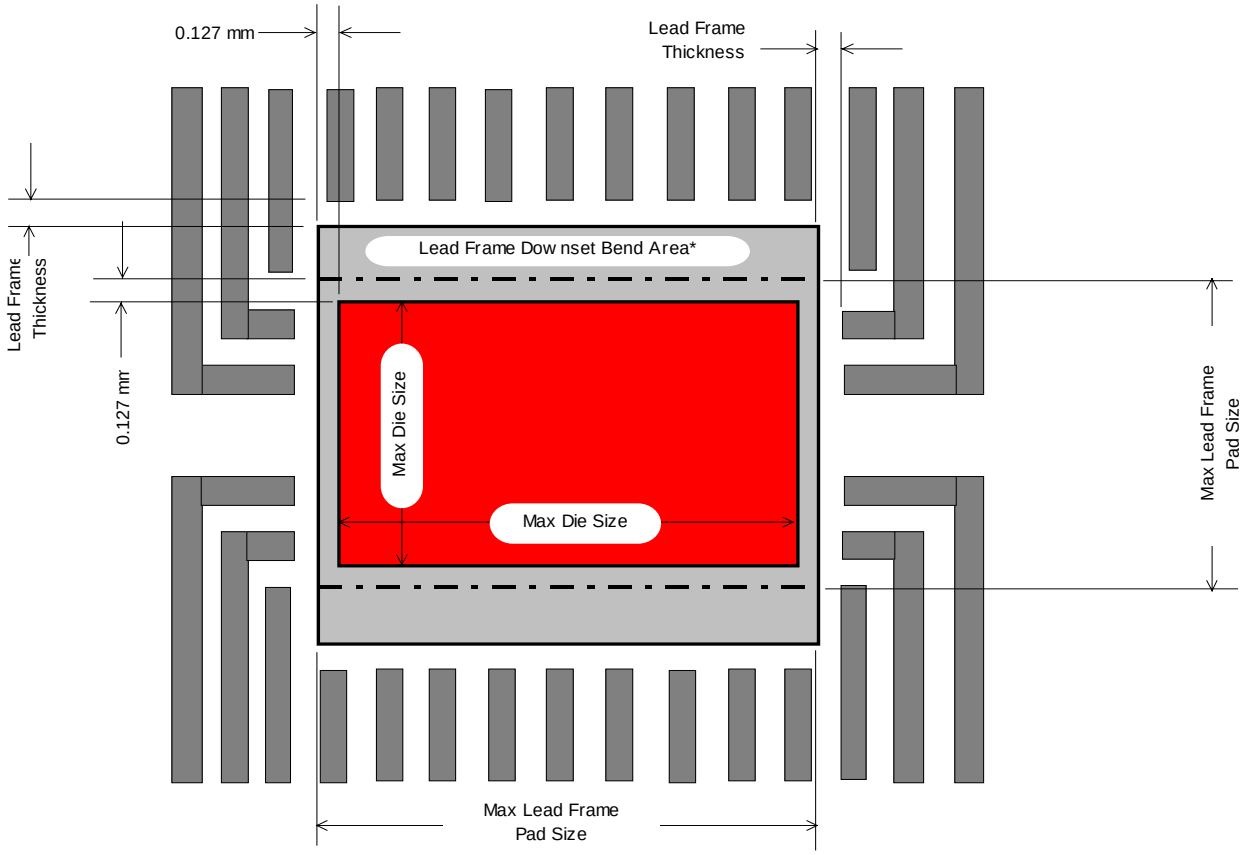
Table 7. PowerPAD Package Template Description

(A)	PCB Thickness:	1.5748 mm	(K)	Package Thickness:	(3)
	PCB Length:	76.2 mm (1)		Package Length:	(3)
	PCB Width:	76.2 mm (1)		Package Width:	(3)
(B)	Chip Thickness:	0.267 mm	(L)	Pad Thickness:	0.147 mm (8)
	Chip Length:	(2)		Pad Length:	(3)
	Chip Width:	(2)		Pad Width:	(3)
(C)	Die Attach Thickness:	0.0127 mm		PCB Trace Length:	25.4 mm
(D)	Lead Frame Downset:	(3)		PCB Trace Thkn:	0.071 mm
	Tie Strap Width:	(3)		PCB Backplane Th:	0.0 mm (4)
(E)	PCB to Package Bottom:	0.09 mm		PCB Trace Width:	0.254 mm
(G)	Shoulder Lead Width:	(3),(5),(6)	(M)	Foot Width:	(5)
(H)	Shoulder Lead Space:	(3),(6)	(N)	Foot Length on PCB:	(3)
(J)	Shoulder to PCB Dist.:	(7)			

Notes: 1) 99.6mm for packages > 27mm max length
2) Chip size is 10 mils smaller than the largest pad size (5 mils from each side)
3) Dependent on package size and type
4) The recommended board requires the addition of two internal copper planes, solder pads, and thermal vias
5) Foot width was set equal to shoulder lead width for model efficiency
6) Lead pitch is equal to the shoulder lead width plus the shoulder lead space (pitch = G + H)
7) The shoulder to board distance is equal to the downset plus the board to package bottom distance (J = D + E)
8) The pad thickness for TQFP/LQFP is equal to 0.127 mm
9) All dimensions are in millimeters.

In addition to following a template for the dimensions of the package, a simplified lead frame was used. A description of the lead frame geometry is seen in Figure 15.

Figure 15. General Leadframe Drawing Configuration



NOTE:
The lead frame downset bend area = 20 mils (lead frame thickness). For SSOP, TSSOP, and TVSOP packages, add the bend area to the width of the pad. For TQFP and LQFP, add the bend area to both the width and length of the pad.

Boundary Conditions

The junction-to-ambient (θ_{JA}), junction-to-case (θ_{JC}), and junction-to-top of package (Ψ_{JT}) thermal resistances were calculated using a Texas Instruments finite difference program. This program uses assumptions in order to simplify the calculation time, but is still accurate to within 10% of the actual measured number. Of course, the model conditions must be approximately the same as the test conditions for this to be true. Below is a summary of the analysis boundary conditions.

Junction-to-ambient (θ_{JA}):

- Software calculated convection coefficients
- No radiation inputs
- 25 ^{o}C ambient temperature

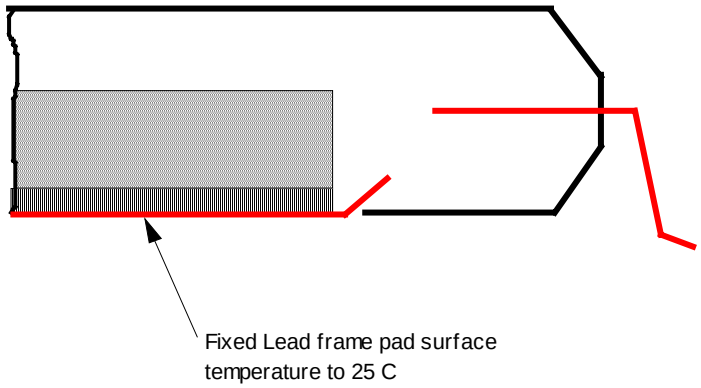
Junction-to-top of package (Ψ_{JT}):

- (Highest Device Temp. - Highest Package Surface Temp.)/Power
- Extracted graphically from θ_{JA} solution

Junction-to-case (θ_{JC}):

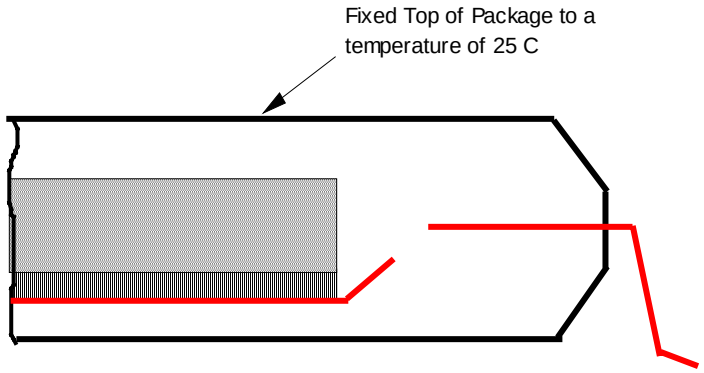
- For the PowerPAD package, the board was removed and the bottom of the pad set to a fixed temperature of 25 ^{o}C (Figure 16).

Figure 16. PowerPAD θ_{JC} Measurement



For the standard package, the board was removed and the top of the package was set to 25 ^{o}C (Figure 17).

Figure 17. Standard Package θ_{JC} Measurement



Results

The purpose of the thermal modeling analysis was to estimate the increase in performance that could be achieved by using the PowerPAD package over a standard package. For this package comparison, several conditions were examined:

Case 1. PowerPAD soldered to the TI recommended board

Case 2. PowerPAD not soldered to the TI recommended board

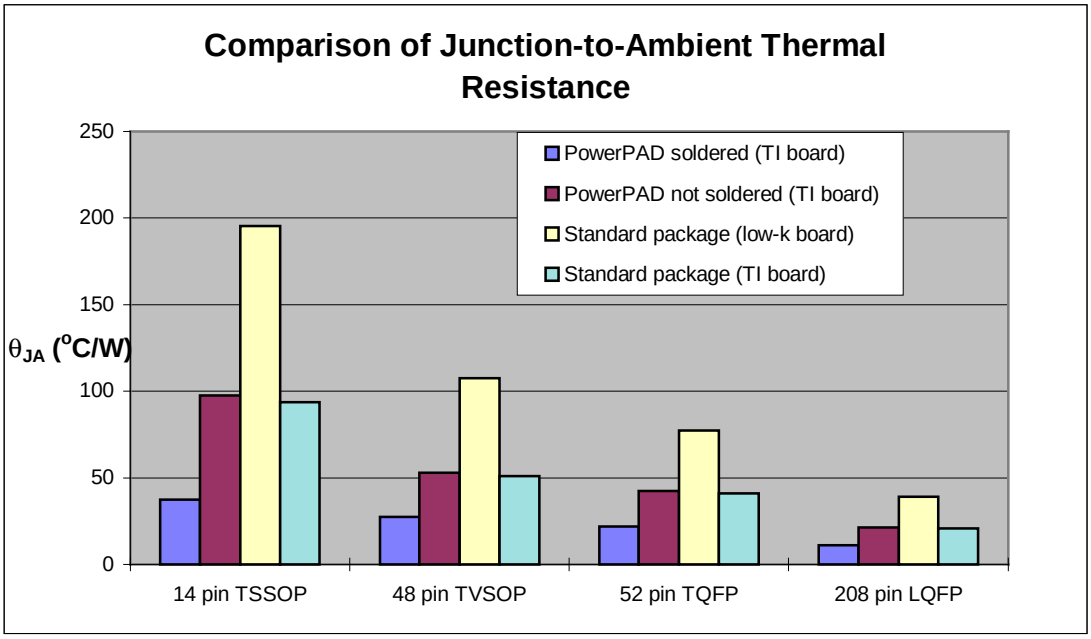
Case 3. A standard package configuration on a low-k board

Case 4. A standard package on the TI recommended board

The first three cases show a comparison of PowerPAD packages on the recommended board to standard packages on a board commonly used in the industry. The results are shown in Table 6. From these results, it was shown that the PowerPAD, when soldered to the TI recommended board, performed an average of 47% cooler than when not soldered, and 73% cooler than a standard package on a low-k board.

For the final case, a separate analysis was performed in order to show the difference in thermal resistance when the standard and the thermally enhanced packages are used on the same board. The results showed that the PowerPAD, when soldered, performed an average of 44% cooler than the standard package (See Figure 18).

Figure 18. Comparison of θ_{JA} for Various Packages



However, when the PowerPAD is not soldered to the board, similar to a standard package, the θ_{JA} is approximately 3% hotter than a standard package. This is due to the location of the lead frame pad relative to the lead fingers, which is the strongest conduction path in a standard package. Since the pad on a standard package lead frame is closer to the lead fingers, more heat is dissipated through the leads than in the PowerPAD package with its deep downset pad.

Conclusions

The deep downset pad of a PowerPAD package allows for an extensive increase in package performance. Standard packages are limited by using only the leads to transport a majority of the heat away. The addition of a heat sink will improve standard package performance, but greatly increases the cost of a package. The PowerPAD package improves performance, but maintains a low cost. The results of the thermal analysis showed that by soldering the PowerPAD package directly to a board designed to dissipate heat, thermal performance increased approximately 44% over the standard packages used on the same board.

Appendix B. Rework Process for Heat Sink TQFP and TSSOP PowerPAD Packages - from Air-Vac Engineering

Introduction

The addition of bottom side heat sink attachment has enhanced the thermal performance of standard surface mounted devices. This has presented new process requirements to effectively remove, redress, and replace (rework) these devices due to the hidden and massive heat sink, coplanarity issues, and balance of heat to the leads and heat sink. The following is based on rework of the TQFP100 and TSSOP20/24 pin devices.

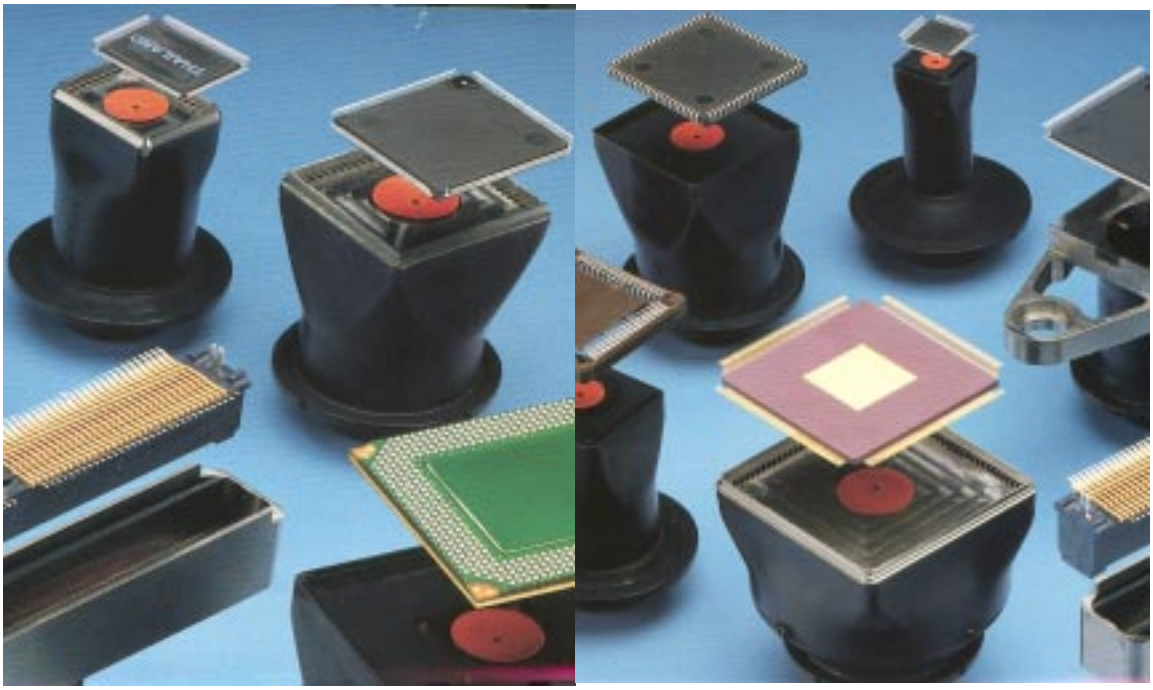
Figure 19. DRS22C Reworking Station

Equipment

The equipment used was the Air-Vac Engineering DRS22C hot gas reflow module. The key requirements for the heat sink applications include: stable PCB platform with sufficient bottom side preheat, alignment capabilities, very accurate heat control, and proper nozzle design.

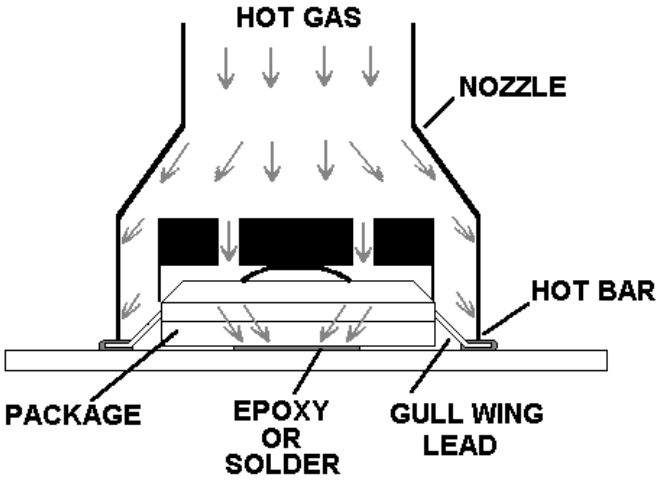
PCB support is critical to reduce assembly sagging and to provide a stable, flat condition throughout the process. The robust convection-based area heater provides sufficient and accurate bottom side heat to reduce thermal gradient, minimize local PCB warpage, and compensate for the heat sink thermal characteristics. The unique pop-up feature allows visible access to the PCB with multiple easy position board supports.

Figure 20. Reworking Nozzles of Various Sizes



During removal, alignment, and replacement, the device is held and positioned by a combination hot gas/hot bar nozzle. Built-in nozzle tooling positions the device correctly to the heat flow. A vacuum cup holds the component in place. Hot gas is applied to the top of the device while hot gas/hot bar heating is applied to the component leads. The hot bar feature also insures bonding of the fine pitch leads.

Figure 21. Nozzle Configuration



Profile

The gas temperature, flow, and operator step-by-step instructions are controlled by an established profile. This allows complete process repeatability and control with minimal operator involvement. Very accurate, low gas flow is required to insure proper temperature control of the package and to achieve good solder joint quality.

Removal

The assembly is preheated to 75 ^{o}C. While the assembly continued to preheat to 100 ^{o}C, the nozzle is preheated. After the preheat cycle, the nozzle is lowered and the device is heated until reflow occurs. Machine settings: TSSOP 20/24 - 220 ^{o}C at 0.39 scfm gas flow for 50 seconds (preheat) above board level, 220 ^{o}C at 0.39 scfm for 10 seconds. TQFP 100 - 240 ^{o}C at 0.10 scfm for 60 seconds (preheat) above board level, 250 ^{o}C at 0.65 scfm for 15 seconds. The built in vacuum automatically comes on at the end of the cycle and the nozzle is raised. The time to reach reflow was approximately 15 seconds. The component is released automatically allowing the part to fall into an appropriate holder.

Site Redress

After component removal the site must be cleaned of residual solder. This may be done by vacuum desoldering or wick. The site is cleaned with alcohol and lint-free swab. It is critical that the heat sink area be flat to allow proper placement on the leads on new device. Stenciling solder paste is the preferred method to apply new solder. Solder dispensing or reflowing the solder bumps on the pads for the leads may also be an alternative, but reflow (solid mass) of solder to the heat sink is not.

Figure 22. Air-Vac Vision System

Alignment

A replacement device is inserted into the gas nozzle and held by vacuum. The device is raised to allow the optical system to be utilized. The optical system used for alignment consists of a beam-splitting prism combined with an inspection quality stereo microscope or camera/video system. the leads of the device are superimposed over the corresponding land pattern on the board. This four sided viewing allows quick and accurate operator alignment.

Replacement

Once aligned, the x/y table is locked and the optical system retracts away from the work area. The preheat cycle is activated. The device is then lowered to the board. An automatic multi-step process provides a controlled reflow cycle with repeatable results. Machine settings for TSSOP 20/24: 160 ^{o}C at 0.39 scfm gas flow for 40 seconds (preheat), 220 ^{o}C at 0.39 scfm for 60 seconds above board level, 220 ^{o}C at 0.39 scfm for 10 seconds. For TQFP 100: 100 ^{o}C at 0.78 scfm for 40 seconds (preheat), 240 ^{o}C at 0.10 scfm for 90 seconds above board level, 250 ^{o}C at 0.65 scfm for 15 seconds (2 stages).

Conclusion

Rework of heat sink devices, TQFP and TSSOP, can be successful with attention to the additional issues they present. With respect to proper thermal profiling of the heat sink, die, and lead temperatures, the correct gas nozzle and profile can be developed to meet the requirements of the device and assembly. Existing equipment and nozzle design by Air-Vac can provide the tools and process knowledge to meet the heat sink TQFP and TSSOP rework application.

Appendix C. PowerPAD Process Rework Application Note from Metcal

The following report references six of Texas Instruments' fine pitch, surface mount prototype packages (TSOP20, TSOP56, TSOP24, TQFP100, and TQFP64). The shapes and sizes are not new to the circuit board industry. Normally, I would use Metcal conduction tools to simply remove and replace these components. However, these packages are unique because all packages include a 'dye lead' on the underside of the package. This dye lead cannot be accessed by contact soldering. Therefore, convection rework methods are necessary for component placement.

NOTE:
Conduction tools can be used for removal. But, convection rework techniques are required for placement, and recommended for removal.)

Removal

Conduction (optional): All packages can be removed with Metcal conduction tips. Use the following tips:

Component	Metcal Tip Cartridge	OK Nozzle
TSOP20	SMTC-006	N-S16
TSOP56	SMTC-166	N-TSW32
TSOP24	SMTC-006	N-S16
TQFP100	SMTC-0118	N-P68
TQFP64	SMTC-112	N-P20

The dye lead, which is not in contact with the Metcal tip, will easily reflow as heat passes through the package.

Conduction Procedure

1) Tin the tip, contact all perimeter leads simultaneously, and wait 3-5 seconds for the leads to reflow.

2) Lift the package off the board (surface tension will hold it in the tip cartridge). Dislodge the component from the tip by wiping the tip cartridge on a damp sponge.

Convection Procedure

1) Flux the leads. Preferably, use a liquid RMA/rosin flux. Pre-heat the board at 100C. Use a convection or IR preheater, like the SMW-2201 from OK Industries. The settings 2-4 will generally heat a heavy board to 100° in 60 seconds.

2) Remove the component with the OK Industries FCR hot air system. Use a nozzle that matches the size and shape of the component (see above). With the preheat still on, heat the top of the board for 30-45 seconds on a setting of 3-4 (depending on board thickness and amount of copper in board*).

Since convection is NECESSARY for placement, convection is recommended for removal.

Placement Procedure

1) Pads can be tinned by putting solder paste on the pads and reflowing with hot air. Simply apply a fine bead of solder paste (pink nozzle, 24AWG) to the rows of pads. Be sure to apply very little paste. Excessive paste will cause bridging, especially with fine pitch components.

2) Once the pads are tinned, apply gel flux (or liquid flux) to the pads. RMA flux is preferable. Be sure to apply gel flux to the dye pad as well. It is important that your pads not be OVER tinned. If too much solder has formed on the dye pad, the component will sit above the perimeter leads, causing co-planarity problems. The gel flux is tacky and helps with manual placement. The joints require very little solder, so stenciling is not necessary. The pads are so thin that a minimal amount of solder is needed to form a good joint. Use a hot air nozzle for the FCR system. Pre-heat the board and (setting 3-5). Use low air flow (5-10 liters/minute) and topside heat (setting 3-4) for about 30-45 seconds*.

NOTES:

The quality of the dye lead's solder joint cannot be visually inspected. An X-ray machine, cross sectioning, or electrical testing will be required.

The vias on the test board are not solder masked very well which causes some bridging and solder wicking.

*Specific board and component temperatures will vary from board to board and from nozzle to nozzle. Larger nozzles require a higher setting because the heat must travel farther away from the heat source. There will be a slight convection cooling effect from pushing hot air through long flutes, and depending on how wide the nozzle is. However, as a rule, keep the board temperature at 100 °C (as thermocoupled from the TOP). You can regulate the board temperature by setting the temperature knob on the bottom side pre-heater. Apply a HIGHER topside heat from the FCR heating head. As a rule, use a maximum of 200-210°C for a short peak period (10 seconds). Look for the flux to burn off. For board profiling purposes, you can visually inspect the condition of the solder joints during the removal process. Note the time allotted for reflow and set the system to Auto Remove or Auto Place at the same time designation for good repeatability. Be sure not to overheat the joints. Excessive heat can cause board delamination and discoloration. Alignment will 'self-correct' once all the solder has reflowed. Tap board lightly. Remove any solder bridges with solder braid. Also, limit the board's heating cycles to a minimum. Excessive heat shock may warp the board or cause cracking in the solder joints.