- **12-Bit ADC With 4 Multiplexed Inputs**
- **Wide Supply Voltage Range 2.6 V to 5.5 V**
- **Low Power Consumption at V_{DD} = 3 V**
  - **0.1 μA in Off Mode (Typ)**
  - **4 μA in Done Mode (Typ)**
  - **80 μA in Active Mode Without A/D Conversions (Typ)**
  - **300 μA in Active Mode With A/D Conversions (Typ)**
- **On-Board 4-Multiplex 56-Segment LCD Driver**
- **Easy Analog Interface From 0.2 × SV_{DD} to 0.4 × SV_{DD} Analog Input Range**
- **On-Board Ratiometric Current Source Programmable From 0.15 mA × (SV_{DD}/V) to 2.4 mA × (SV_{DD}/V)**
- **Two Independent 32.768-kHz Crystal Controlled Timers**
- **Internal MOS Oscillator Serves as System Clock**
- **Programmable Microcontroller**
- **960 Bits of Static RAM With 12 Internal Data Storage Registers**
- **Simple and Easy Programming With SMPL™ Macro Language**
- **4K Bytes of ROM Preprogrammed With**
  - **SMPL™ Macro Language Interpreter**
  - **Memory Bank Switching**

description

The TSS400-S2 sensor signal processor is an ultra-low power, intelligent, 12-bit analog-to-digital converter (ADC) that has been preprogrammed with the Sensor Macro Programming Language (SMPL™) interpreter. This language allows fast, easy, and economical customization of the TSS400-S2 to a wide range of sensor signal processing applications. Some of the typical applications include:

- Temperature measurements with calculating, controlling, and warning features
- Pressure and acceleration measurements
- Timers with control functions
- Intelligent keyboard and display drivers

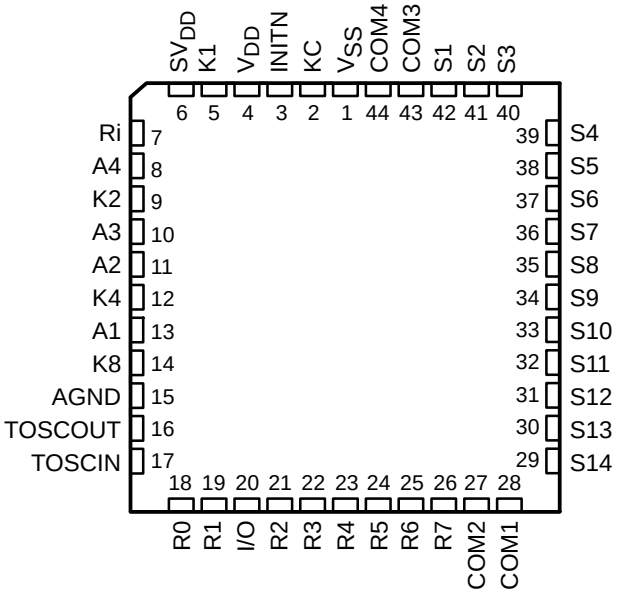
The application-specific programs that customize the operation of the TSS400-S2 are stored in external EEPROMs along with additional data required by the application. The main components of the TSS400-S2 are a four-input multiplexed 12-bit ADC, a programmable constant-current source, an LCD driver capable of driving 56 segments using a four-multiplex drive scheme, two crystal-controlled independent timers, an on-board RAM, six output-only terminals (R1 to R6), a 4-bit programmable I/O port (K1, K2, K4, K8), and I^2C serial EEPROM communications. Using the TSS400-S2 is very easy because it is controlled by a SMPL language program. These programs can be stored in an external EEPROM (stand-alone mode) or stored in a host computer (slave mode). The SMPL language is a powerful, easy-to-learn, and easy-to-use macro language. Some SMPL language features include single-command EEPROM read and EEPROM write operations, three levels of subroutines, a single-command A/D conversion instruction that specifies the numbers of conversions and the types of conversions (either compensated or noncompensated), and two reduced power consumption modes (done and off).

AVAILABLE OPTIONS

T_A	PACKAGE
	44-PIN PLCC (FN)
0°C to 70°C	TSS400CFN-S2
–40°C to 105°C	TSS400QFN-S2

SMPL is a trademark of Texas Instruments Incorporated.

FN PACKAGE
(TOP VIEW)

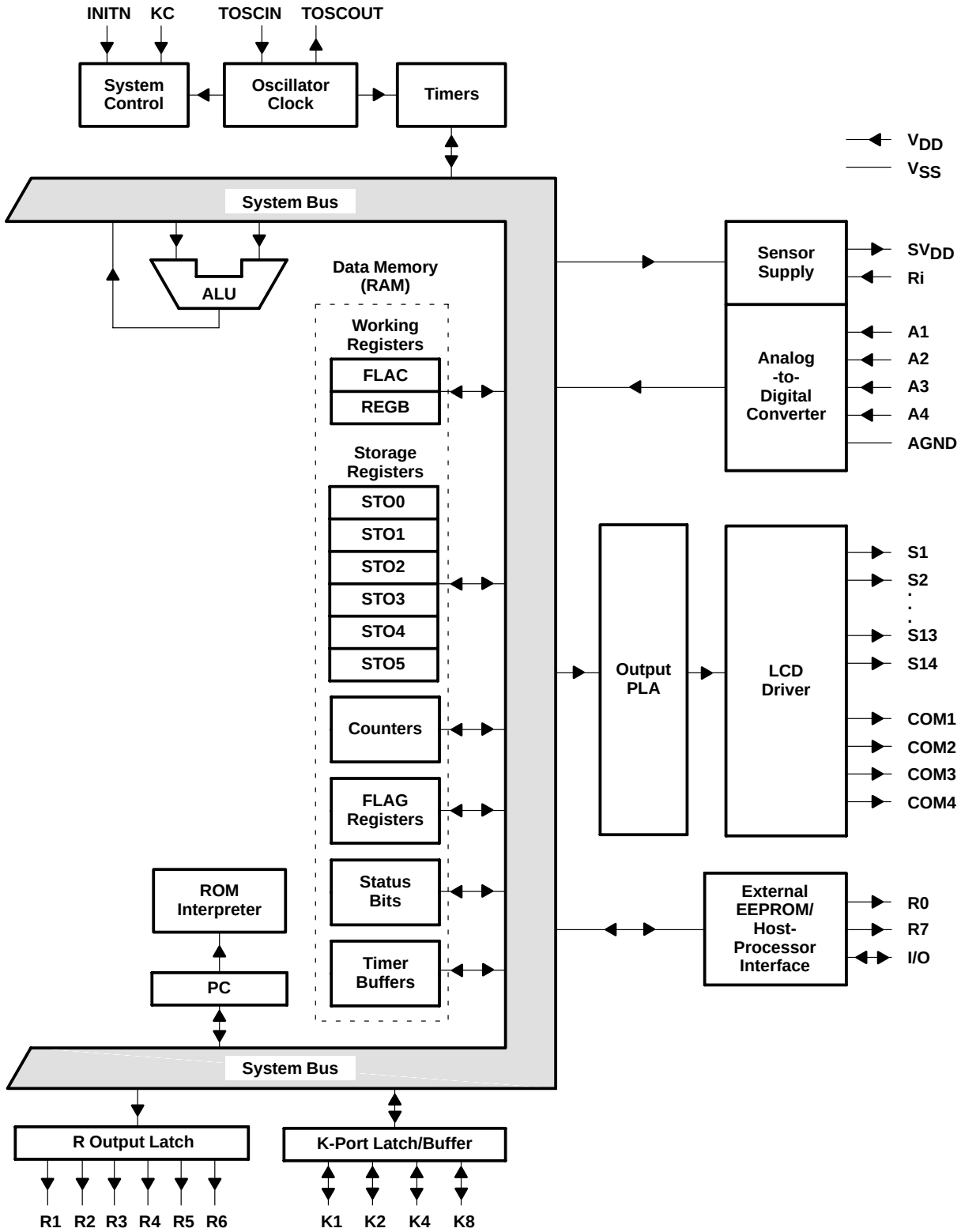


Terminal Functions

PIN NAME	PIN NUMBER	I/O	DESCRIPTION
A1, A2, A3, A4	13, 11, 10, 8	I	Analog inputs for the ADC
AGND	15		Analog ground
COM1, COM2, COM3, COM4	28, 27, 43, 44	O	LCD commons
I/O	20	I/O	Communication input/output
INITN	3	I	Initialization. INITN is normally tied to V_{DD} and held high. If INITN is held low for more than 10 μs, the TSS400-S2 begins a warm start.
K1, K2, K4, K8	5, 9, 12, 14	I/O	4-bit programmable parallel input/output port
KC	2		Test. This terminal must be tied to V_{SS} during normal operation.
R0†	18	O	Controls the EEPROM clock
R1, R2, R3, R4, R5, R6	19, 21–25	O	Digital outputs
R7†	26	O	Controls EEPROM power switch
Ri	7		Current source (programming resistor connection)
S1–S14	42–29	O	LCD segments
SV_{DD}	6		Switchable V_{DD}
TOSCIN	17	I	Oscillator input. TOSCIN is the input connection for the crystal oscillator (32.768 kHz).
TOSCOUT	16	O	Oscillator output. TOSCOUT is the output connection for the crystal oscillator (32.768 kHz).
V_{DD}	4		Power supply
V_{SS}	1		Ground

† Not directly accessible by the user's program

functional block diagram



description (continued)

The TSS400-S2 is designed to meet a wide variety of sensor systems applications including those that require short time-to-market and rapid and/or frequent programming updates. The TSS400-S2 does not require mask programming. It can be purchased in any quantity. Typical applications include:

- Measurements of temperature, pressure, acceleration, gas content, magnetic field, relative humidity, speed, direction, and volume
- Measurements requiring calculation, control, and/or warning functions
- Measurements where temperature compensation is required for accuracy
- Measurements where software calibration and linearization is desirable

These sensor systems can be found in many types of applications including home appliances, industrial control subsystems, HVAC systems and instrumentation, portable instrumentation, consumer products, automotive products, or where precise (12-bit), ultra-low power (12 μA–15 μA typ), intelligent A/D conversion is essential.

The TSS400-S2 is available in two temperature ranges. The TSS400CFN-S2 is characterized for operation from 0°C to 70°C. The TSS400QFN-S2 is characterized for operation from –40°C to 105°C.

initialization and power up

Initialization is started by hardware in two ways:

- Power Up: The voltage V_{DD} is switched on (cold start). The CPU starts to work at PC 000 after the internal oscillator has started operation. This may take from 1 to 6 seconds.
- INITN: INITN is held low (switched to ground) for more than 10 μs. When this occurs during program execution, it is called a warm start. The CPU starts operation at PC 000 when INITN is released to V_{DD} potential.

Table 1 lists the TSS400-S2 register contents after a power up or an INITN-terminal initialization.

Table 1. Register Contents

REGISTER	POWER UP (COLD START)	INITN TERMINAL (WARM START)
Program counter (PC)	000	000
Status bits POS, NEG, and ZERO	undefined	unchanged
RAM contents †	reset to 0	unchanged
Digit latches (DLn)	reset to 0	reset to 0
K lines' latch contents	undefined	unchanged
Timers	0	unchanged
ADC voltage SV_{DD}	switched off	switched off
LCD segment latches	undefined	unchanged
Subroutine stack	level 0	level 0

† Despite the RAM remaining unchanged during a warm start, the memory addressed when INITN is activated may be destroyed by a write cycle.

initialization and power up (continued)

If the TSS400-S2 system is battery powered and contains calibration factors or other important data in RAM, it is advisable to distinguish between cold start and warm start. The reason is the possibility of initializations caused by electromagnetic inductance (EMI). If such an erroneous initialization is not tested for legality, EMI influence could destroy the RAM contents by clearing the RAM with the initialization software routine. The TSS400-S2 compares two reserved RAM nibbles to see if they contain $A5_{16}$ after each initialization:

- If the RAM nibbles contain the expected information ($A5_{16}$), initialization continues at PC 000. The RAM contents are not changed. This means that a spurious signal caused the initialization (warm start).
- If the RAM nibbles differ from $A5_{16}$, the RAM is cleared and the program continues at PC 000. This means that the TSS400-S2 supply voltage was switched on (cold start).

The short timer and the long timer are not stopped by a warm start. This means that they remain active and must be stopped by a STPTIMx instruction, if necessary.

operating conditions

The TSS400-S2 has four different modes of operation: off, done, active without A/D conversion, and active with A/D conversion. The off mode conserves the most power. In this mode, only the RAM and the outputs (I/O, R outputs, and K lines) are maintained. The TSS400-S2 enters off mode with a software command and is awakened via the K lines or by initialization. Table 2 lists the conditions needed for the K lines to awaken the processor.

Table 2. K-Line Wake-Up Conditions

K8		K4		K2		K1	CONDITION
0	.AND.	0	.AND.	0	.AND.	0	condition before wake up
1	.OR.	1	.OR.	1	.OR.	1	condition to wake up processor
1	.AND.	0	.AND.	0	.AND.	0	condition before wake up
0	.OR.	1	.OR.	1	.OR.	1	condition to wake up processor

The done mode is also a low-power mode. In the done mode, the RAM, the outputs, and the display are maintained and the timekeeping circuits remain active. The device enters done mode with a software command and is awakened via the K lines, initialization, or with a wake up by internal timers.

When the TSS400-S2 is executing instructions, it is in the active mode. This mode can be broken into two separate states: with A/D conversion and without A/D conversion. All portions of the TSS400-S2 are fully operational in the active mode with A/D conversion. The A/D-conversion circuitry is powered down only in the active mode without A/D conversion. See Figure 1 for a state diagram of the TSS400-S2 operational modes.

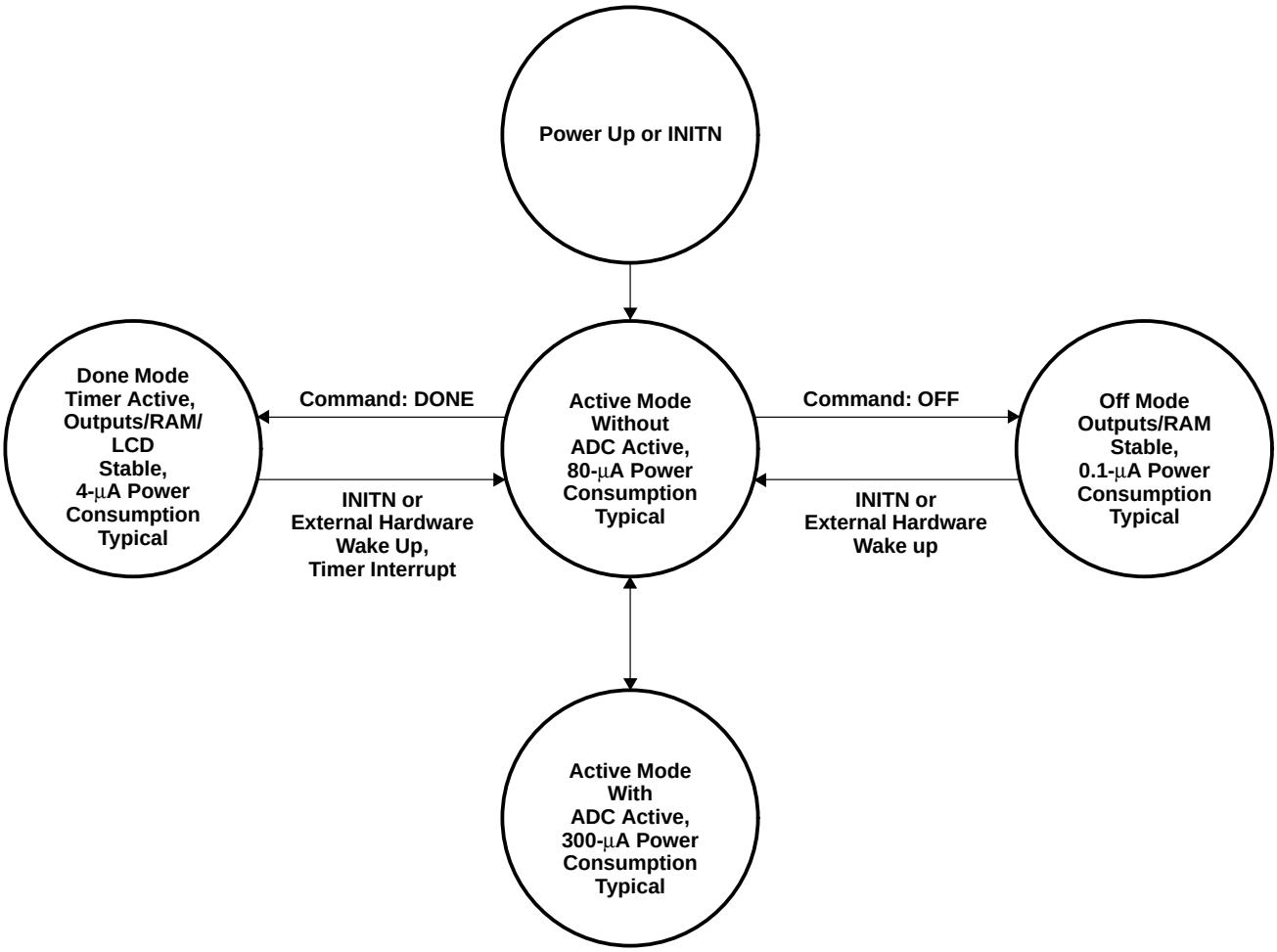


Figure 1. State Diagram for TSS400-S2 Operational Modes

analog-to-digital converter (ADC) (see Figure 2)

The TSS400-S2 offers a 12-bit ratiometric successive-approximation ADC. Sensors are interfaced to this converter via the four multiplexed analog inputs (A1–A4). The analog conversion operation is executed with the MEASR instruction. The SMPL interpreter automatically switches the internal digit latches DL9, DL10, and DL11 such that the ADC is connected to the analog input line specified by the MEASR operand. Table 3 lists the instructions required to access all four analog inputs.

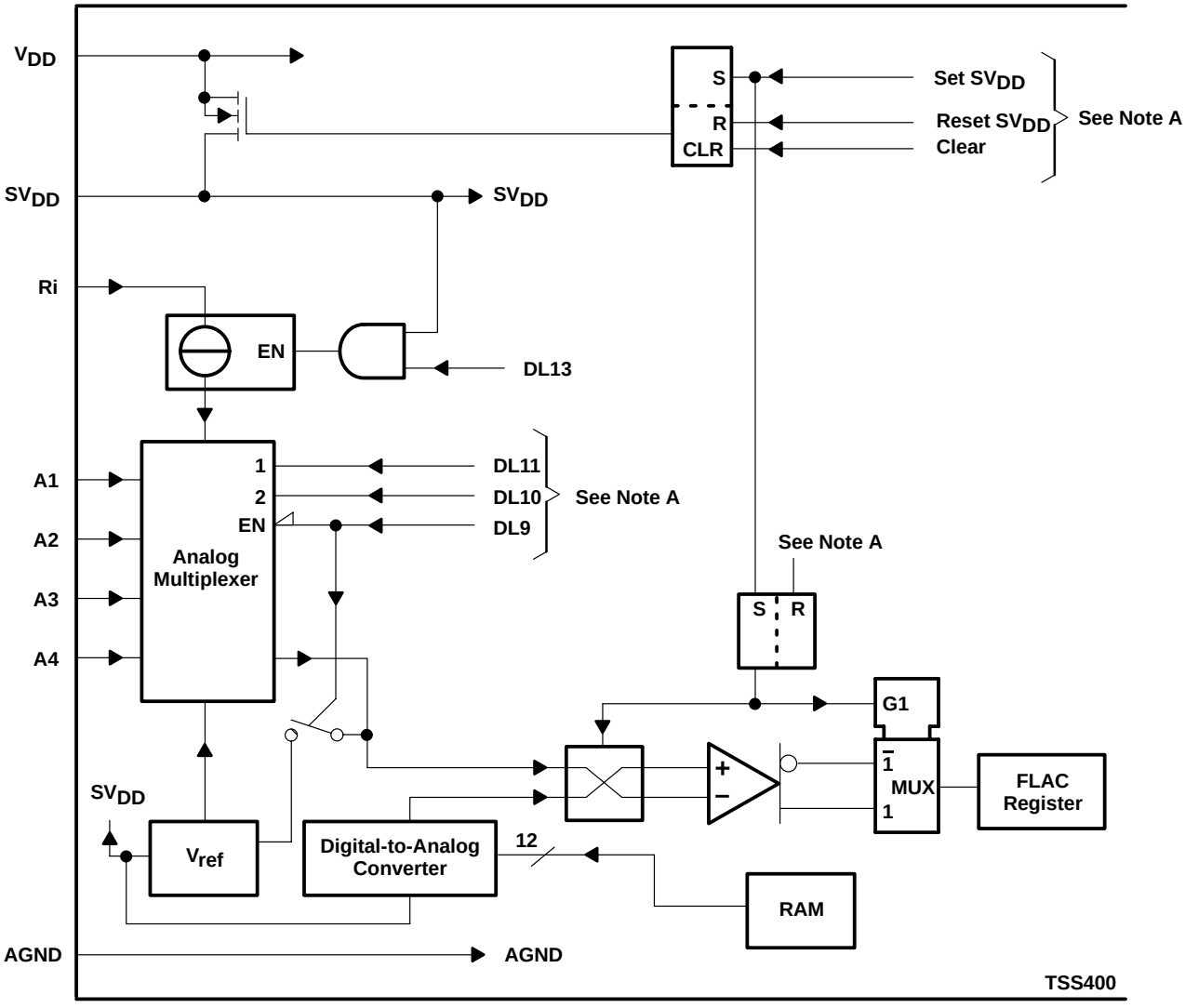
Table 3. Instructions Required to Access Analog Inputs

INSTRUCTION	OPERAND	DL9	DL10	DL11	ACTION
MEASR	0	0	1	0	Connect A1 to the ADC
MEASR	1	0	0	0	Connect A2 to the ADC
MEASR	2	0	1	1	Connect A3 to the ADC
MEASR	3	0	0	1	Connect A4 to the ADC
CHKBATT	X	1	X	X	Check current supply voltage against value in FLAC
ADJBATT	X	1	X	X	Set minimum supply voltage point

analog-to-digital converter (ADC) (continued)

The interpreter automatically switches on the switched-sensor supply voltage (SV_{DD}) just prior to making the A/D conversion and switches it off immediately after the conversion is complete. The MEASR instruction is followed by a BYTE instruction. The operand of the BYTE instruction specifies the number of conversions to be made and whether the conversions are to be compensated or noncompensated. A noncompensated measurement is a single A/D conversion. A compensated measurement is defined as a measurement wherein two conversions are made, one conversion with the ADC comparator connected normally and the other conversion with the comparator inputs reversed. The two results are added together so comparator offsets cancel. The interpreter automatically takes care of all required switching to perform the specified type of conversion.

Absolute measurements are possible if SV_{DD} is held constant. This requires a stable V_{DD} during the conversion and constant loading of SV_{DD}. The ADC measures the ratio of the input voltage at the analog input (V_{DD}) to the switched-sensor supply voltage (SV_{DD}) and not absolute voltages. This ensures that the measurement of the sensors is independent of the supply voltage.



NOTE A: These signals are automatically controlled by the interpreter during A/D conversion.

Figure 2. ADC Functional Block Diagram

measurement range and conversion formulas

The analog input range is the same for all four analog outputs, A1 to A4. The nominal properties of the ADC range and the equations associated with them are listed below:

$$V_I = (A + B \times N) \times SV_{DD}$$

where:

V_I = unknown analog input voltage
A = converter count for $V_I = 0$
= 0.231271438 for the TSS400-S2
B = delta in $\mu V/SV_{DD}$ for a 1-bit difference in conversion result
= 0.000043048228 for the TSS400-S2
N = A/D conversion result for a single measurement
SV_{DD} = switched-sensor supply voltage

For the TSS400-S2, the analog input voltage is:

$$V_I = (0.231271438 + 0.000043048228 \times N) \times SV_{DD}$$

For multiple measurements, the V_I equation becomes:

$$V_I = \left(A + \frac{B \times N}{M}\right) \times SV_{DD}$$

$$= \frac{\left(\left(0.231271438 \times SV_{DD}\right) + (0.000043048228 \times N)\right) \times SV_{DD}}{M}$$

where:

M = the number of measurements taken

Since a conversion result of 0 is used to indicate an underrange input and FFF_{16} is used to indicate an overrange input, the usable range for N (in a single measurement) is:

$$1_{16} \le N \le FFE_{16}$$

or in decimal format:

$$1 \le N \le 4094$$

The minimum measurable analog input voltage to SV_{DD} ratio is:

$$V_I min = \frac{V_I}{SV_{DD}} \text{ when } N = 1$$

$$= \frac{(0.231271438 + 0.000043048228) \times \cancel{SV_{DD}}}{\cancel{SV_{DD}}}$$

$$= 0.237968$$

The maximum measurable analog input voltage to SV_{DD} ratio is:

$$V_I max = \frac{V_I}{SV_{DD}} \text{ when } N = 4094$$

$$= \frac{(0.231271438 + 0.000043048288 \times 4094) \times \cancel{SV_{DD}}}{\cancel{SV_{DD}}}$$

$$= 0.400839$$

The allowable analog input voltage range for V_I is:

$$0.231314 \times SV_{DD} \le V_I \le 0.407511 \times SV_{DD}$$

measurement range and conversion formulas (continued)

If the input voltage is below the lower limit ($V_I$min), the value 000_{16} is returned. If the input voltage is above the upper limit ($V_I$max), the value FFF_{16} is returned. The NEG status bit is set in both cases. The ZERO status bit is set if 000_{16} is returned.

battery check

Since the TSS400-S2 is ideal for battery applications, an internal supply voltage check is available. This operation is executed by the instructions ADJBATT and CHKBATT. ADJBATT measures the internal reference voltage and puts the results in the FLAC register. By setting the supply voltage at a minimum acceptable level and executing the ADJBATT instruction, a representative value is placed in the FLAC register. Saving this number in a storage register or EEPROM location enables it to be recalled for use by the CHKBATT instruction when the current supply voltage needs to be checked against the preset acceptable minimum. To perform these operations, an internal stable reference is connected to the input of the ADC and a measurement is made. Due to the ratiometric nature of the conversion, the measured value is an indication of the TSS400-S2 supply voltage. The ADJBATT instruction performs this operation and stores the result in the FLAC register. The CHKBATT instruction performs the same operation but compares the resulting measurement to the number in the FLAC register and sets the positive (POS) and negative (NEG) status bits according to the result.

programmable current source

A programmable current source ratiometric to SV_{DD} is available for supplying a fixed current to the analog sensors. When turned on, the current source sends a constant current out of the addressed analog input (An). The voltage generated by the external sensor is measured with the same An input. The voltage used for A/D conversions and the reference voltage (V_{ref}) used to set the current of the current source are both proportional to SV_{DD} and have a fixed ratio to one another. This ensures optimum tracking. The current source is activated by digit latch DL13. When DL13 is set to 1 and SV_{DD} is on, the current source is on. When DL13 is set to 0, the current source is off. Figure 3 shows a diagram of the programmable current source.

The current I is programmed by an external resistor R_{ext}, which is connected between SV_{DD} and Ri. This current is given by the following equation:

$$I_{An} = \frac{V_{Rext}}{R_{ext}}$$

V_{Rext} is approximately $0.24 \times SV_{DD}$

The programmable current range that the current source can supply to the ADC input is:

0.15 mA to 2.4 mA $\times$ (SV_{DD}/V)

$$V_I = I_{An} \times R_I$$

with R_I = sensor resistance

$$V_I = V_{Rext} \times \frac{R_I}{R_{ext}}$$

programmable current source (continued)

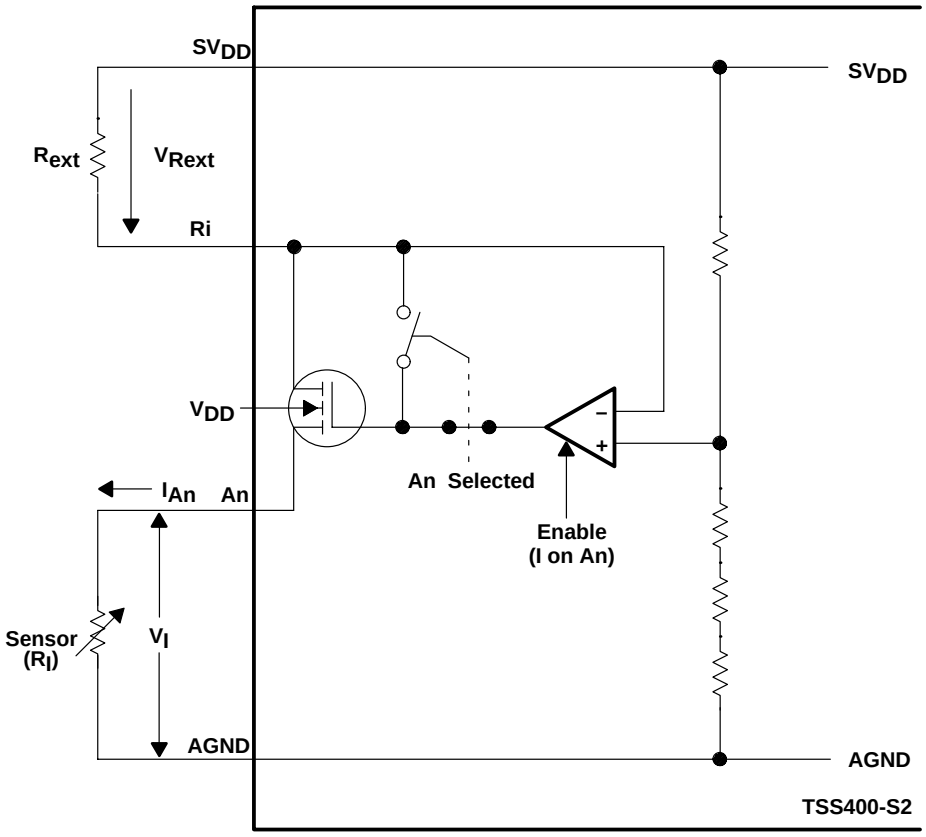


Figure 3. Programmable Current Source Diagram

timers

Two independent crystal-controlled timers are available on the TSS400-S2. Each timer requires a 32.768-kHz crystal that allows very accurate time measurements and clock functions to be performed. These timers function at 1 Hz and 16 Hz and can be used as a wake-up signal from the done mode of operation in addition to the other timing functions. The crystal is also used to control the LCD driver circuitry.

counters

Two decimal counters, counter 1 and counter 2, are available for use on the TSS400-S2. The individual counters range from 0 to 99. They can also be cascaded together for a range of 0 to 9999. Counter 1 is the least significant part of the combined counter. After the counters are incremented or decremented, the ZERO status bit is set when the counter reaches zero or reset if the counter is not zero.

EEPROM addressing

The TSS400-S2 provides the option to address up to 128K bytes of external EEPROM. The entire address space of the TSS400-S2 is separated into banks. Each bank has an address space of 2048 bytes. To select individual banks, an external multiplexer or an analog switch must be connected to the R outputs. Control of the multiplexer is done with the R1–R6 outputs. Table 4 lists the hardware addresses within a bank as defined by the logic levels of terminals A1 and A2.

EEPROM addressing (continued)

Table 4. EEPROM Hardware Addresses

EEPROM PINS		ADDRESS SPACE
A2	A1	
0	0	0 — 511 (0_{16} — $1FF_{16}$)
0	1	512 — 1023 (200_{16} — $3FF_{16}$)
1	0	1024 — 1535 (400_{16} — $5FF_{16}$)
1	1	1536 — 2047 (600_{16} — $7FF_{16}$)

Jumps from one EEPROM bank to another are done with the CHAPTER instruction. The I/O line is directed via a multiplexer or an analog switch to one selected chapter. The chapter is selected by the R outputs R1–R6. It is important to have pullup resistors connected to the EEPROM data lines to generate a defined level in case a bank is not selected.

After initialization, the default bank is 0 (all R outputs are set to 0). All jumps, conditional jumps, calls, burn EEPROM commands, and reads EEPROM commands are performed in the selected EEPROM bank. Figure 4 shows the EEPROM connections for the TSS400-S2.

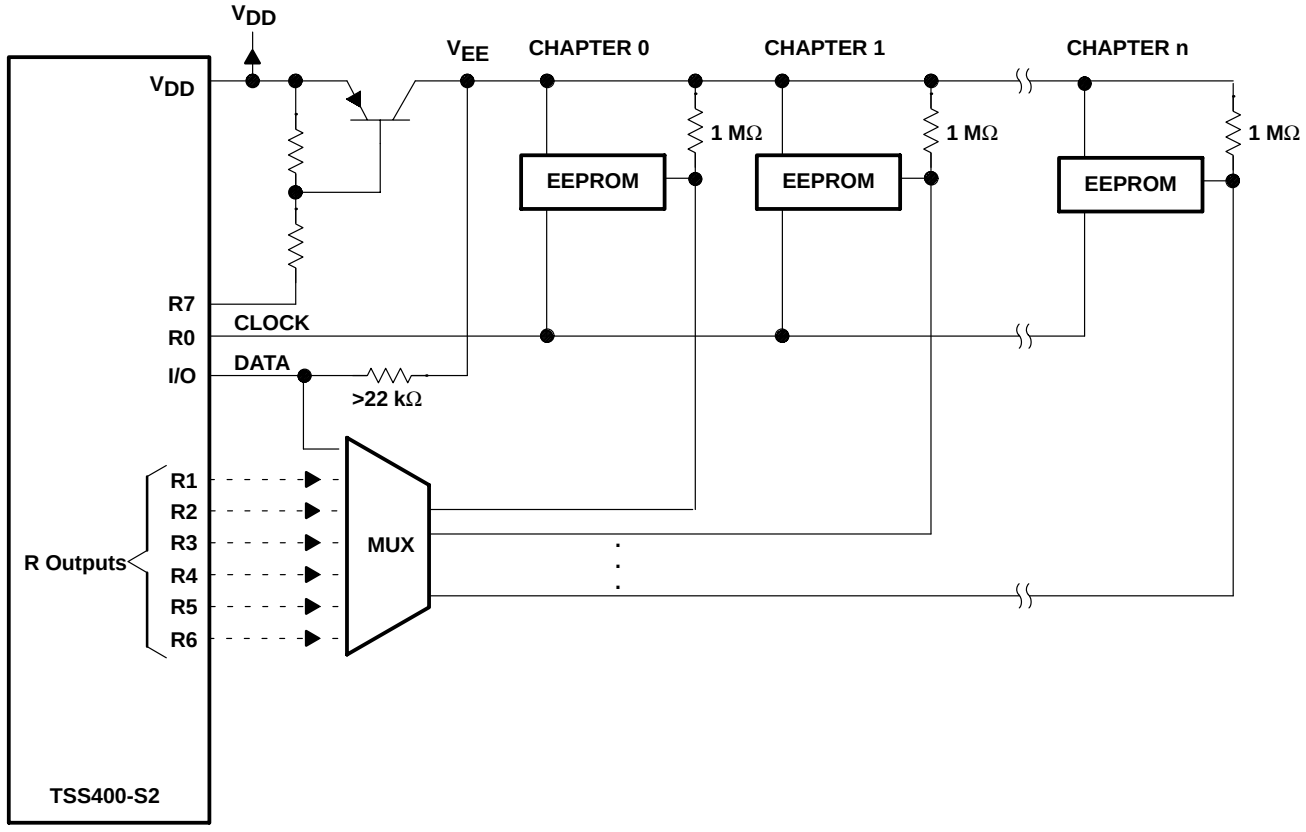


Figure 4. EEPROM Connections for the TSS400-S2

implemented bus structure

The TSS400-S2 has a multislave bus system built into the interpreter code. This bus system allows a unidirectional communication on a two-wire bus line (e.g., Meter-Bus). This bus line can be an ordinary twisted-pair telephone-type cable. Data can be sent from the slave to the master on request of the master. Asynchronous data transmission can also be initiated from a slave on its own if the bus is active. For example, this is done when the slave measures a value that has to invoke an alarm. To connect a slave module based on the TSS400-S2, it is recommended that a Texas Instruments TSS721 interface circuit be used. Figure 5 shows the bus structure topology.

A remote read out of a slave module is performed with the ENBUS instruction. The ENBUS instruction causes the master to generate a high-to-low transmission on K1. This tells the TSS400-S2 slave to send out the contents of STO1 through STO5 in a specific time frame. Each frame is determined by the unique bus address of each slave module. The data transfer then proceeds according to a specified protocol.

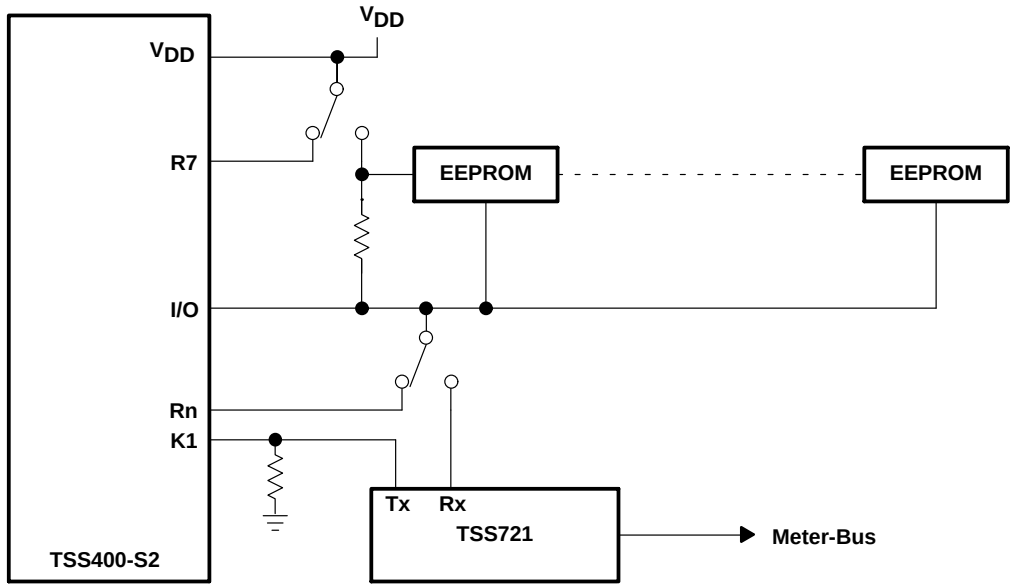


Figure 5. Bus Structure Topology

RAM usage

The RAM size of the TSS400-S2 is enlarged to 960 bits. The 960-bit matrix is organized in 15 RAM banks each containing 16 four-bit nibbles. The first 14 of these RAM banks are normal RAM banks. The last RAM bank is a special direct-access memory (DAM) bank. The RAM also includes the FLAC, REGB, storage, and flag registers.

FLAC register

The FLAC register is the main working register of the TSS400-S2. It consists of eight nibbles for the number, one nibble for the sign, and two flags that are used internally by arithmetic routines. The sign bit is set to zero for positive numbers and one for negative numbers. The following diagram shows the format of the FLAC register:

10E7	10E6	10E5	10E4	10E3	10E2	10E1	10E0	Sign and Flags
Most Significant Nibble					Least Significant Nibble			Sign

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FLAC register (continued)

The FLAC register is used for:

- Receiving the result of an A/D conversion.
- Storing the results of all arithmetic and logic operations.
- Holding the first operand for arithmetic and logic operations.
- Containing the result of a hexadecimal-to-decimal conversion.
- Holding information for transfer to the EEPROM.
- Holding information to be displayed on the LCD.

REGB register

The REGB register is the second working register. It consists of eight nibbles for the number and one nibble for the sign. The format of the REGB register is the same as the FLAC register. The REGB register is used for:

- Holding the second operand for arithmetic and logic operations.
- Holding constants read from the EEPROM.
- Holding contents after transfers from the counters.

storage registers

The TSS400-S2 has 12 general-purpose storage registers. These storage registers have the same format as the FLAC register, each with eight nibbles for the number and one nibble for the sign.

The first six storage registers are addressable by using the names STO0 to STO5. Use of the STO0 register is restricted since it is also used by the device during multiplication, division, and hexadecimal-to-decimal conversions. After multiplication and hexadecimal-to-decimal conversion operations, the contents of STO0 are set to 0; after a division, STO0 contains the remainder of the operation. This remainder can be used in conversions (e.g., minutes to hours).

The other six storage registers (STO6 – STO11) are called expanded storage registers. To access the expanded storage registers, the statement EXPAND has to be used in conjunction with the mnemonic (see Table 8 for more information on the EXPAND instruction).

NOTE: To access the expanded storage registers in the software simulator, use the function key F3 of the window function.

flag registers

Two general-purpose flag register groups, each with 16 flags, have been set aside. They are named group 1 and group 2. The selection of the groups is made with the SMPL instructions SELGRP1 and SELGRP2. The group selected is in use until the other group is selected. Each of the 16 flags in each group may be set, reset, and tested. The contents of the flags can then be used to control program flow, define the action of jumps, indicate errors in hardware function, and for any other user-defined purpose. The use of some of the flags is restricted since their operation has been predefined. Table 5 lists the assigned use of each flag.

Table 5. Flag Assignment

GROUP 1 FLAGS				GROUP 2 FLAGS			
FLAG	DEFINITION	FLAG	DEFINITION	FLAG	DEFINITION	FLAG	DEFINITION
0	Arbitrary	8	Arbitrary	0	Arbitrary	8	Arbitrary
1	Seg. H1 information	9	Arbitrary	1	Arbitrary	9	Arbitrary
2	Seg. H2 information	10	Long timer	2	Arbitrary	10	Arbitrary
3	Seg. H3 information	11	Short timer	3	Arbitrary	11	Arbitrary
4	Seg. H4 information	12	K1 buffer	4	Arbitrary	12	Arbitrary
5	Seg. H5 information	13	K2 buffer	5	Arbitrary	13	Arbitrary
6	Seg. H6 information	14	K4 buffer	6	Arbitrary	14	Arbitrary
7	Seg. H7 information	15	K8 buffer	7	Arbitrary	15	Arbitrary

R outputs and digit latches

Outputs R1 through R6 are available as general-purpose outputs. They can be used for scanning keyboards or switches, for controlling relays, lamps, LCDs, etc., or for digital communications using buffers, multiplexers, etc., as required by the designer. The R0 and R7 outputs cannot be addressed by the software. They are used by the interpreter when EEPROM reads or writes are performed. R0 performs as the clock connection, and R7 switches the supply voltage to the EEPROM as required to conserve system power.

The TSS400-S2 contains 14 one-bit digit latches (DL0 through DL13) that (except for DL0 and DL7) can be set and reset independently with software. These digit latches can be separated into two distinct groups, those with external outputs (DL0 through DL7) and those without external outputs (DL8 through DL13). The digit latches without external outputs (DL8 through DL13) each control a unique hardware function. Table 6 gives the digit-latch names and the hardware functions they control.

Table 6. Digit-Latch Names and Hardware Functions

DIGIT LATCH	HARDWARE FUNCTION			
DL0	Not user addressable. R0 is the clock for the EEPROM.			
DL1–DL6	6 R outputs (R1–R6) for general use			
DL7	Not user addressable. R7 is the power switch for the EEPROM.			
DL8	0	Sets K port to input		
	1	Sets K port to output		
DL9–DL11†	**DL9**	**DL10**	**DL11**	**Addressed Analog Input Connected to the ADC**
	0	0	0	A1
	0	1	0	A2
	0	0	1	A3
	0	1	1	A4
	1	X	X	Battery-check functions
DL12	0	1-Hz timer input into the ALU for timer instructions		
	1	16-Hz timer input into the ALU for timer instructions		
DL13	0	Constant-current source of the ADC off		
	1	Constant-current source of the ADC. This signal is on if SV_{DD} is on.		

† It is not normally necessary to change these digit latches with software since the interpreter controls them automatically.

K port

The K port is a 4-bit programmable I/O port with individual lines labeled K1, K2, K4, and K8. The direction of data flow through the K lines is controlled by digit latch DL8. Data to be output through the K lines is first stored in the 4-bit K-lines latch. The K-port output structure is open source. For data input, the K lines are read via Schmitt triggers into the ALU. If the TSS400-S2 has been placed in either the off or done mode, it is possible to use the K lines to generate a wake-up signal.

status logic

The status logic consists of three bits that are modified after the execution of specific instructions. The status bits are checked by conditional jumps that are executed or not executed depending on the state of the tested status bit. Not every instruction rewrites the status bits. If an instruction does not affect the status bits, the status of the last instruction to rewrite the status bits is preserved. The following diagram shows the three bits making up the status logic.

POS	NEG	ZERO

POS bit

The POS bit is set after an arithmetic instruction if the result of the operation has a positive sign. If the result is negative, the POS bit is reset. Other instructions set the POS bit if no error occurred, thus making it possible to use the POS bit status as an error indicator. If the A/D measurement is within range, the POS bit is set.

NEG bit

The NEG bit is set after an arithmetic instruction if the result of the operation has a negative sign. If the result is positive, the NEG bit is reset. Other instructions set the NEG bit if an error occurred, thus making it possible to use the NEG bit status as an error indicator. If the A/D measurement is out of range, the NEG bit is set.

ZERO bit

The ZERO bit is set to one if the result of the last instruction is zero or if a comparison results in equality. If the result is not zero or the comparison is not equal, the ZERO bit is cleared. If the A/D measurement is under range, the ZERO bit is set.

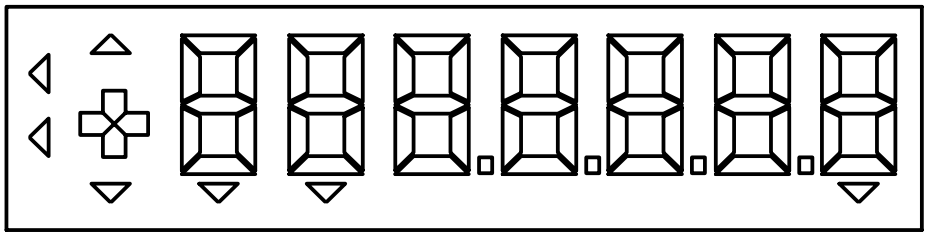
LCD driver

The TSS400-S2 contains LCD-driver circuitry that is designed to get the best results for a wide range of applications. From a software point of view, the 4-input multiplexed 56-segment LCD driver looks very simple. No timing problems exist with multiplexing for getting a quiet, stable display. The LCD-driver-hardware outputs display information automatically without any software burden during the active and done modes of operation. Software has only to decide which segment information is to be displayed and in which digit to display it.

NOTE: LCDs are available for prototype development. Contact the nearest TI sales office for more information.

digit addressing

The FLAC's most significant nibble (10E7) cannot be displayed because of the 7-digit configuration of the display driver. If it is necessary to display the most significant nibble, a shift right (SHIFTR) with decimal correction of the FLAC contents has to be done. The following diagram shows the TSS400-S2 display configuration and accompanying FLAC nibbles, and Figure 6 shows the odd and even selects.



FLAC NIBBLE	10E7	10E6	10E5	10E4	10E3	10E2	10E1	10E0
SELECTS	—	S1/S2	S3/S4	S5/S6	S7/S8	S9/S10	S11/S12	S13/S14
DIGIT n	—	1	2	3	4	5	6	7

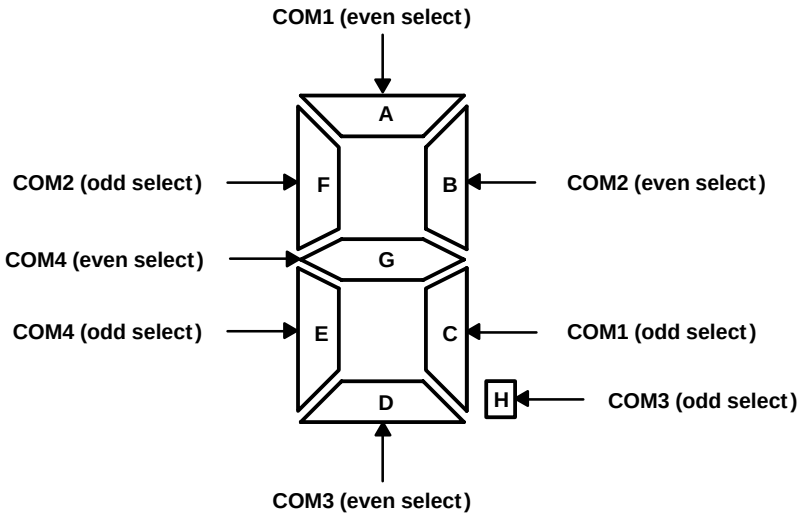


Figure 6. LCD Odd and Even Selects

segment addressing

The OPLA (output programmable logic array) definition is based on the following hardware configuration.

SELECT LINES								COMMON			
								1	2	3	4
ODD SELECT	S1	S3	S5	S7	S9	S11	S13	C	F	H	E
EVEN SELECT	S2	S4	S6	S8	S10	S12	S14	A	B	D	G
LCD DIGIT	1	2	3	4	5	6	7				

Caution: The common/select definition shown cannot be modified, and any display chosen to be used with the TSS400-S2 must conform to the shown definition.

segment addressing (continued)

The chosen common/select configuration is designed to be fail safe. This means that no valid numbers or characters are displayed when a segment or common signal failure occurs. Instead, meaningless segment combinations are displayed that cannot be mistaken as valid data.

The TSS400-S2 LCD driver contains a gate-level OPLA that is a 64 × 7 bit configuration. The seven bits represent the segment information A through G for 64 predefined combinations (the H segment is independent of the OPLA and is given with the display instructions). Each of the predefined characters can be used with the display command. Table 7 gives the segments displayed and the character for each.

Table 7. Segments Display and Character

CHARACTER NUMBER	SEGMENTS	CHARACTER	DISPLAYED SEGMENTS
0	A B C D E F	0 or O	0
1	B C	1 or |	1
2	A B D E G	2	2
3	A B C D G	3	3
4	B C F G	4	4
5	A C D F G	5 or S	5
6	A C D E F G	6	6
7	A B C	7	7
8	A B C D E F G	8 or B	8
9	A B C D F G	9	9
10	A B C E F G	A or R	A
11	C D E F G	b	b
12	A D E F	C or [	C
13	B C D E G	d	d
14	A D E F G	E	E
15	A E F G	F	F
16	None	Blank	
17	B C D	J	J
18	D E F	L	L
19	A B E F G	P	P
20	B C D E F	U	U
21	D E G	c	c
22	C E F G	h	h
23	D E	l	l
24	C E G	n	n
25	C D E G	o	o
26	E G	r	r

Table 7. Segments Display and Character (Continued)

CHARACTER NUMBER	SEGMENTS	CHARACTER	DISPLAYED SEGMENTS
27	D E F G	t	
28	C D E	v	
29	B C D F G	Y	
30	B C E F G	H	
31	B C G	–1	
32	None	Blank	
33	A		
34	F		
35	A F		
36	B		
37	A B		
38	BF		
39	A B F		
40	G	Minus Sign	
41	A G		
42	F G		
43	A F G		
44	B G		
45	A B G		
46	B F G		
47	A B F G	Degree	
48	E		
49	A E		
50	E F		
51	A E F		
52	B E		
53	A B E		
54	B E F		
55	A B E F		
56	E G		
57	A E G		
58	E F G		
59	A E F G	F	
60	C		
61	D		
62	A B C D	]	
63	A B C D E	J	

sensor macro programming language (SMPL)

The TSS400-S2 features a processor that is programmed with an easy-to-use macro language (SMPL). The internal ROM is preprogrammed with optimized calibration, display, A/D-conversion routines, the SMPL macro interpreter, and EEPROM communications protocol. The TSS400-S2 SMPL language is an optimized 89-instruction language that is easier to use than assembly language. Each SMPL instruction is equivalent, on average, to six or seven assembly language instructions. This greatly reduces the amount of memory space required to store a given program and eases programming tasks.

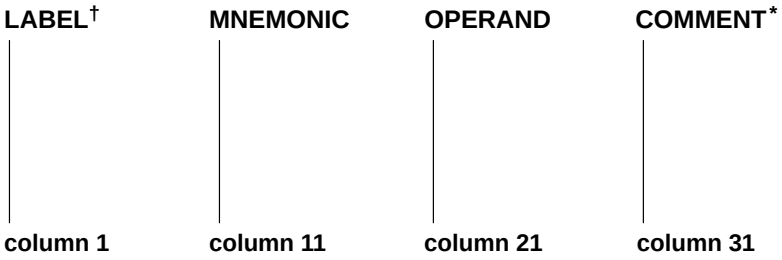
SMPL interpreter instruction coding format

The following rules should be followed in writing a program:

- Label fields are a maximum of eight alphanumeric characters, starting with an alphabetic character. The label field must begin in column one.
- The mnemonic is to the right of a label and must be separated by at least one blank space. If no label is used, the mnemonic begins after the first column (second column or further right).
- The operand is to the right of the mnemonic and must be separated by at least one blank.
- A comment must start to the right of the operand and be separated by at least one blank. If a comment occupies a separate line, it must begin with an asterisk (*) in column one.

For legibility, it is recommended that fields begin in the following columns:

- Label fields must begin in column 1
- Mnemonics should begin in column 11
- Operands should begin in column 21
- Comments to an instruction should begin in column 31
- Full-line comments must begin with an asterisk (*) in column 1



† Labels are 8 characters max and must start in column 1.
* An asterisk in column 1 reserves the entire line for a comment.

Table 8 lists the SMPL language programming instructions in each of the following major categories:

- Register-to-register transfer instructions
- Arithmetic instructions
- Arithmetic compare instructions
- Bit-manipulation instructions
- Counter instructions
- Display instructions
- Miscellaneous instructions
- Constant-transfer instructions
- Timer instructions
- Input/output instructions
- Program flow control instructions
- A/D-conversion instructions

Table 8. SMPL Programming Instructions

FUNCTION GROUP	SMPL INSTRUCTION		DESCRIPTION
Register-to-Register Transfer	MOVFLSTO	n	Move FLAC to storage register n
	MOVSTOFL	n	Move storage register n to FLAC
	MOVRBSTO	n	Move REGB to storage register n
	MOVSTORB	n	Move storage register n to REGB
	EXCHRBFL		Exchange REGB and FLAC registers
	MOVFLRB		Move FLAC register to REGB register
	MOVRBFL		Move REGB register to FLAC register
	MOVFLPRM	label	Move FLAC to EEPROM starting at address label
	MOVPRMRB	label	Move EEPROM contents starting at address label to REGB
	PRMMODER	a+n	Move n number of bytes to read index with a incrementing registers from EEPROM
	PRMMODEW	a + n	Move n number of bytes to write index with a incrementing registers to EEPROM
	EXPAND MOVRBSTO	n	Move REGB into an expanded storage register
	EXPAND MOVSTORB	n	Move expanded storage register into REGB
	EXPAND MOVFLSTO	n	Move FLAC into an expanded storage register
	EXPAND MOVSTOFL	n	Move expanded storage register into FLAC
Arithmetic	ADD		Add REGB to FLAC decimally
	SUB		Subtract REGB from FLAC decimally
	MPY		Multiply FLAC and REGB decimally
	DIV		Divide FLAC by REGB decimally
	ADDH		Add REGB to FLAC hexadecimally
	SUBH		Subtract REGB from FLAC hexadecimally
	HEXDEC		Hexadecimal-to-decimal conversion
	ROUND n		Round FLAC n times (0<n<5)
	SHIFTR n		Shift right FLAC n times (0<n<3)
	SHIFTL n		Shift left FLAC n times (0<n<3)
Arithmetic Compare	CMPFLRB		Compare FLAC and REGB then set status flags
	TSTRB		Test contents of REGB then set status flags
	CMPIXR	>N	Compare read index to value N then set status flags
	CMPIXW	>N	Compare write index to value N then set status flags
Bit Manipulation	SBIT	n	Set flag bit n (0 ≤ n<16)
	RBIT	n	Reset flag bit n (0 ≤ n<16)
	TBIT	n	Test flag bit (0 ≤ n<16)
	SELGRP n		Select flag bits group n (0<n<3)
	OR		Logical OR FLAC and REGB with result to FLAC
	AND		Logical AND FLAC and REGB with result to FLAC
Counter	DECCNT n		Decrement counter n decimally
	INCCNT n		Increment counter n decimally
	DECDBL		Decrement double counter decimally
	INCDBL		Increment double counter decimally
	LDCNT n	>NN	Load counter n decimally with constant >NN
	MOVCNT n		Move counter n to REGB
	MOVDBL		Move combined counters to REGB

Table 8. SMPL Programming Instructions (Continued)

FUNCTION GROUP	SMPL INSTRUCTION		DESCRIPTION
Display	DISPLDG n	>NN	Display information of operand NN in digit n
	DISPLCLR		Clear display
	DISPLFL	>MN	Display FLAC from digit M to digit N and append (M−N+1) bytes containing information for each digit
Constant Transfer	LDFLPOS	n	Load FLAC with a positive constant (BCD format) contained in the n following bytes (n = 0 : 4 Bytes)
	LDFLNEG	n	Load FLAC with a negative constant (BCD format) contained in the n following bytes (n = 0 : 4 Bytes)
	LDRBPOS	n	Load REGB with a positive constant (BCD format) contained in the n following bytes (n = 0 : 4 Bytes)
	LDRBNEG	n	Load REGB with a negative constant (BCD format) contained in the n following bytes (n = 0 : 4 Bytes)
	CLRFL		Clear FLAC register
	CLRRB		Clear REGB
	CLRRAM		Clear RAM
Timer	LDTIML	NNN	Load long timer with constant NNN
	LDTIMS	NNN	Load short timer with constant NNN
	ACTTIM		Actualize timers
	STPTIML		Stop long timer
	STPTIMS		Stop short timer
Input/Output	SETR	n	Set output Rn (DLn)
	RSTR	n	Reset output Rn (DLn)
	TSTKEY	>NN	Test keyboard like described by operand
	KINTIM		Actualize K input and timers
	KIN		Read K inputs to FLAC (LSD) and FLAG 12 thru 15
	FLKOUT		Output LSD of FLAC to K lines
	KOUT	n	Output constant n to K lines
	ROUT	>N	Transfer constant to R Ports
	FLROUT		Output LSD of FLAC to R Ports
Program-Flow Control	JMP	label	Jump to label unconditionally
	JZ	label	Jump to label if zero (Status Bit ZERO = 1)
	JEQ	label	Jump to label if equal (status bit ZERO = 1)
	JNZ	label	Jump to label if not zero (status bit ZERO = 0)
	JNE	label	Jump to label if not equal (status bit ZERO = 0)
	JP	label	Jump to label if positive (status bit POS = 1)
	JN	label	Jump to label if negative (status bit NEG = 1)
	CALL	label	Call subroutine label
	RETN		Return from subroutine
A/D Conversion	SVDDON		Set converter supply voltage
	SVDDOFF		Reset converter supply voltage
	MEASR BYTE	a n	Measure addressed A/D input a+1 and following BYTE contains n number of conversions and mode
	ADJBATT		Measure battery voltage and put result in FLAC
	CHKBATT		Check battery voltage
	ADJCOMP		Measure A/D input and put result in FLAC
	CHKCOMP		Compare A/D input with value in FLAC

Table 8. SMPL Programming Instructions (Continued)

FUNCTION GROUP	SMPL INSTRUCTION		DESCRIPTION
Miscellaneous	DONE		Enter done mode
	OFF		Enter off mode
	NOP		No operation
	SLV	>NN	Host control instruction
	CHAPTER	>VXY	Switches the I/O line that data is transferred to and from the EEPROM
	ENBUS	x	Enable bus capability as background program via Rn
	DISBUS		Disable bus capability

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.3 V to 7 V
Input voltage range, V_I . . . . . V_{SS} –0.3 V to V_{DD} +0.3 V
Diode current . . . . . ± 2 mA
Operating free-air temperature range, T_A: TSS400CFN-S2 . . . . . 0°C to 70°C
TSS400QFN-S2 . . . . . –40°C to 105°C
Storage temperature range . . . . . –50°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The voltage value is measured with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.6	3	5.5	V
Supply voltage, V_{SS}		0	0	0	V
Timer frequency (XTAL)			32.768		kHz
Operating free-air temperature, T_A	TSS400CFN-S2	0	25	70	°C
	TSS400QFN-S2	–40	25	105	°C

electrical characteristics, T_A = 0°C to 70°C (unless otherwise noted)

total device supply current

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(active)}$	Supply current, active mode	With A/D†	V_{DD} = 3 V		300	500	μA
			V_{DD} = 3 V, T_A = –40°C to 105°C		300	500	
			V_{DD} = 5 V		800	1100	
			V_{DD} = 5 V, T_A = –40°C to 105°C		800	1400	
		Without A/D†	V_{DD} = 3 V		80	140	μA
			V_{DD} = 3 V, T_A = –40°C to 105°C		80	140	
			V_{DD} = 5 V		400	500	
			V_{DD} = 5 V, T_A = –40°C to 105°C		520	650	
$I_{DD(done)}$	Supply current, done mode	Standby†	V_{DD} = 3 V		4	8	μA
			V_{DD} = 3 V, T_A = –40°C to 105°C		6	9	
			V_{DD} = 5 V		10	18	
			V_{DD} = 5 V, T_A = –40°C to 105°C		12	20	
$I_{DD(off)}$	Supply current, off mode	Halt†	V_{DD} = 3 V		0.1	1	μA
			V_{DD} = 3 V, T_A = –40°C to 105°C		0.1	1	
			V_{DD} = 5 V		0.1	1	
			V_{DD} = 5 V, T_A = –40°C to 105°C		0.1	1	

† Current values are for input levels in the range of 0 to 0.3 V for $V_{IK(L)}$, $V_{IO(L)}$, and V_{DD} – 0.3 V for $V_{IK(H)}$, $V_{IO(H)}$ (all outputs open).

K and I/O inputs (Schmitt trigger)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_{DD} = 3 V		1.5	2	V
		V_{DD} = 5 V		2.7	3.9	
$V_{T–}$	Negative-going threshold voltage	V_{DD} = 3 V		0.8	1.5	
		V_{DD} = 5 V		1	1.9	
	Hysteresis (V_{T+} – $V_{T–}$)	V_{DD} = 3 V		0.4	1.4	V
		V_{DD} = 5 V		0.8	2.9	
I_I	Input current	V_{DD} = 3.8 V,	V_I = 0	–0.1	0.1	μA
		V_{DD} = 5.5 V,	V_I = 0	–0.1	0.1	
		V_{DD} = 3.8 V,	V_I = V_{DD}	–0.1	0.1	
		V_{DD} = 5.5 V,	V_I = V_{DD}	–0.1	0.1	

K outputs

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = 3 V,	I_{OH} = –0.1 mA	V_{DD} – 0.2	V_{DD}	V
		V_{DD} = 3 V,	I_{OH} = –0.3 mA	V_{DD} – 0.6	V_{DD}	
		V_{DD} = 5 V,	I_{OH} = –0.5 mA	V_{DD} – 0.6	V_{DD}	

I/O output

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = 3 V,	I_{OH} = –0.1 mA	V_{DD} –0.2	V_{DD}	V
		V_{DD} = 3 V,	I_{OH} = –0.3 mA	V_{DD} –0.6	V_{DD}	
		V_{DD} = 5 V,	I_{OH} = –0.75 mA	V_{DD} –0.6	V_{DD}	
V_{OL}	Low-level output voltage	V_{DD} = 3 V,	I_{OL}= 0.5 mA	V_{SS}	V_{SS} +0.4	V
		V_{DD} = 5 V,	I_{OL}= 1 mA	V_{SS}	V_{SS} +0.4	

electrical characteristics, T_A = 0°C to 70°C (continued)

R outputs

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$V_{OH(R)}$	High-level output voltage, R output	V_{DD} = 3 V,	I_{OH} = –0.1 mA	V_{DD} –0.2	V_{DD}	V
		V_{DD} = 3 V,	I_{OH} = –0.3 mA	V_{DD} –0.6	V_{DD}	
		V_{DD} = 5 V,	I_{OH} = –0.3 mA	V_{DD} –0.4	V_{DD}	
$V_{OL(R)}$	Low-level output voltage, R output	V_{DD} = 3 V,	I_{OL} = 0.3 mA	V_{SS}	V_{SS} +0.4	V
		V_{DD} = 5 V,	I_{OL} = 0.3 mA	V_{SS}	V_{SS} +0.4	

INITN input

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$I_{I(INITN)}$	Input current, INITN	V_{DD} = 3 V,	V_I = 0	–0.2	–1	μA
		V_{DD} = 5 V,	V_I = 0	–0.5	–2.2	
		V_{DD} = 3.8 V to 5.5 V,	V_I = V_{DD}	–0.1	0.1	

SV_{DD} output

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_O	Output voltage, switched V_{DD}	V_{DD} = 2.6 V,	I_{SVDD} = 2 mA	V_{DD} –0.2	V_{DD}	V
		V_{DD} = 2.6 V,	I_{SVDD} = 6.5 mA	V_{DD} –0.3	V_{DD}	
I_O	Output current, switched V_{DD}	V_{DD} = 3.8 V to 5.5 V,	SV_{DD} off (0 V)	–0.1	0.1	μA

LCD lines: common and segment (1/4 duty cycle)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{DD} = 3 V,	I_{OH} = –50 μA	V_{DD} –0.4		V_{DD}	V
		V_{DD} = 5 V,	I_{OH} = –100 μA	V_{DD} –0.4		V_{DD}	
V_O	Output voltage, (2/3) V_{DD}	V_{DD} = 3 V,	I_{OZ} = ±10 nA	(2/3) V_{DD} –0.04	(2/3) V_{DD}	(2/3) V_{DD} +0.04	V
		V_{DD} = 5 V,	I_{OZ} = ±10 nA	(2/3) V_{DD} –0.04	(2/3) V_{DD}	(2/3) V_{DD} +0.04	
V_O	Output voltage, (1/3) V_{DD}	V_{DD} = 3 V,	I_{OZ} = ±10 nA	(1/3) V_{DD} –0.04	(1/3) V_{DD}	(1/3) V_{DD} +0.04	V
		V_{DD} = 5 V,	I_{OZ} = ±10 nA	(1/3) V_{DD} –0.04	(1/3) V_{DD}	(1/3) V_{DD} +0.04	
V_{OL}	Low-level output voltage	V_{DD} = 3 V,	I_{OL} = 50 μA	V_{SS}		V_{SS}+0.4	V
		V_{DD} = 5 V,	I_{OL} = 100 μA	V_{SS}		V_{SS}+0.4	

electrical characteristics, T_A = 0°C to 70°C (continued)

ADC current source, $V_{Rext} = V_{SVDD} - V_{Ri}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(Rext)}$	Voltage (across programming resistor)†	V_{DD} = 3.5 V, I_{Ri} = 1.3 mA, T_A = 25°C	0.236635 × SV_{DD}	0.240238 × SV_{DD}	0.243843 × SV_{DD}	V
		V_{DD} = 5 V, I_{Ri} = 1.3 mA, T_A = 25°C	0.237836 × SV_{DD}	0.240238 × SV_{DD}	0.242641 × SV_{DD}	
$r_{i(Rext)}$	External programming resistor	V_{DD} = 3.5 V, T_A = 25°C	0.1		1.6	kΩ
		V_{DD} = 5 V, T_A = 25°C	0.1		1.6	
	Temperature stability (dN/dT)	V_{DD} = 3 V, V_{Rext}/R_{ext} = 1.3 mA, N = $00A0_{16}$ = 10		0.07		LSB/°C
		V_{DD} = 3 V, V_{Rext}/R_{ext} = 1.3 mA, N = $0F5F_{16}$ = 3935		0.14		
		V_{DD} = 5 V, V_{Rext}/R_{ext} = 1.3 mA, N = $00A0_{16}$ = 10		0.07		
		V_{DD} = 5 V, V_{Rext}/R_{ext} = 1.3 mA, N = $0F5F_{16}$ = 3935		0.14		
	SV_{DD} rejection ratio (dN/dSV_{DD})	V_{DD} = 3 V, T_A = 25°C, N = $00A0_{16}$ = 10	–7	–3.5	2.5	LSB/V
		V_{DD} = 3 V, T_A = 25°C, N = $0F5F_{16}$ = 3935	–14	–7	5	
		V_{DD} = 5 V, T_A = 25°C, N = $00A0_{16}$ = 10	–7	–3.5	2.5	
		V_{DD} = 5 V, T_A = 25°C, N = $0F5F_{16}$ = 3935	–14	–7	5	

ADC

PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
V_{IH}	High-level analog input voltage for A/D conversion	V_{DD} = 3 V, N = $0F5F_{16}$ = 3935	0.398514 × SV_{DD}	0.400666 × SV_{DD}	0.402819 × SV_{DD}	V
		V_{DD} = 5 V, N = $0F5F_{16}$ = 3935	0.398514 × SV_{DD}	0.400666 × SV_{DD}	0.402819 × SV_{DD}	
V_{IL}	Low-level analog input voltage for A/D conversion	V_{DD} = 3 V, N = $00A0_{16}$ = 10	0.236007 × SV_{DD}	0.238159 × SV_{DD}	0.240312 × SV_{DD}	
		V_{DD} = 5 V, N = $00A0_{16}$ = 10	0.236007 × SV_{DD}	0.238159 × SV_{DD}	0.240312 × SV_{DD}	
V_I	Input voltage range for A/D conversion	V_{DD} = 3 V, N = $00A8_{16}$ to $0F5F_{16}$ = 168 to 3935	0.161216 × SV_{DD}	0.162507 × SV_{DD}	0.163799 × SV_{DD}	V
		V_{DD} = 3 V, N = $00A8_{16}$ to $00F5F_{16}$ = 168 to 3935	0.161216 × SV_{DD}	0.162507 × SV_{DD}	0.163799 × SV_{DD}	
I_{IB}	Input bias current (all inputs)†	V_I = V_{SS} to V_{DD}, Current source off			±30	nA

† This range is available only for $V_{DD} \geq 3.5$ V. The A/D range is limited due to the offset of the comparator. The range can be larger if the comparator offset is made smaller.

‡ N = A/D conversion result for a single measurement. See measurement range and conversion formulas.

operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Linearity		V_{DD} = 3 V, DDV ≤ 120 LSB	−1		1	LSB
			V_{DD} = 3 V, 120 LSB < DDV ≤ 240 LSB	−1.5		1.5	
			V_{DD} = 3 V, 240 LSB < DDV ≤ 2600 LSB	−2.5		2.5	
			V_{DD} = 3 V, 2600 LSB < DDV	−4.5		4.5	
			V_{DD} = 5 V, 120 LSB ≥ DDV	−1		1	LSB
			V_{DD} = 5 V, 120 LSB < DDV ≤ 240 LSB	−1.5		1.5	
			V_{DD} = 5 V, 240 LSB < DDV ≤ 2600 LSB	−2.5		2.5	
			V_{DD} = 5 V, 2600 LSB < DDV	−4.5		4.5	
$V_{DD(BC)}$	Supply voltage, battery check		000_{16} < conversion result < FFF_{16}			4.8	V
	Clock frequency, internal MOS		V_{DD} = 3 V, T_A = 25 °C		650		kHz
			V_{DD} = 5 V, T_A = 25 °C		840		
t_c	Conversion time	Single-compensated measurement	V_{DD} = 3.5 V		1.2		ms
		Single-uncompensated measurement	V_{DD} = 3.5 V		1		
		ADJCOMP	V_{DD} = 3.5 V		1		
	Processor frequency, internal (f_{proc})				700		kHz
C_L	Capacitance load	LCD display, any common			1000		pF
		LCD display, any segment			200		
	Internal assembly language instruction execution time†			15	8.5	6	μs

† Macro-command execution times typically require 150 internal assembly instruction executions per byte of macro code read from EEPROM.

TYPICAL CHARACTERISTICS

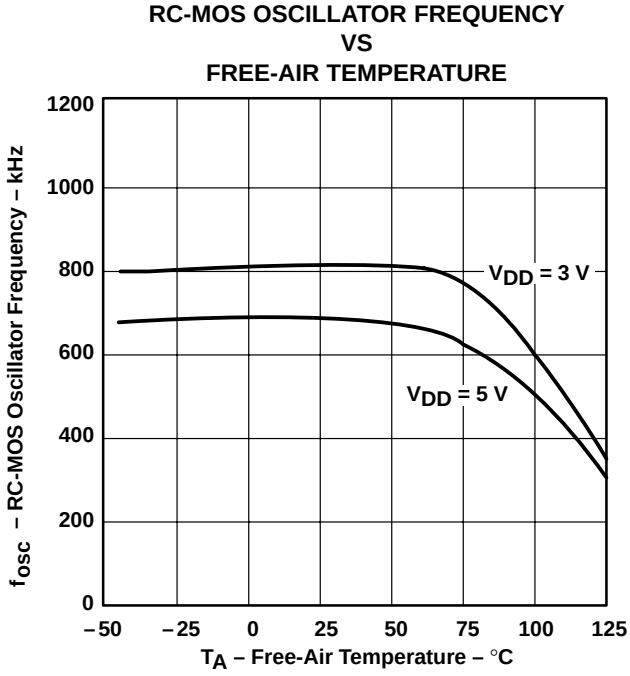


Figure 7

APPLICATION INFORMATION

Figure 8 shows all the components that are necessary to run a TSS400-S2 and the connected sensors for a temperature-calibrated pressure application. In this case, a 3-V lithium battery is used as a power supply. The pressure application could be an altimeter, a pressure gauge, or a manometer. This example uses simple uncalibrated silicon sensors. It is assumed that a simple, easy-to-perform software calibration routine is used to get accurate results. This temperature-compensation software calibration and the 12-bit ADC ensure that a high degree of accuracy can be realized with this application.

All of the analog circuitry in Figure 8 is connected to the SV_{DD} (switchable V_{DD}) terminal. By doing this, the sensor network is only powered when it is needed for A/D conversion. This is done to reduce total system power consumption.

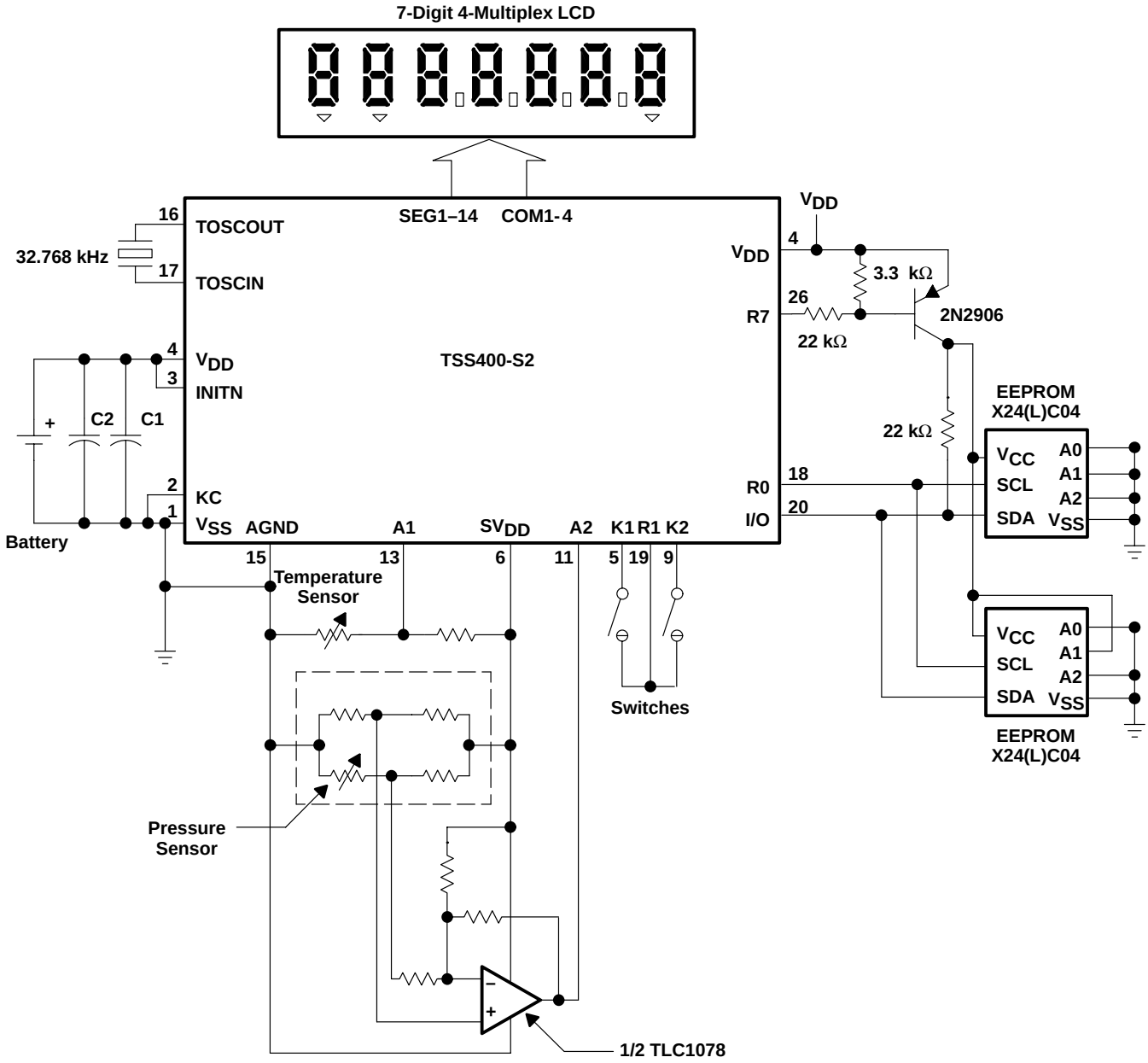


Figure 8. Temperature-Compensated Pressure Application

APPLICATION INFORMATION

SDT-400 development tool

The SDT-400 is an inexpensive software development tool used for development of TSS400-S2 applications. It consists of three basic parts:

- A 5.25-inch floppy diskette that contains the TSS400-S2 software simulator program, the ASM400 SMPL macro language assembler program, and demonstration and example routine programs
- The SDT-400 User's Manual that details how to use the development system and the TSS400-S2
- A hardware development board

The SDT-400 works with an IBM-compatible personal computer and supports program debug at the macro instruction level. It also provides on-screen simulation of the LCD display and most functions of the TSS400-S2. These functions (all internal registers, inputs, outputs, and flags) can be edited on the screen in the simulator with the keyboard. It also provides a burn routine for downloading an application program into the EEPROMs on the hardware development board. The hardware development board has all of the components and connectors required for it to be connected to a personal computer parallel printer port and for it to serve as a prototyping system board for the application under development.

hardware development board

The hardware development board contains a seven-digit LCD display, a 16-key keypad, sockets for four 512 $\times$ 8 EEPROMs, a socket for the TSS400-S2, connectors for the parallel printer port, all supply terminals, input terminals, and output terminals of the TSS400-S2 and an on-board voltage regulator that allows a user to power the system from the personal computer cable, a 9-V transistor battery, or a dc power supply. The development system comes with four EEPROMs, two standard TSS400s, a 3-V LCD, a 5-V LCD, and a cable to connect the development board to the personal computer.

software simulator

The software simulator, which runs on all IBM-AT compatible personal computers, allows fast development of application software for the TSS400-S2. All functions, with the exception of the hardware communication with inputs and outputs, can be simulated. The development of program algorithms requires no hardware. As shown in Figure 9, all internal registers, inputs, outputs, and flags are shown simultaneously on one screen. These may be modified whenever needed, even during simulator's RUN mode from the keyboard. Figure 9 shows the simulator software running on a PC.

APPLICATION INFORMATION

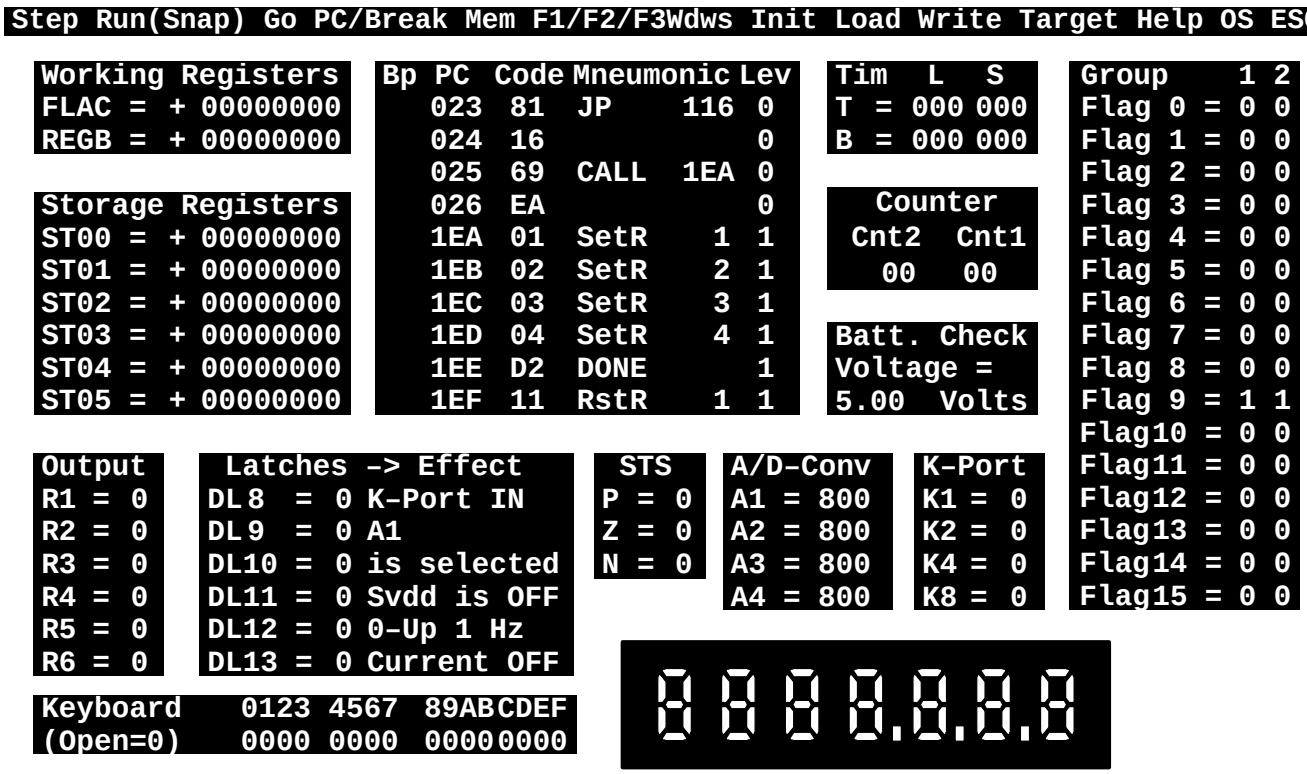


Figure 9. SDT-400 Simulator Screen

real-time debugging

After verification of all software parts that do not need connection to the target hardware, the real-time tests with the development board connected to the target hardware can begin. The development board is connected to the printer port on the personal computer by means of the included cable. The tested user's program is burned into the EEPROMs with the appropriate simulator instruction and reread for verification. The user's program, now stored in the EEPROMs on the development board, can be started and stopped by instructions from the software simulator.

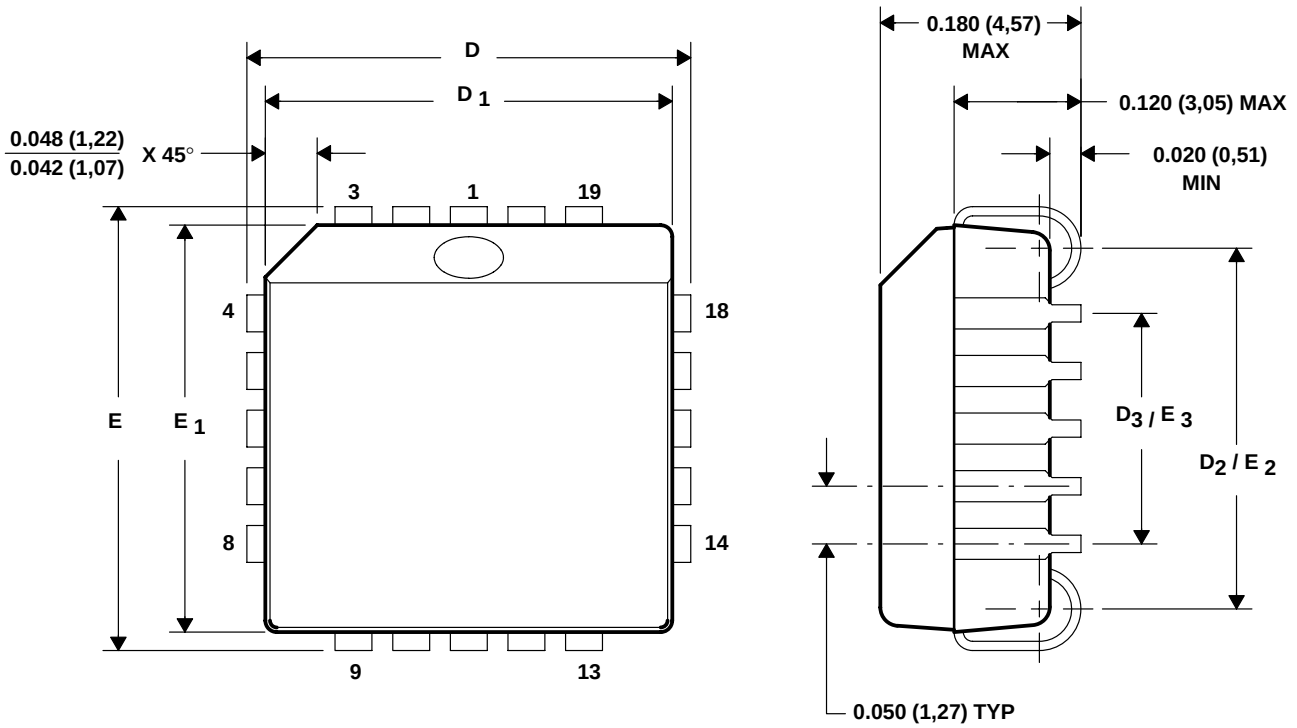
Real-time debugging with the development board is made by inserting pauses into the user's program as desired, usually when some subprogram portion is complete. This can be after computations are complete, A/D conversions are complete, the keyboard has been tested, and so on. The following are several possible locations for the pauses and checking a program:

- Jumps to the same location
- Waits for a definitive key to be pressed
- Displays of the register that contain important information
- Displays of the registers with wait states

MECHANICAL DATA

FN/S-PQCC-J** **PLASTIC J-LEADED CHIP CARRIER**

20-PIN SHOWN



JEDEC OUTLINE	NO. OF PINS**	D / E		D_1 / E_1		D_2 / E_2		D_3 / E_3
		MIN	MAX	MIN	MAX	MIN	MAX	TYP
MO-047AA	20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.290 (7,34)	0.330 (8,38)	0.200 (5,08)
MO-047AB	28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.390 (9,91)	0.430 (10,92)	0.300 (7,62)
MO-047AC	44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.590 (14,99)	0.630 (16,00)	0.500 (12,70)
MO-047AD	52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.690 (17,53)	0.730 (18,54)	0.600 (15,24)
MO-047AE	68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.956 (24,28)	0.890 (22,61)	0.930 (23,62)	0.800 (20,32)
MO-047AF	84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	1.090 (27,69)	1.130 (28,70)	1.000 (25,40)

4040005/A–10/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions D_1 and E_1 do not include mold flash or protrusion. Protrusion shall not exceed 0.010 (0,25) on any side.
D. All dimensions conform to JEDEC Specification MO-047.
E. Maximum deviation from coplanarity is 0.004 (0,10).

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