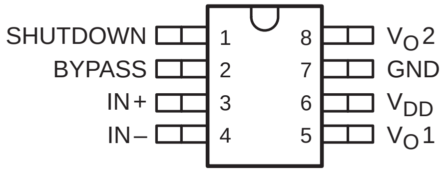
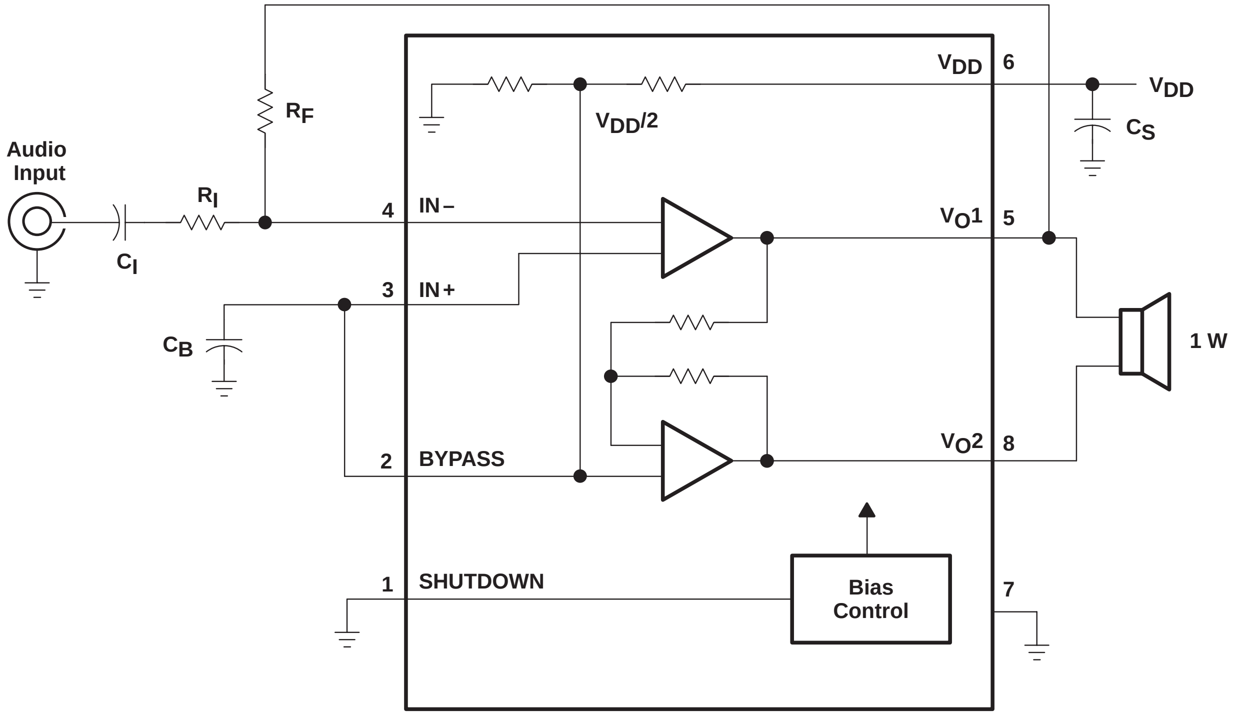
- **1-W BTL Output (5 V, 0.2 % THD+N)**
- **3.3-V and 5-V Operation**
- **No Output Coupling Capacitors Required**
- **Shutdown Control (I_{DD} = 0.6 μA)**
- **Uncompensated Gains of 2 to 20 (BTL Mode)**
- **Surface Mount Packaging**
- **Thermal and Short-Circuit Protection**
- **High Power Supply Rejection (56 dB at 1 kHz)**
- **LM4861 Drop-In Compatible**

D PACKAGE
(TOP VIEW)



description

The TPA4861 is a bridge-tied load (BTL) audio power amplifier capable of delivering 1 W of continuous average power into an 8-Ω load at 0.4 % THD+N from a 5-V power supply in voiceband frequencies (f < 5 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output in most applications. Gain is externally configured by means of two resistors and does not require compensation for settings of 2 to 20. Features of the amplifier are a shutdown function for power-sensitive applications as well as internal thermal and short-circuit protection. The TPA4861 works seamlessly with TI's TPA4860 in stereo applications. The amplifier is available in an 8-pin SOIC surface-mount package that reduces board space and facilitates automated assembly.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

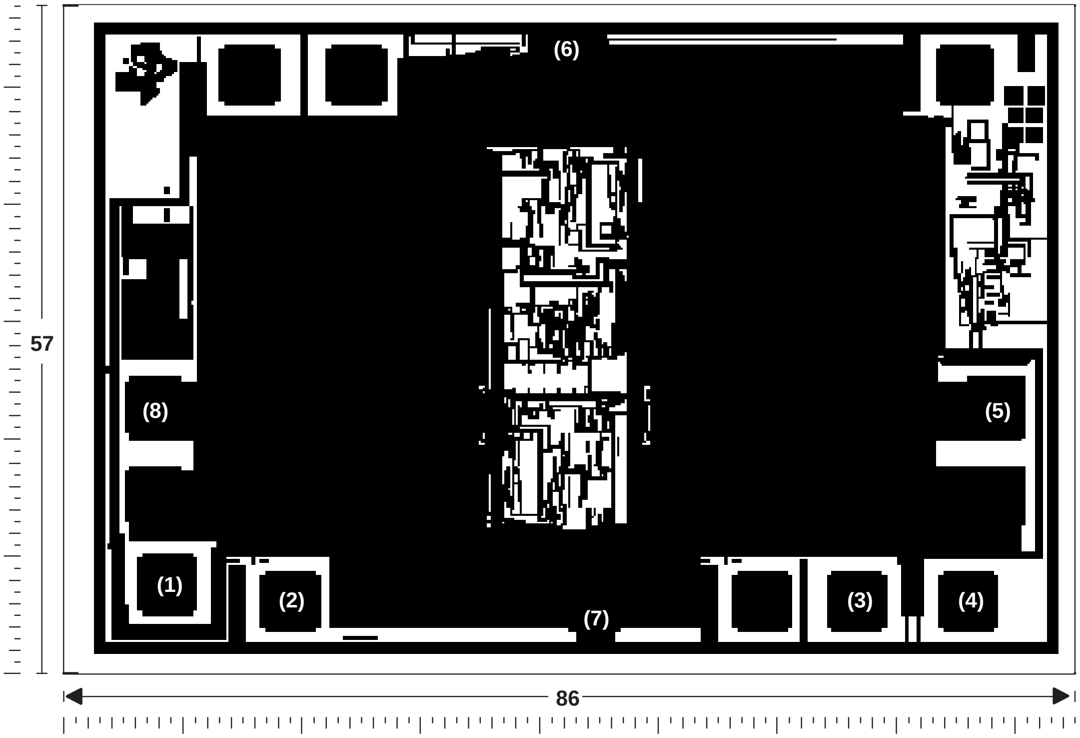
AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	CHIP FORM
	SMALL OUTLINE (D)	
–20°C to 85°C	TPA4861D	TPA4861Y

TPA4861Y chip information

This chip, when properly assembled, displays characteristics similar to the TPA4861C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINAL (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} . . . . 6 V
Input voltage, V_I . . . . –0.3 V to V_{DD} +0.3 V
Continuous total power dissipation . . . . internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A . . . . –20°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
D	731 mW	5.8 mW/°C	470 mW	383 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2.7	5.5	V
Common-mode input voltage, V_{IC}	V_{CC} = 3 V	1.25	2.7	V
	V_{CC} = 5 V	1.25	4.5	V
Operating free-air temperature, T_A		–20	85	°C

electrical characteristics at specified free-air temperature, V_{CC} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPA4861			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1		5	20	mV
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{OO}$)	V_{DD} = 3.2 V to 3.4 V		75		dB
$I_{DD(q)}$	Quiescent current			2.5		mA
$I_{DD(sd)}$	Quiescent current, shutdown mode			0.6		µA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4861			UNIT
				MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, A_V = 2		350		mW
			THD = 2%, f = 1 kHz, A_V = 2		500		mW
B_{OM}	Maximum output power bandwidth		Gain = 10, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection	BTL	f = 1 kHz		56		dB
		SE	f = 1 kHz		30		dB
V_n	Noise output voltage, see Note 3		Gain = 2		20		µV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

electrical characteristics at specified free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	TPA4861			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1		5	20	mV
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{OO}$)	V_{DD} = 4.9 V to 5.1 V		70		dB
$I_{DD(q)}$	Quiescent current			3.5		mA
$I_{DD(sd)}$	Quiescent current, shutdown mode			0.6		µA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristic, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4861			UNIT
				MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, A_V = 2		1000		mW
			THD = 2%, f = 1 kHz, A_V = 2		1100		mW
B_{OM}	Maximum output power bandwidth		Gain = 10, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection	BTL	f = 1 kHz		56		dB
		SE	f = 1 kHz		30		dB
V_n	Noise output voltage, see Note 3		Gain = 2		20		µV

NOTES: 2. Output power is measured at the output terminals of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

electrical characteristics at specified free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPA4861Y			UNIT
			MIN	TYP	MAX	
V_{OO}	Output offset voltage	See Note 1		5		mV
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{OO}$)	V_{DD} = 4.9 V to 5.1 V		70		dB
$I_{DD(q)}$	Quiescent current			3.5		mA
$I_{DD(sd)}$	Quiescent current, shutdown mode			0.6		µA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

operating characteristic, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER			TEST CONDITIONS	TPA4861Y			UNIT
				MIN	TYP	MAX	
P_O	Output power, see Note 2		THD = 0.2%, f = 1 kHz, A_V = 2		1000		mW
			THD = 2%, f = 1 kHz, A_V = 2		1100		mW
B_{OM}	Maximum output power bandwidth		Gain = 10, THD = 2%		20		kHz
B_1	Unity-gain bandwidth		Open Loop		1.5		MHz
	Supply ripple rejection	BTL	f = 1 kHz		56		dB
		SE	f = 1 kHz		30		dB
V_n	Noise output voltage, see Note 4		Gain = 2		20		µV

NOTES: 2. Output power is measured at the output pins of the device.
3. Noise voltage is measured in a bandwidth of 20 Hz to 20 kHz.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{OO}	Output offset voltage	Distribution	1,2
I_{DD}	Supply current distribution	vs Free-air temperature	3,4
THD+N	Total harmonic distortion plus noise	vs Frequency	5,6,7,8,9, 10,11,15, 16,17,18
		vs Output power	12,13,14, 19,20,21
I_{DD}	Supply current	vs Supply voltage	22
V_n	Output noise voltage	vs Frequency	23,24
	Package power dissipation	vs Free-air temperature	25
	Power dissipation	vs Output power	26,27
	Maximum power output	vs Free-air temperature	28
	Output power	vs Load Resistance	29
		vs Supply Voltage	30
	Open loop frequency response	vs Frequency	31
	Power supply rejection ratio	vs Frequency	32,33

TYPICAL CHARACTERISTICS

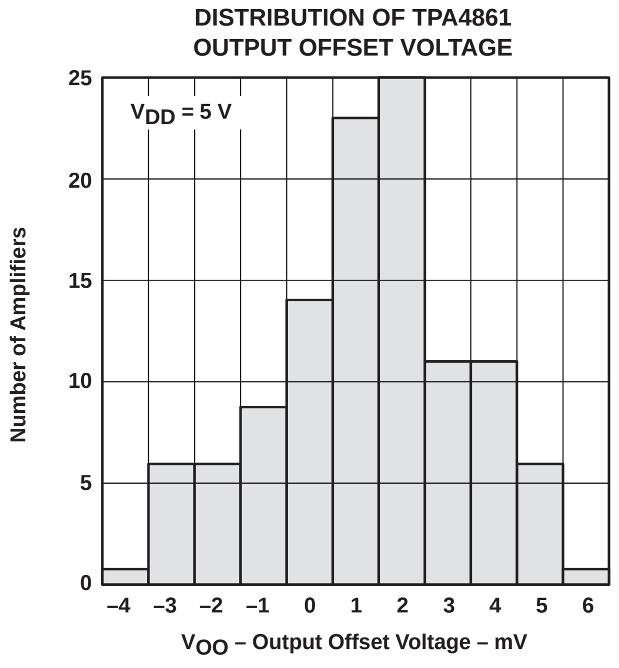


Figure 1

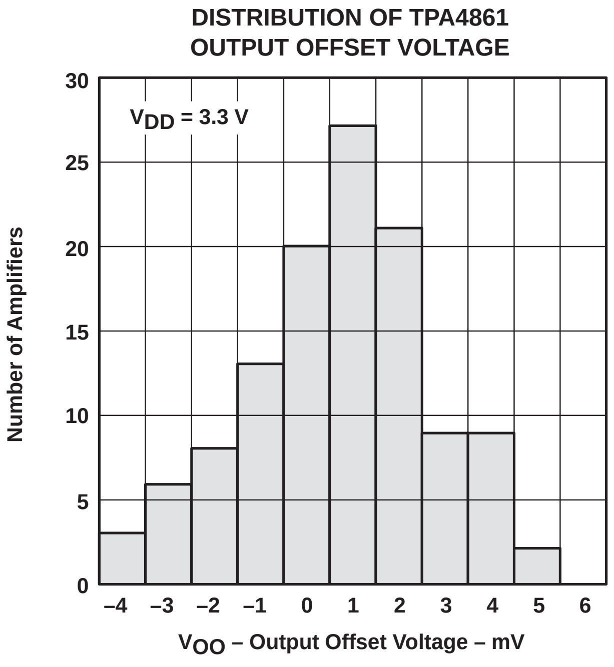


Figure 2

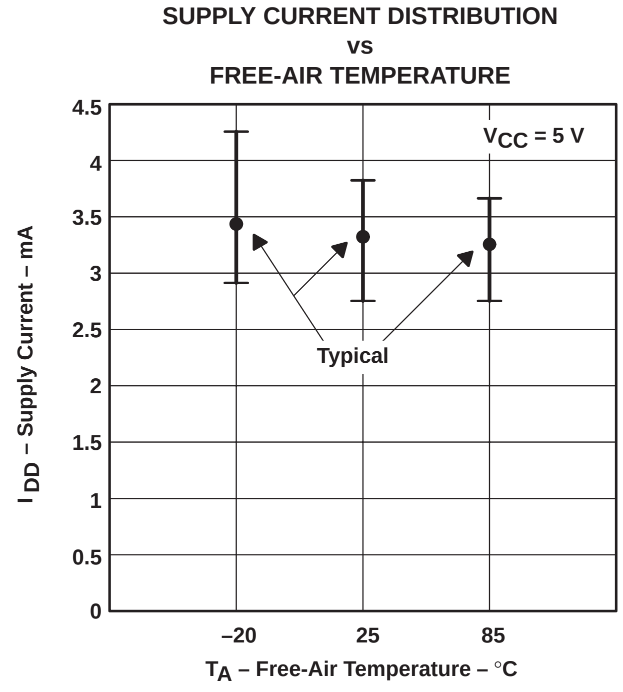


Figure 3

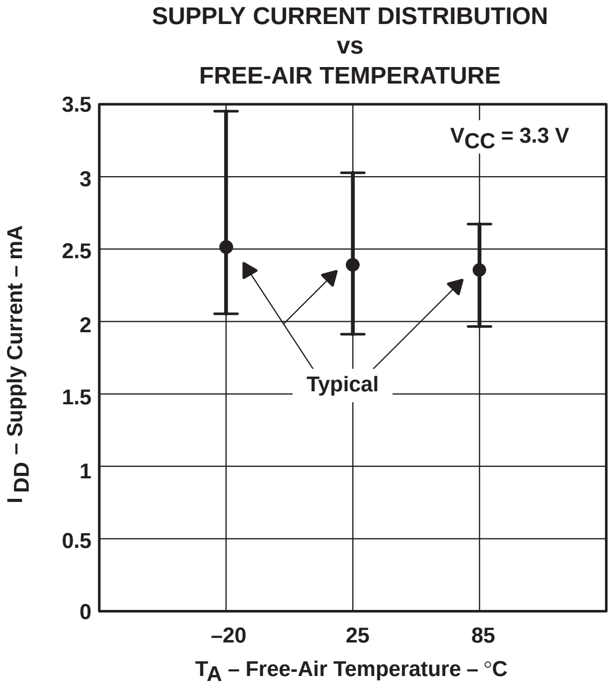


Figure 4

TYPICAL CHARACTERISTICS

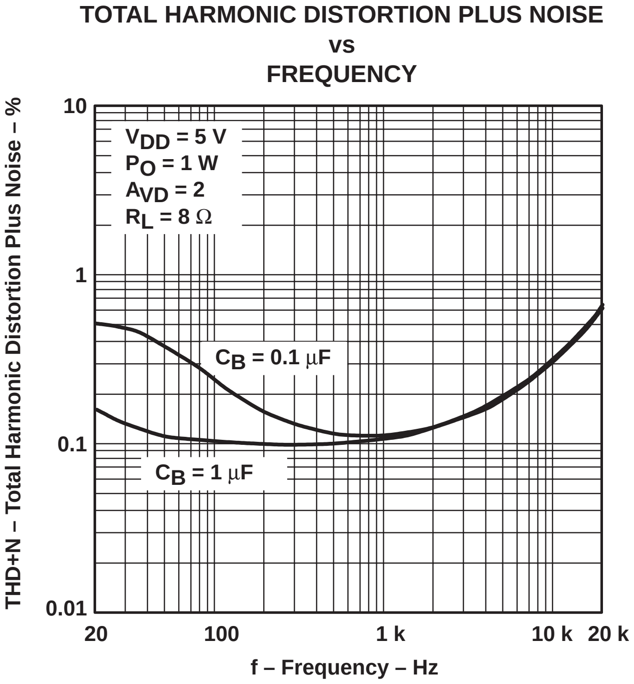


Figure 5

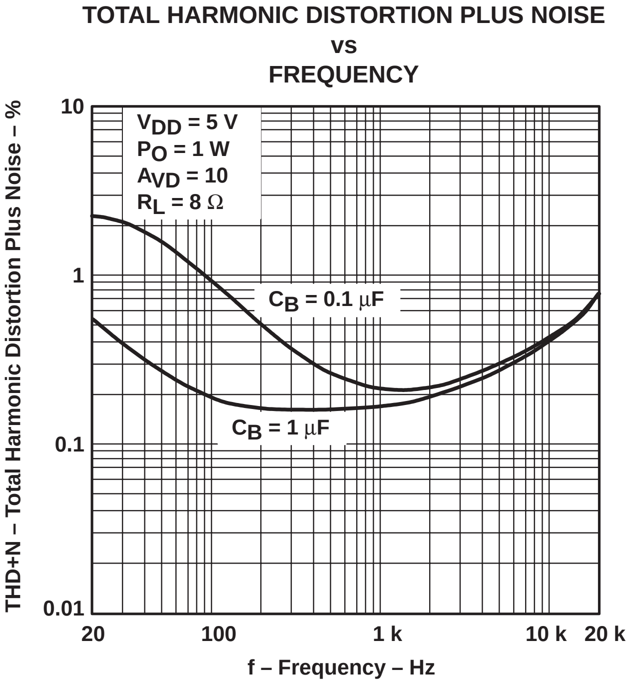


Figure 6

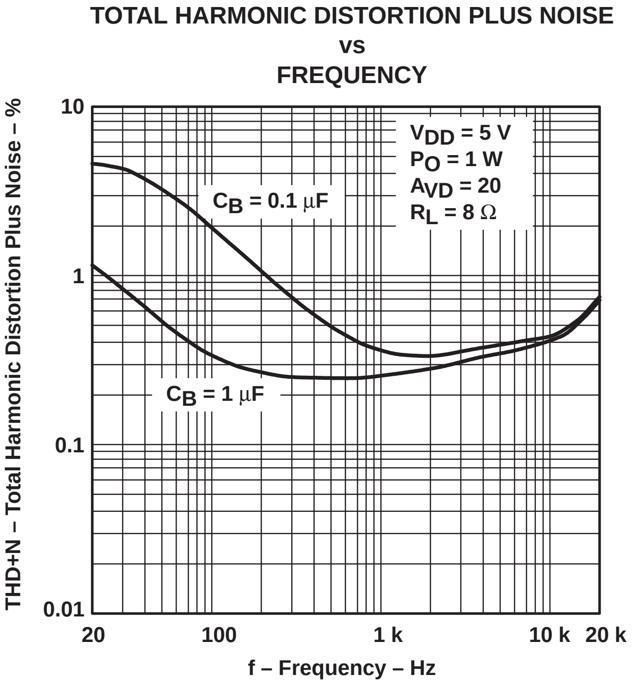


Figure 7

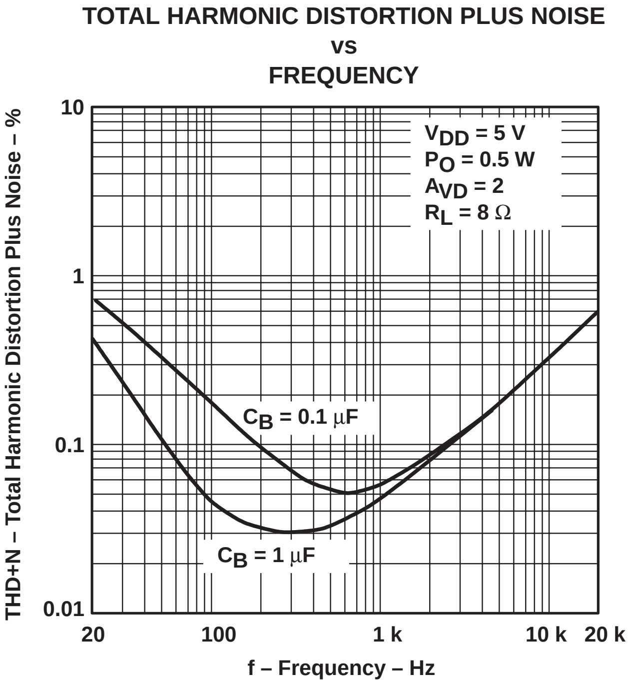


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

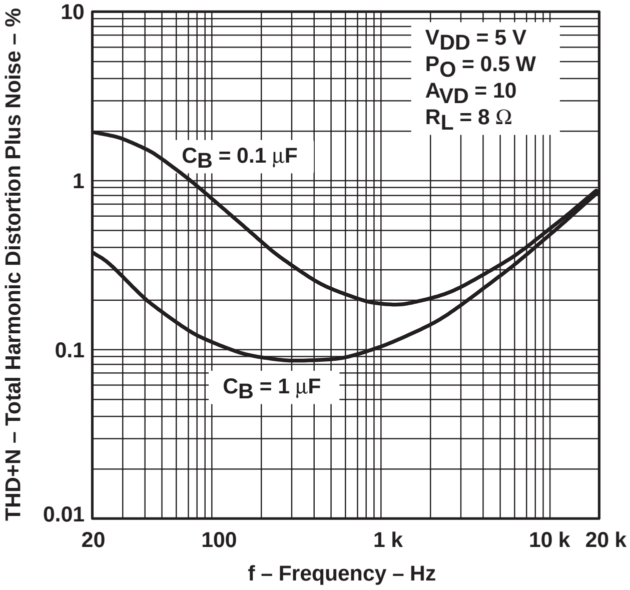


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

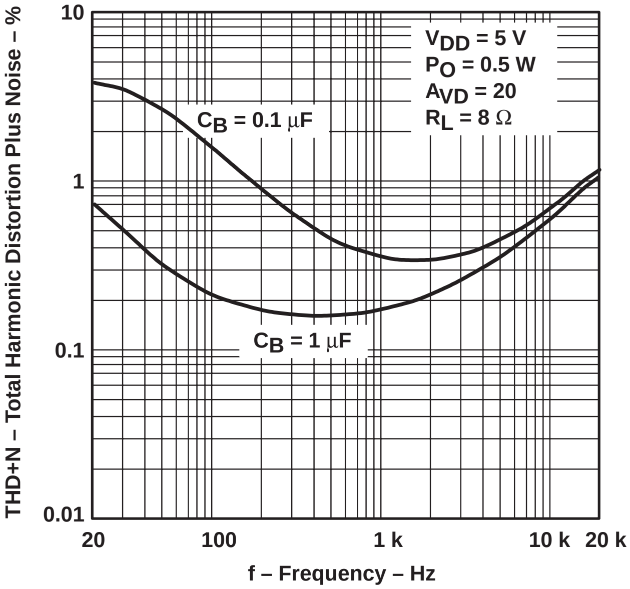


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

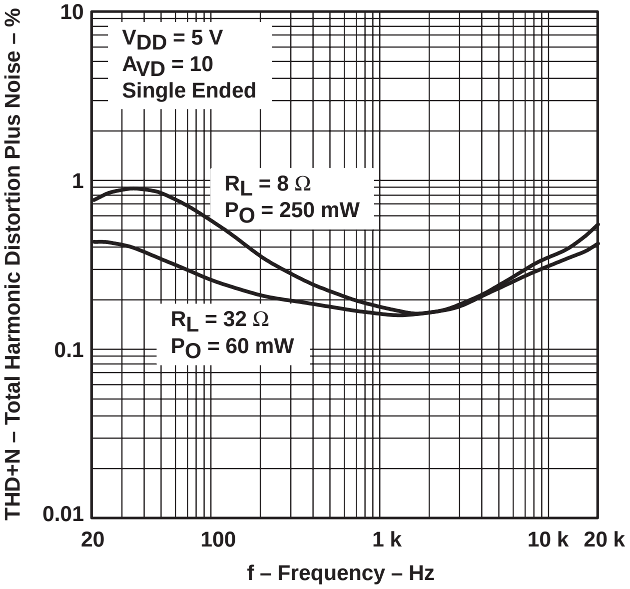


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

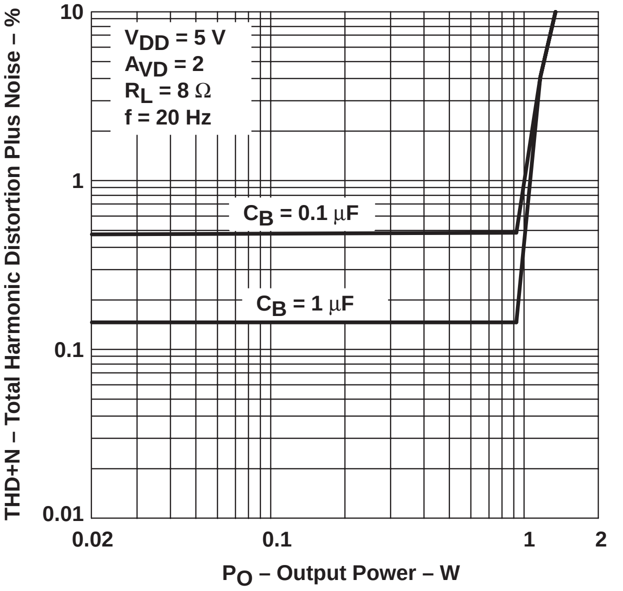


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

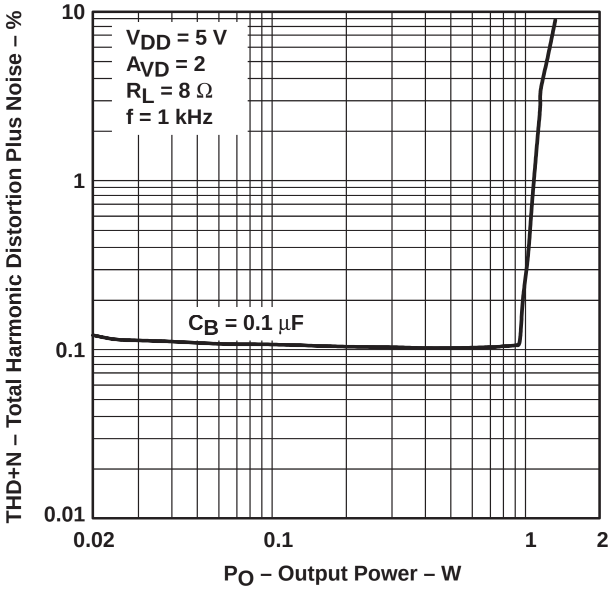


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

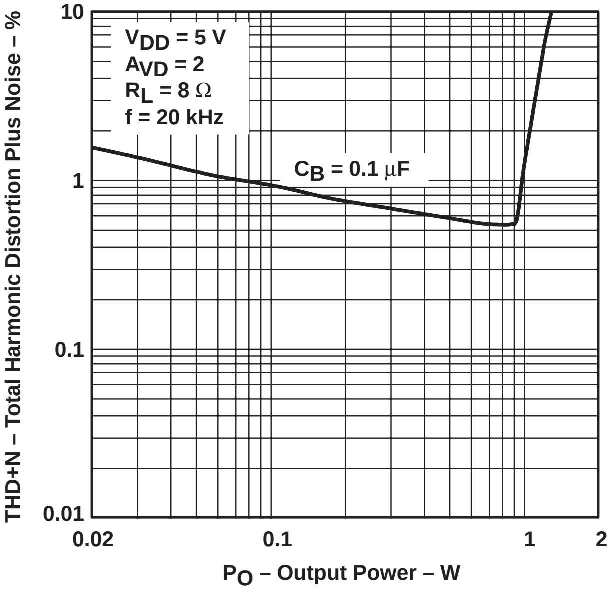


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

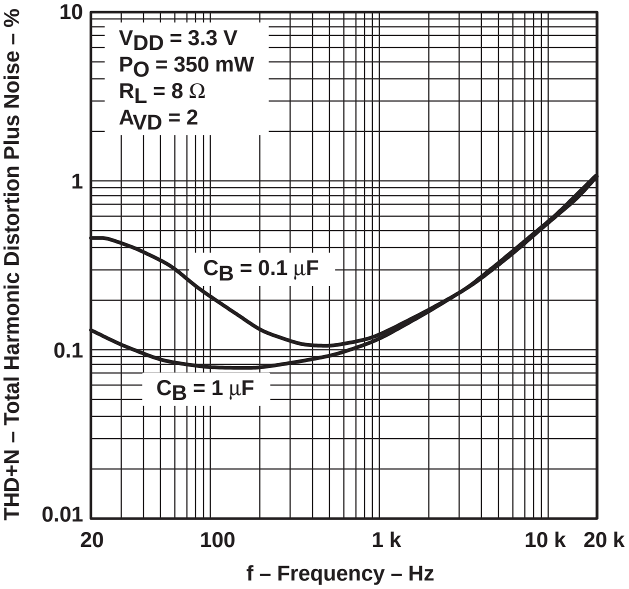


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

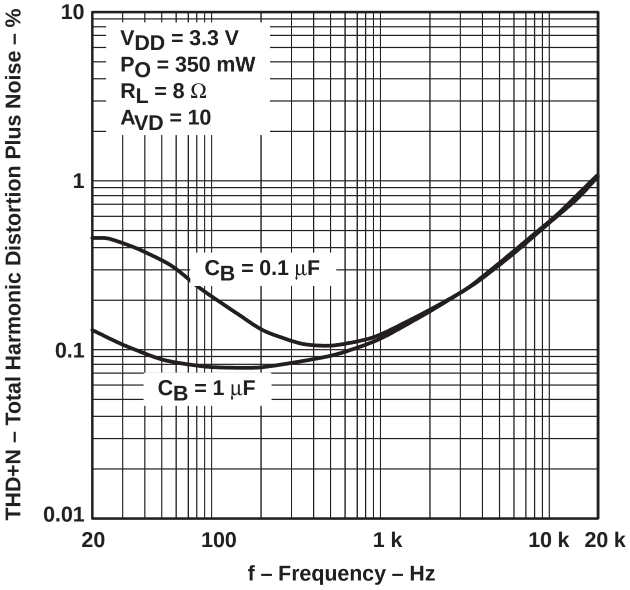


Figure 16

TYPICAL CHARACTERISTICS

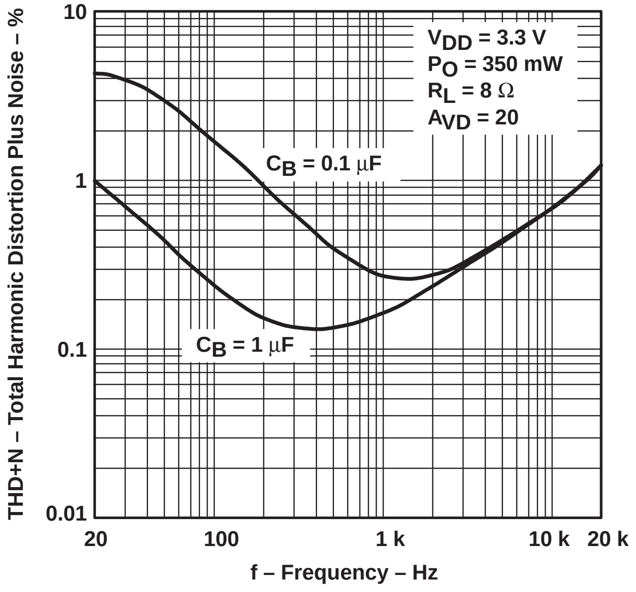

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 17

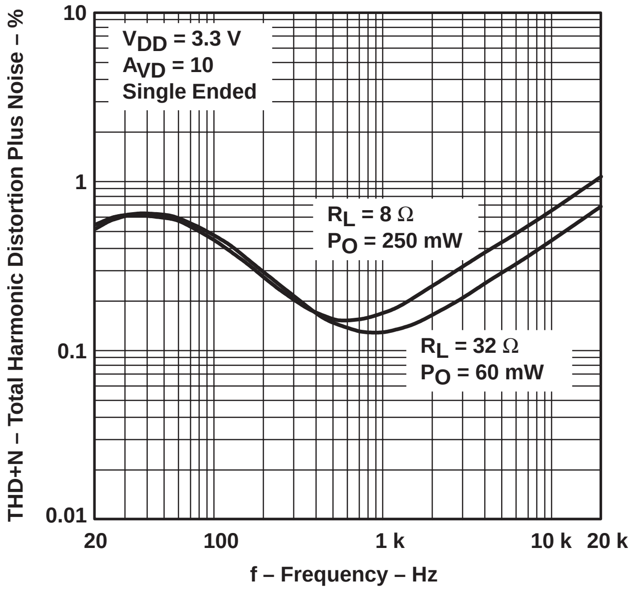

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 18

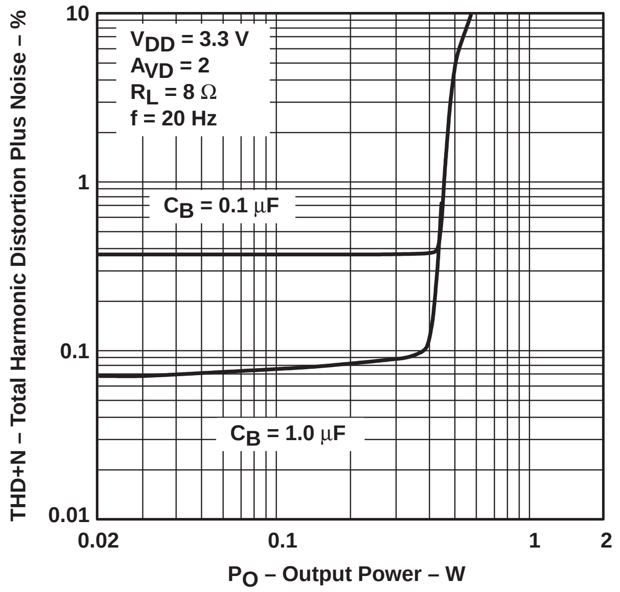

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 19

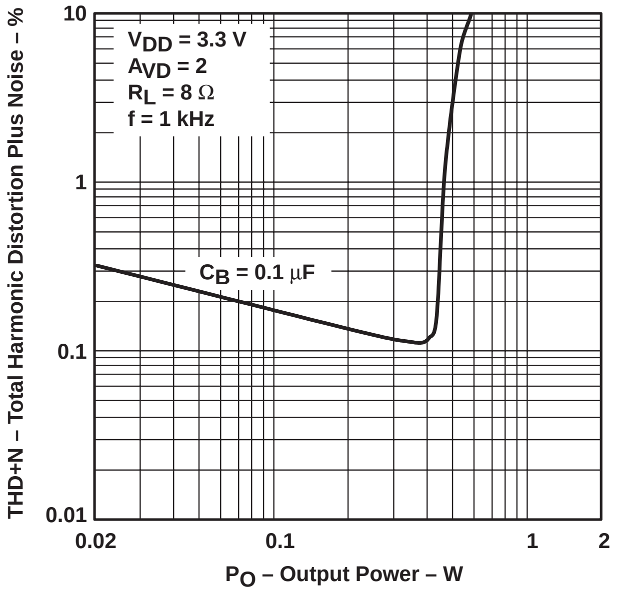

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 20

TYPICAL CHARACTERISTICS

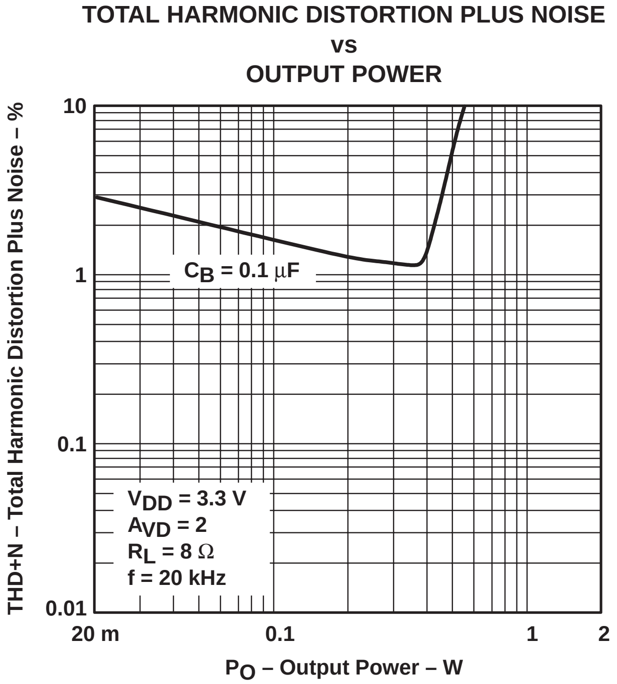

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 21

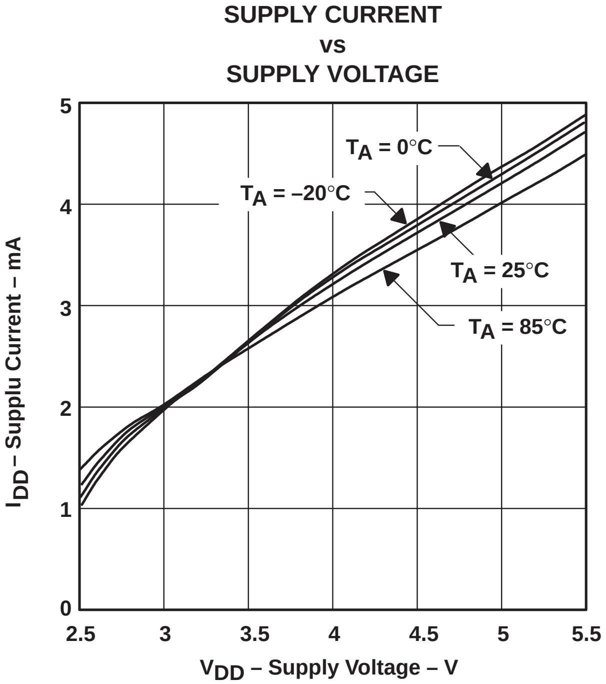

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 22

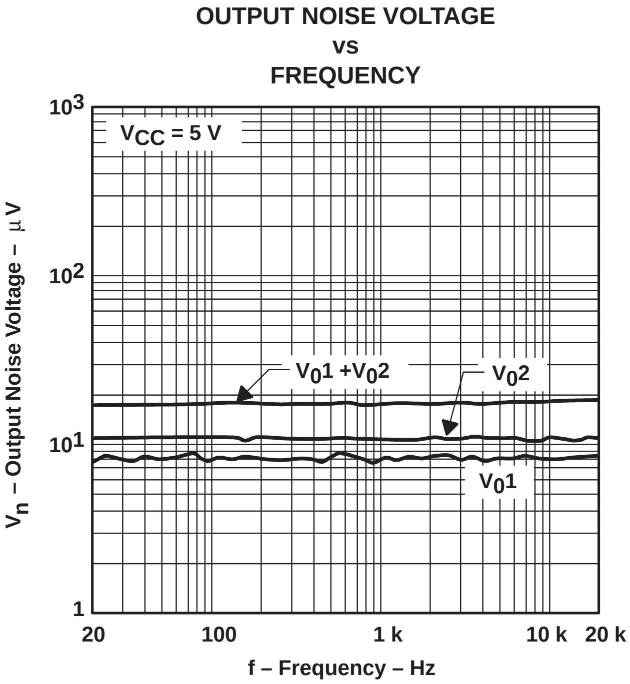

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 23

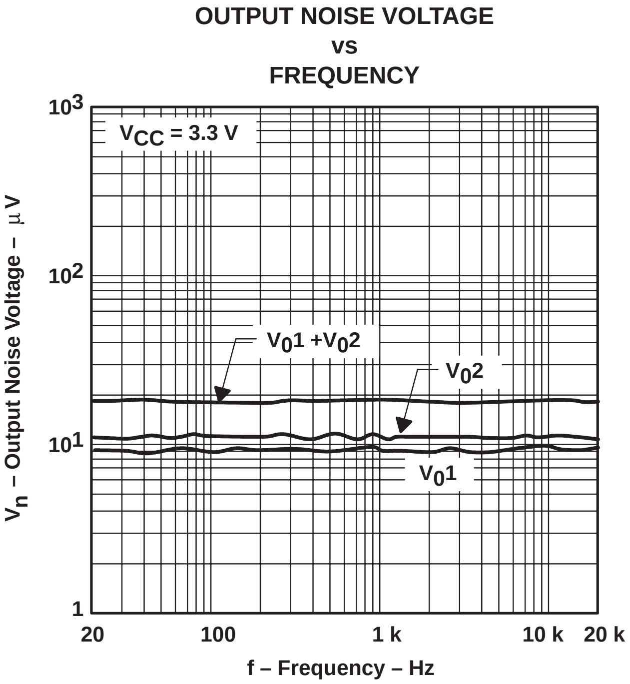

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 24

TYPICAL CHARACTERISTICS

MAXIMUM PACKAGE POWER DISSIPATION vs FREE-AIR TEMPERATURE

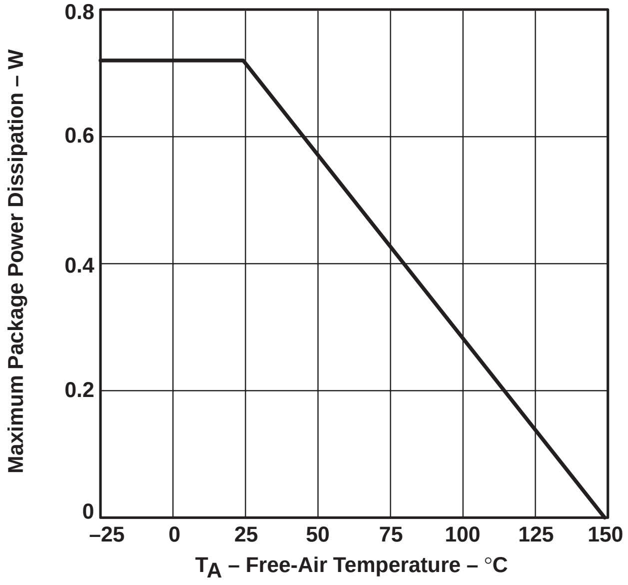


Figure 25

POWER DISSIPATION vs OUTPUT POWER

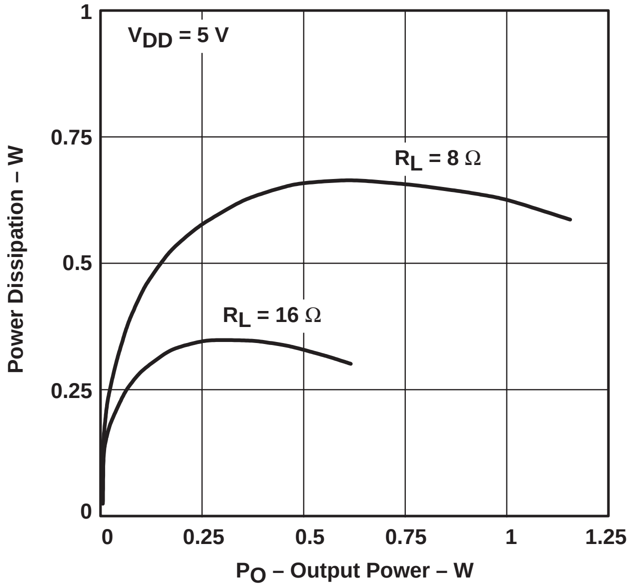


Figure 26

POWER DISSIPATION vs OUTPUT POWER

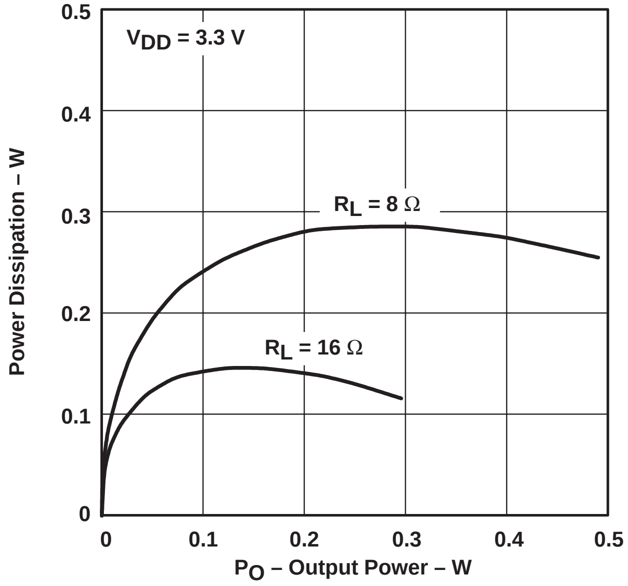


Figure 27

MAXIMUM OUTPUT POWER vs FREE-AIR TEMPERATURE

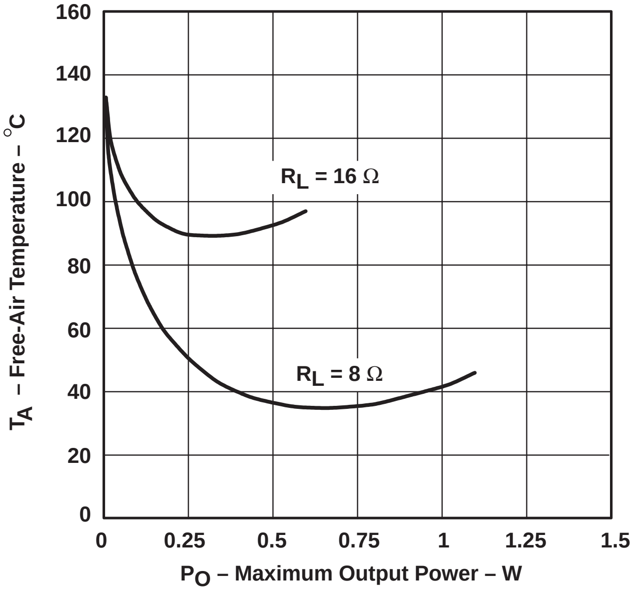


Figure 28

TYPICAL CHARACTERISTICS

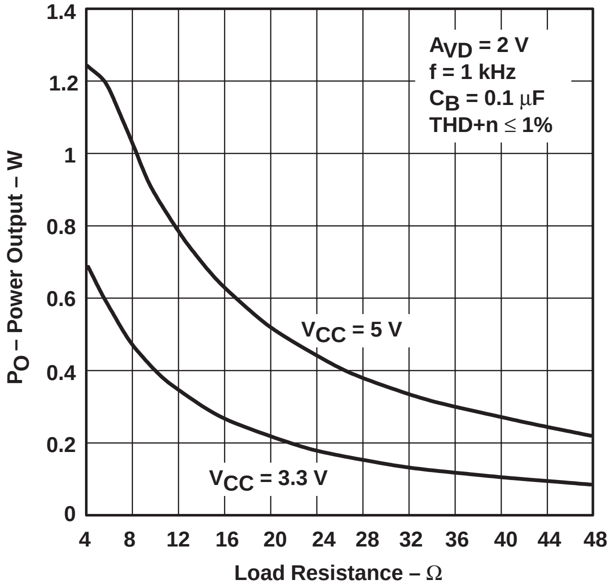

OUTPUT POWER
vs
LOAD RESISTANCE

Figure 29

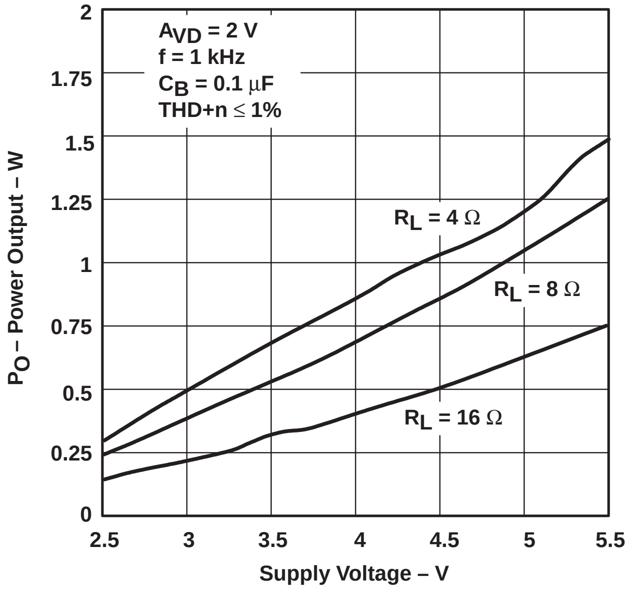

OUTPUT POWER
vs
SUPPLY VOLTAGE

Figure 30

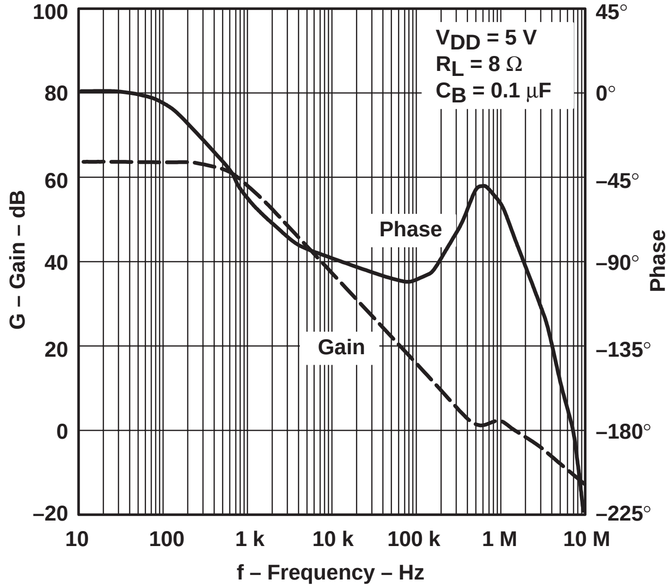

OPEN LOOP FREQUENCY RESPONSE

Figure 31

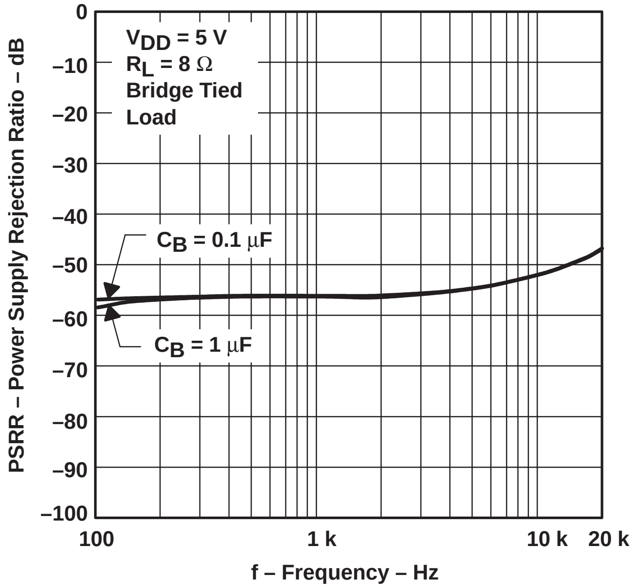

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

Figure 32

TYPICAL CHARACTERISTICS

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

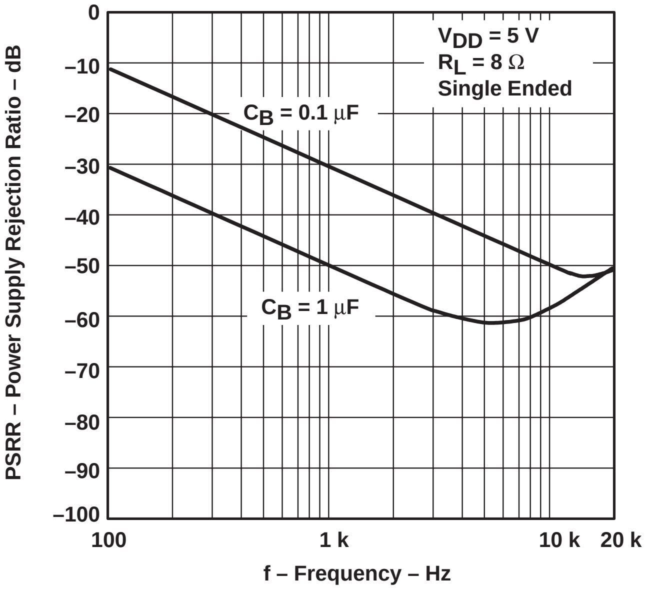


Figure 33

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 34 shows a linear audio power amplifier (APA) in a bridge tied load (BTL) configuration. A BTL amplifier actually consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially let us consider power to the load. The differential drive to the speaker means that as one side is slewing up the other side is slewing down and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging twice the voltage into the power equation, where voltage is squared, yields 4 times the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{{V_{(rms)}}^2}{R_L} \qquad (1)$$

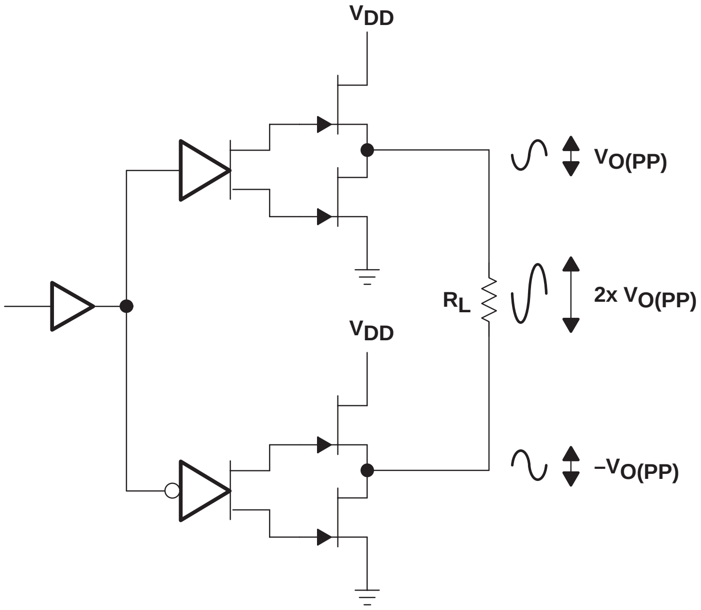


Figure 34. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into a 8-Ω speaker from a singled-ended (SE) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns, consider the single-supply SE configuration shown in Figure 35. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 40 µF to 1000 µF) so they tend to be expensive, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

$$f_{(corner)} = \frac{1}{2\pi R_L C_C} \qquad (2)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

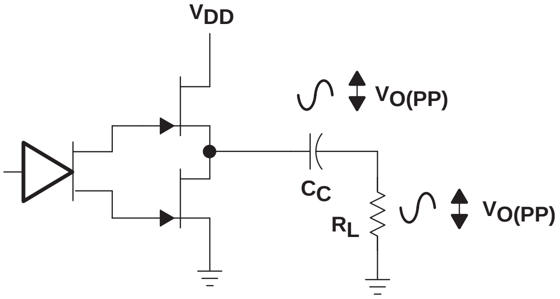


Figure 35. Single-Ended Configuration

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4 times the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy to use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveforms shapes must first be understood (see Figure 36).

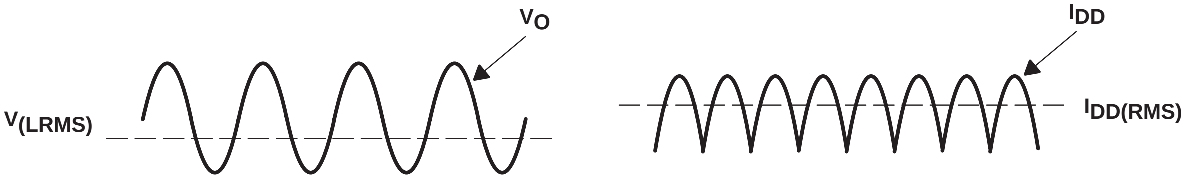


Figure 36. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistor are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \qquad (3)$$

where:

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p^{\ 2}}{2R_L}$$

$$P_{SUP} = V_{DD}\ I_{DD}\text{rms} = \frac{V_{DD}\ 2V_P}{\pi\ R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\ R_L}$$

$$\begin{array}{c}\text{Effiency of a}\\ \text{BTL Configuration}\end{array} = \frac{\pi\ V_P}{2V_{DD}} = \frac{\pi\left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \qquad (4)$$

Table 1 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 1. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak-to-Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

APPLICATION INFORMATION

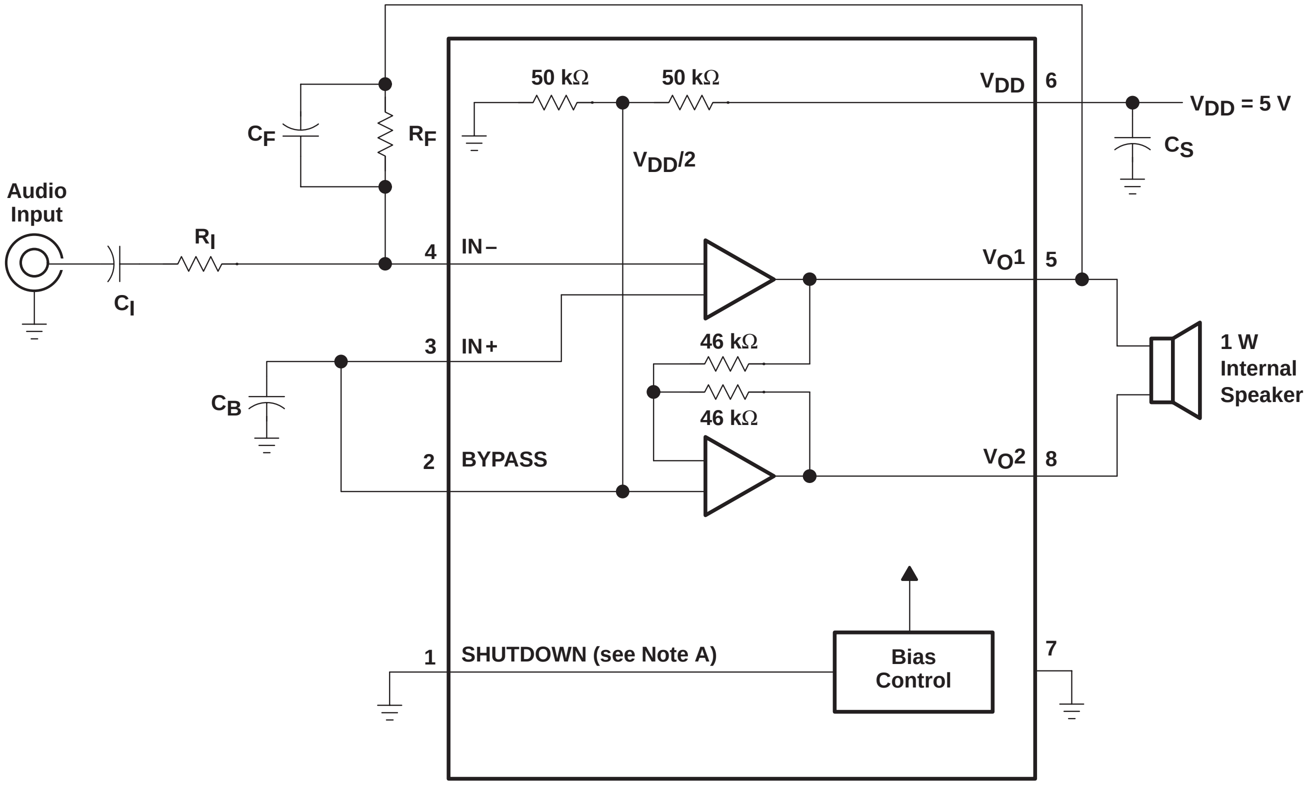
BTL amplifier efficiency (continued)

A final point to remember about linear amplifiers whether they are SE or BTL configured is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

For example, if the 5-V supply is replaced with a 10-V supply (TPA4861 has a maximum recommended V_{DD} of 5.5 V) in the calculations of Table 1 then efficiency at 1 W would fall to 31% and internal power dissipation would rise to 2.18 W from 0.59 W at 5 V. Then for a stereo 1-W system from a 10-V supply, the maximum draw would be almost 6.5 W. Choose the correct supply voltage and speaker impedance for the application.

selection of components

Figure 37 is a schematic diagram of a typical notebook computer application circuit.



NOTE A: SHUTDOWN must be held low for normal operation and asserted high for shutdown mode.

Figure 37. TPA4861 Typical Notebook Computer Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for the TPA4861 is set by resistors R_F and R_I according to equation 5.

$$\text{Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA4861 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\begin{matrix}\text{Effective}\\ \text{Impedance}\end{matrix} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The gain of the amplifier would be –10 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \tag{7}$$

For example if R_F is 100 kΩ and Cf is 5 pF then f_{co} is 318 kHz, which is well outside of the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \tag{8}$$

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_{co}} \tag{9}$$

In this example, C_I is 0.40 µF so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA4861 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so slow it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained.

$$\frac{1}{\left(C_B \times 25k\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \qquad (10)$$

As an example, consider a circuit where C_B is 0.1 µF, C_I is 0.22 µF and R_I is 10 kΩ. Inserting these values into the equation 9 we get:

$$400 \le 454$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

APPLICATION INFORMATION

single-ended operation

Figure 38 is a schematic diagram of the recommended SE configuration. In SE mode configurations, the load should be driven from the primary amplifier output (OUT1, terminal 10).

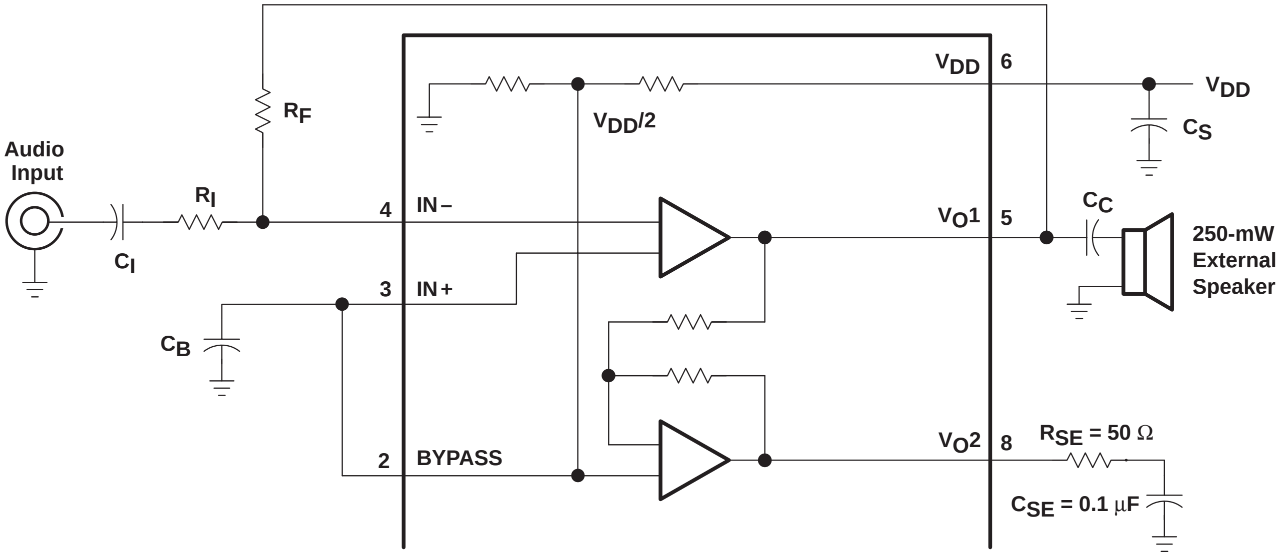


Figure 38. Singled-Ended Mode

Gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2 is not included.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \tag{11}$$

The phase margin of the inverting amplifier into an open circuit is not adequate to ensure stability, so a termination load should be connected to V_O2. This consists of a 50-Ω resistor in series with a 0.1-µF capacitor to ground. It is important to avoid oscillation of the inverting output to minimize noise and power dissipation.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

$$\frac{1}{\left(C_B \times 25k\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \tag{12}$$

APPLICATION INFORMATION

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 13.

$$f_{out\ high} = \frac{1}{2\pi R_L C_C} \tag{13}$$

The main disadvantage, from a performance standpoint, is that the load impedances are typically small, which drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 μF is chosen and loads vary from 8 Ω, 32 Ω, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
8 Ω	68 μF	293 Hz
32 Ω	68 μF	73 Hz
47,000 Ω	68 μF	0.05 Hz

As Table 2 indicates, most of the bass response is attenuated into 8-Ω loads while headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

shutdown mode

The TPA4861 employs a shutdown mode of operation designed to reduce quiescent supply current, $I_{DD(q)}$, to the absolute minimum level during periods of nonuse for battery-power conservation. For example, during device sleep modes or when other audio-drive currents are used (i.e., headphone mode), the speaker drive is not required. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD(q)} < 1$ μA. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

thermal considerations

A prime consideration when designing an audio amplifier circuit is internal power dissipation in the device. The curve in Figure 39 provides an easy way to determine what output power can be expected out of the TPA4861 for a given system ambient temperature in designs using 5-V supplies. This curve assumes no forced airflow or additional heat sinking.

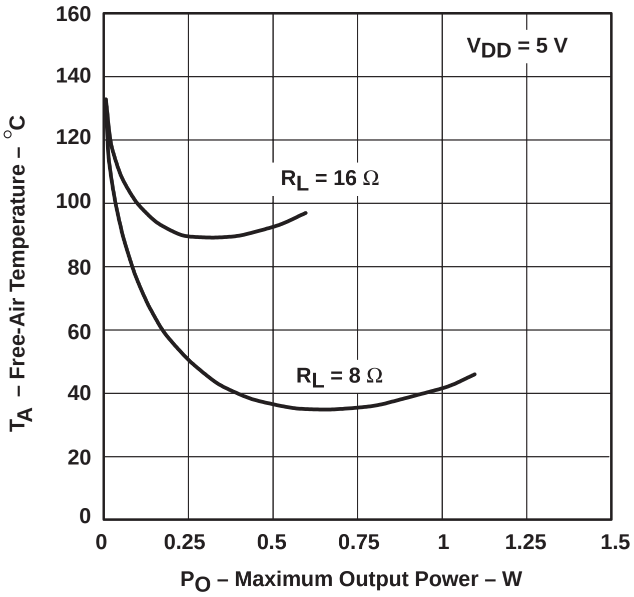


Figure 39. Free-Air Temperature Versus Maximum Continuous Output Power

5-V versus 3.3-V operation

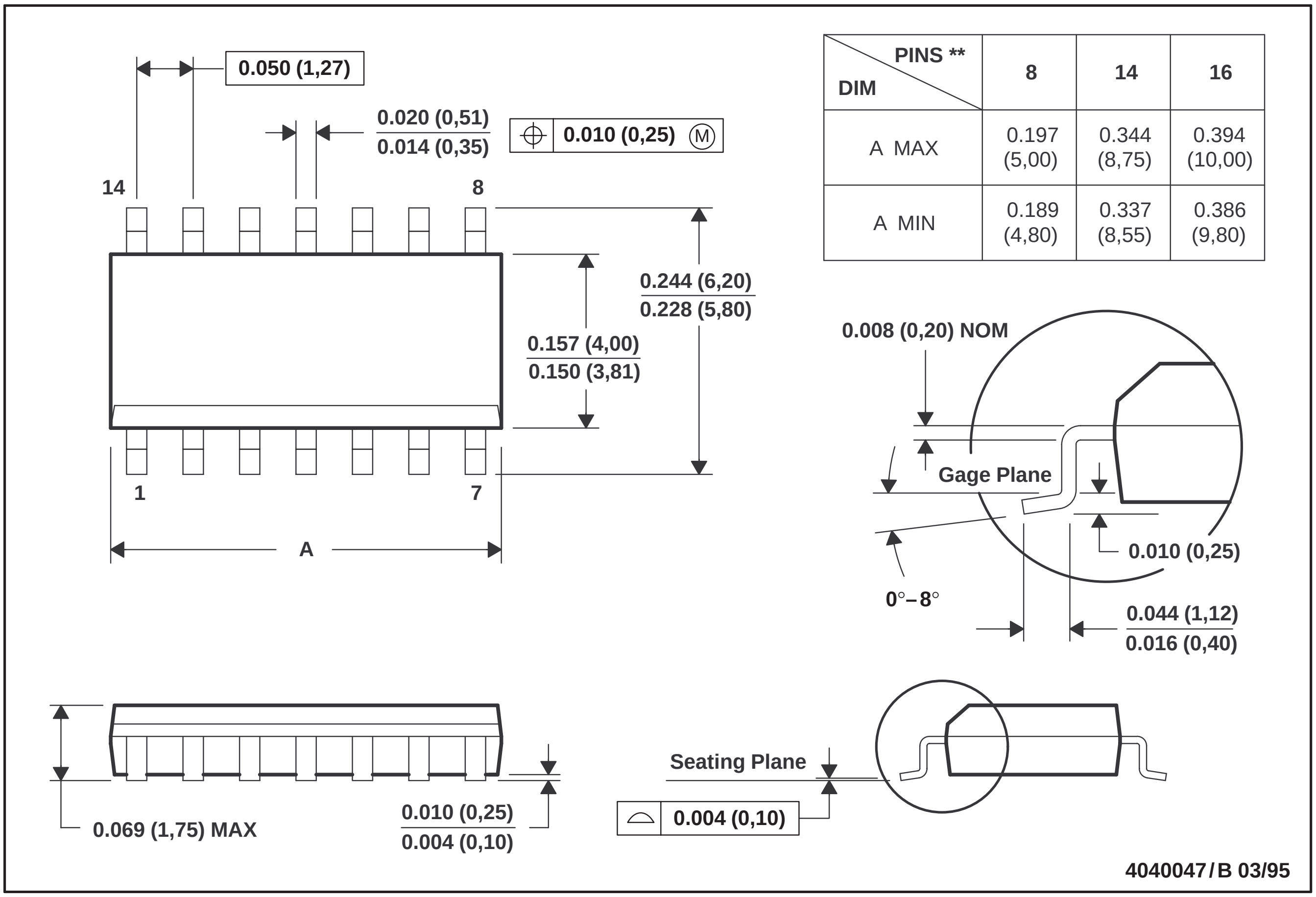
The TPA4861 was designed for operation over a supply range of 2.7 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting or stability. Supply current is slightly reduced from 3.5 mA (typical) to 2.5 mA (typical). The most important consideration is that of output power. Each amplifier in TPA4861 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load to less than 0.33 W before distortion begins to become significant.

Operation at 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds of the supply power for a given output-power level than operation from 5-V supplies. When the application demands less than 500 mW, 3.3-V operation should be strongly considered, especially in battery-powered applications.

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Four center pins are connected to die mount pad.
- E. Falls within JEDEC MS-012

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