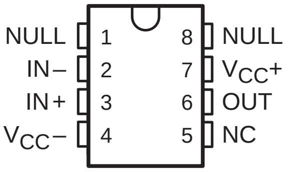
THS4001
HIGH-SPEED LOW-POWER OPERATIONAL AMPLIFIER

SLOS206– DECEMBER 1997

- **Very High Speed**
  - **300 MHz Bandwidth (Gain = 1, –3 dB)**
  - **400 V/µsec Slew Rate**
  - **30-ns Settling Time (0.1%)**
- **High Output Drive, I_O = 100 mA**
- **Wide Range of Power Supplies V_{CC} = ± 2.5 V to ± 15 V, I_{CC} = 7.5 mA**
- **Available in an 8-Pin SOIC**
- **Very Low Distortion**
  - **THD = –72 dBc at f = 1 MHz**

D PACKAGE
(TOP VIEW)



NC – No internal connection

description

The THS4001 is a very high-performance, voltage-feedback operational amplifier especially suited for a wide range of video applications. The device is specified to operate over a wide range of supply voltages from ± 15 V to ± 2.5 V. With a bandwidth of 300 MHz, a slew rate of over 400 V/µs, and settling times of less than 30 ns, the THS4001 offers the unique combination of high performance in an easy to use voltage feedback configuration over a wide range of power supply voltages.

The THS4001 is stable at all gains for both inverting and non-inverting configurations. It has a high output drive capability of 100 mA and draws only 7.5 mA of quiescent current. Excellent professional video results can be obtained with the differential gain/phase performance of 0.04°/0.15° and 0.1 dB gain flatness to 60 MHz. For applications requiring low distortion, the THS4001 is ideally suited with total harmonic distortion of –72 dBc at f = 1 MHz.

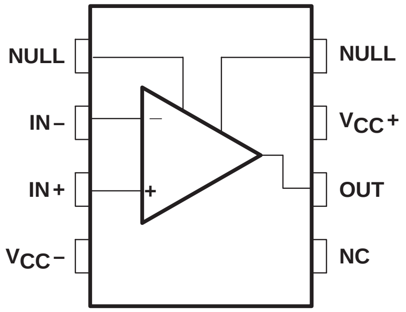
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	SMALL OUTLINE[†] (D)
0°C to 70°C	THS4001CD
–40°C to 85°C	THS4001ID

[†] The D packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4001CDR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

symbol



absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{CC}	16.5 V
Input voltage, V_I	±V_{CC}
Output current, I_O	175 mA
Differential input voltage, V_{ID}	±4 V
Continuous total power dissipation	See Dissipation Ratings Table
Operating free air temperature, T_A: C suffix	0°C to 70 °C
I suffix	–40°C to 85 °C
Storage temperature, T_{stg}	–65°C to 150 °C
Lead temperature, 1.6Mm (1/16 Inch) from case for 10 seconds	300°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	740 mW	6 mW/°C	475 mW	385 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}	Dual supply	±2.5		±16	V
	Single supply	±5		±32	
Quiescent current, I_{CC}	±15 V		7.8	9.5	mA
	±5 V, ±2.5 V		6.7	8	
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	–40		85	

electrical characteristics, V_{CC} = ±15 V, R_L = 150 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
	Differential gain error	Gain = 2, R_L = 150 Ω, f = 3.58 MHz		±15 V		0.04%		
				±5 V		0.01%		
	Differential phase error			±15 V		0.15°		
				±5 V		0.08°		
V_{IO}	Input offset voltage	T_A = 25°C		±15 V, ±5 V		2	8	mV
		T_A = full range					10	
I_{IB}	Input bias current	T_A = 25°C		±15 V, ±5 V		2.6	5	µA
		T_A = full range					6	
I_{OS}	Input offset current	T_A = 25°C		±15 V, ±5 V		35	200	nA
		T_A = full range					500	
	Open-loop gain	V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	±15 V	5	10		V/mV
			T_A = full range		3			
		V_O = ±2.5 V, R_L = 500 Ω	T_A = 25°C	±5 V	3	6		
			T_A = full range		2			
CMRR	Common-mode rejection ratio	$V_{(CM)}$ = ±12 V	T_A = 25°C	±15 V	85	100		dB
			T_A = full range		75			
PSRR	Power supply rejection ratio	T_A = 25°C		±15 V, ±5 V	75	85		dB
		T_A = full range			70			
V_{ICR}	Common-mode input voltage range			±15 V	13.5 to –13	14.8 to –14		V
				±5 V	3.6 to –2.7	4.4 to –3.6		
V_O	Output voltage swing	R_L = 500 Ω		±15 V	±13	±13.5		V
				±5 V	±3.3	±3.8		
				±2.5 V	±0.8	±1.3		
I_O	Output current			±15 V	50	100		mA
				±5 V	50	100		
				±2.5 V	50	100		
THD	Total harmonic distortion	V_I = 1 $V_{(PP)}$, f = 1 MHz		±15 V		–72		dBc
R_I	Input resistance					10		MΩ
C_I	Input capacitance					1.5		pF
R_O	Output resistance	Open loop				10		Ω

operating characteristics, V_{CC} = ±15 V, R_L = 150 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
	Slew rate	Gain = –1	±15 V		400		V/µs
			±5 V		400		
			±2.5 V		350		
	Settling time to 0.1%	10 V step (0 to 10 V), Gain = –1	±15 V		40		ns
		–2.5 V to 2.5 V step, Gain = –1	±5 V		30		
	–3 dB Bandwidth	Gain = +1, R_L = 150 Ω, R_f = 150 Ω	±15 V		270		MHz
			±5 V		220		
			±2.5 V		180		
		Gain = –1, R_L = 150 Ω, R_f = 150 Ω	±15 V		80		MHz
			±5 V		75		
			±2.5 V		70		
	Bandwidth for 0.1 dB flatness	Gain = +1	±15 V		60		MHz
			±5 V		50		
			±2.5 V		40		
V_n	Equivalent input noise voltage	f = 10 kHz	±15 V, ±5 V		12.5		nV/$\sqrt{Hz}$
I_n	Equivalent input noise current	f = 10 kHz	±15 V, ±5 V		1.5		pA/$\sqrt{Hz}$

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	1
V_{IO}	Input offset voltage	vs Free-air temperature	2
	Open-loop gain	vs Frequency	3
	Phase	vs Frequency	3
	Differential gain	vs DC voltage	4, 5
	Differential phase	vs DC voltage	4, 5
	Closed-loop gain	vs Frequency	6, 7
CMRR	Common-mode rejection ratio	vs Frequency	8
PSRR	Power-supply rejection ratio	vs Frequency	9
		vs Free-air temperature	10
$V_{O(PP)}$	Output voltage swing	vs Supply voltage	11
		vs Load resistance	12
	Bandwidth (– 3 dB)	vs Feedback resistance	13, 14
I_{CC}	Supply current	vs Supply voltage	15
		vs Free-air temperature	16
E_{nv}	Noise spectral density	vs Frequency	17
THD	Total harmonic distortion	vs Frequency	18

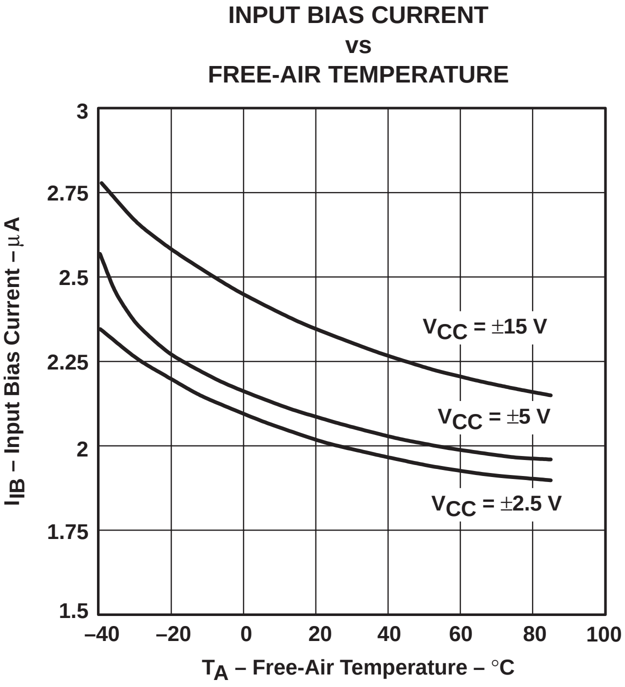


Figure 1

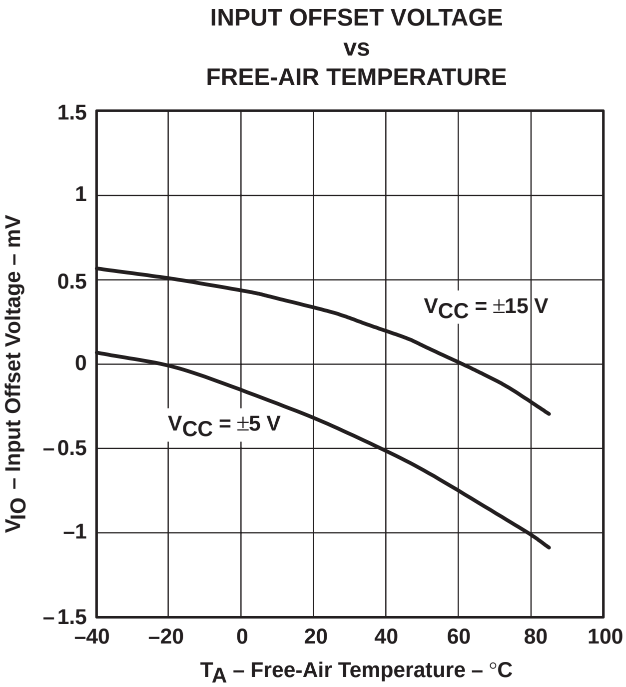


Figure 2

TYPICAL CHARACTERISTICS

OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY

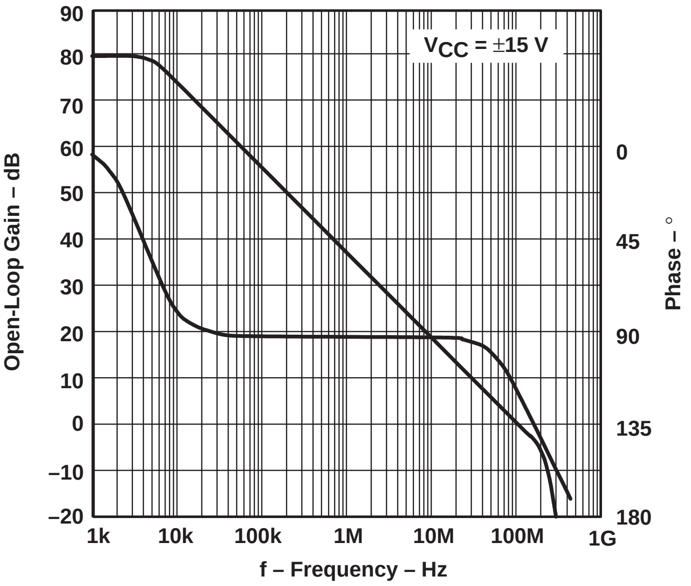


Figure 3

DIFFERENTIAL GAIN AND
DIFFERENTIAL PHASE
vs
DC VOLTAGE

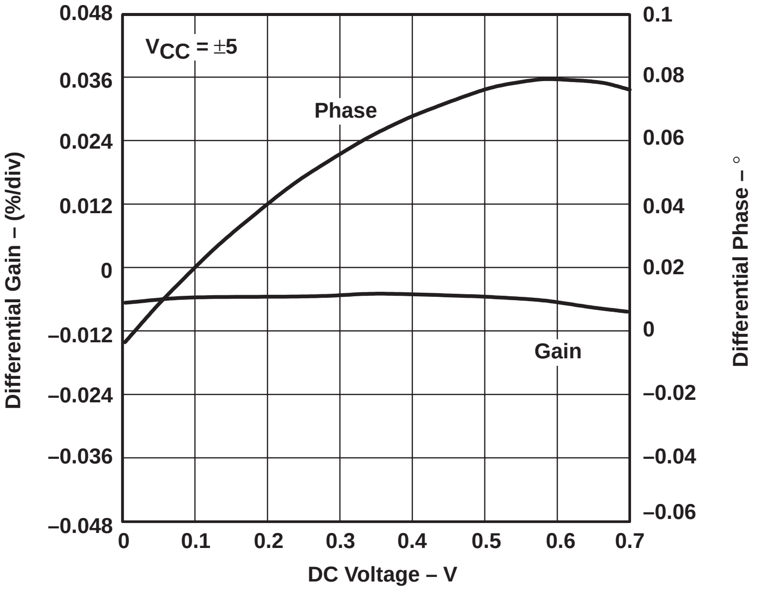


Figure 4

TYPICAL CHARACTERISTICS

DIFFERENTIAL GAIN AND DIFFERENTIAL PHASE vs DC VOLTAGE

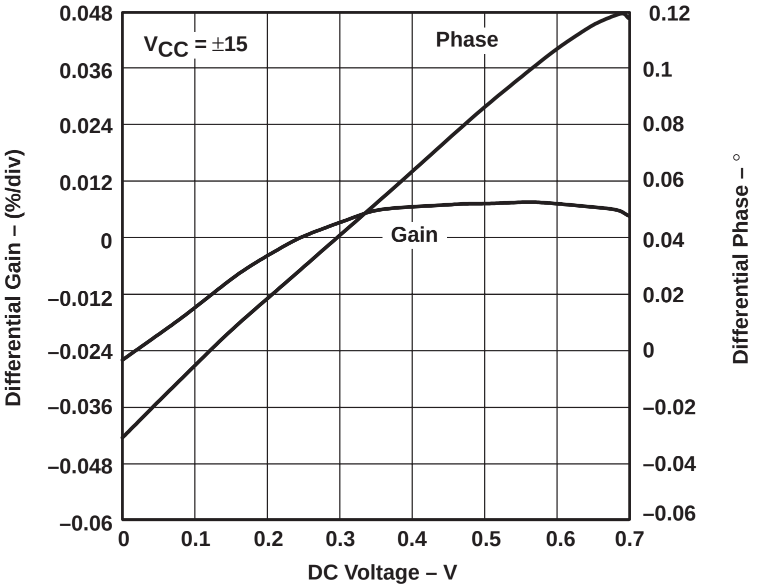


Figure 5

CLOSED-LOOP GAIN vs FREQUENCY

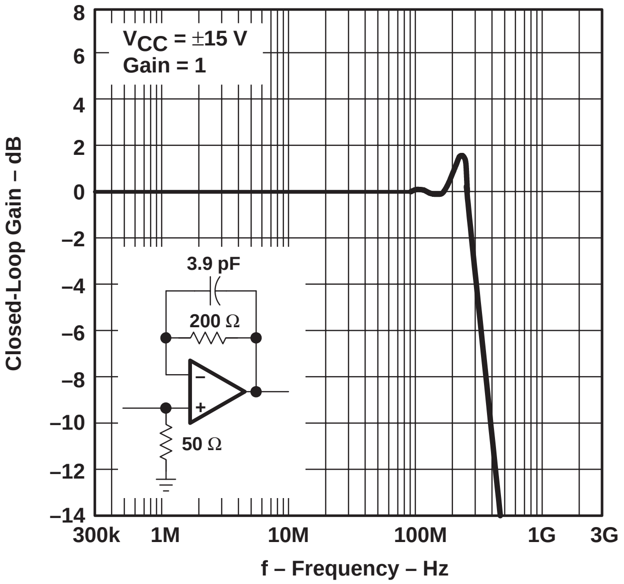


Figure 6

CLOSED-LOOP GAIN vs FREQUENCY

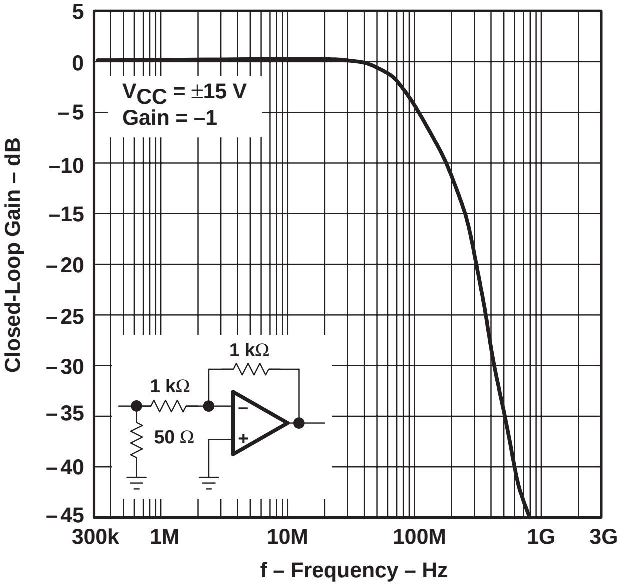


Figure 7

TYPICAL CHARACTERISTICS

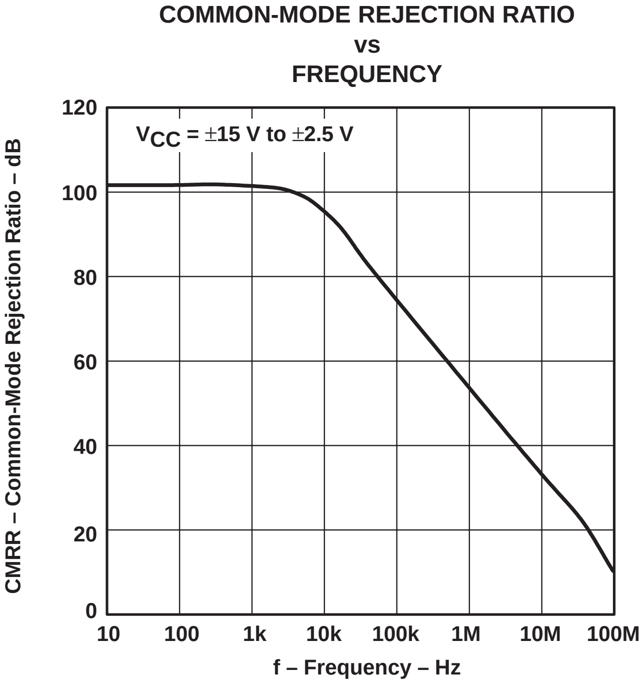


Figure 8

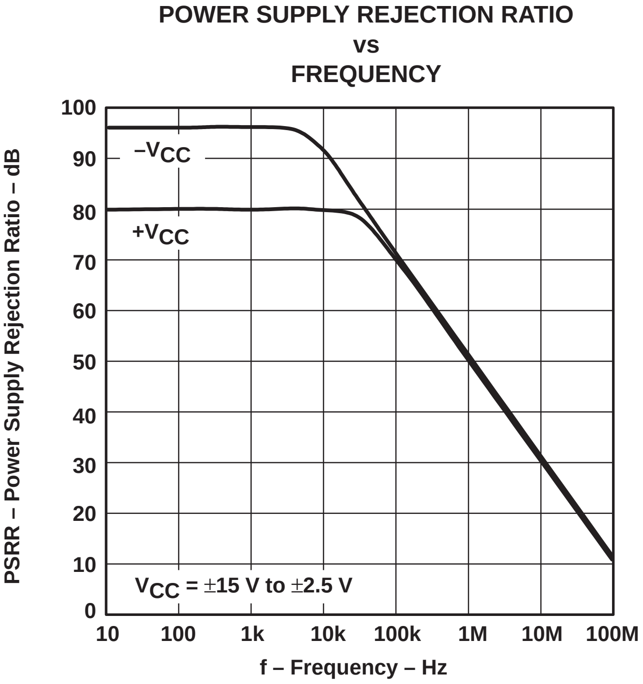


Figure 9

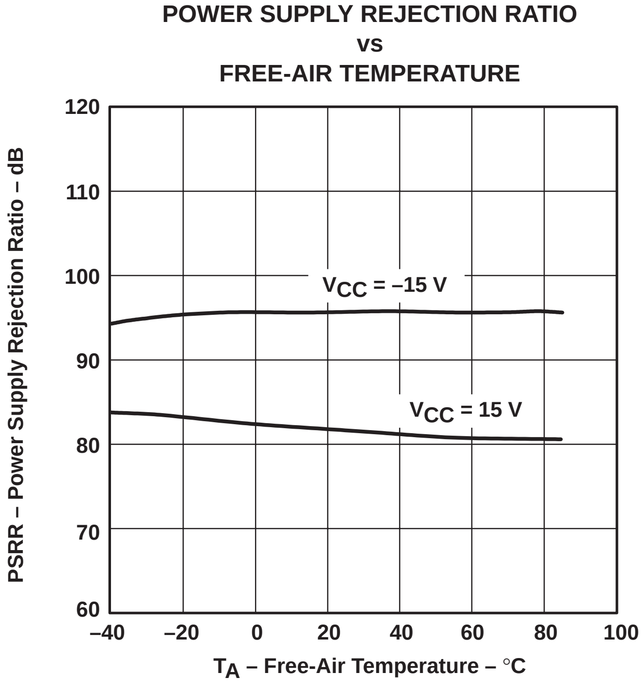


Figure 10

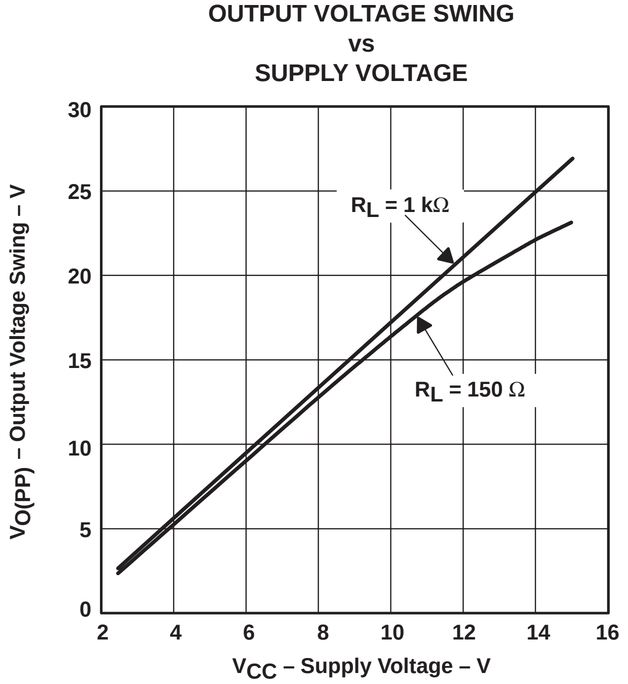


Figure 11

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

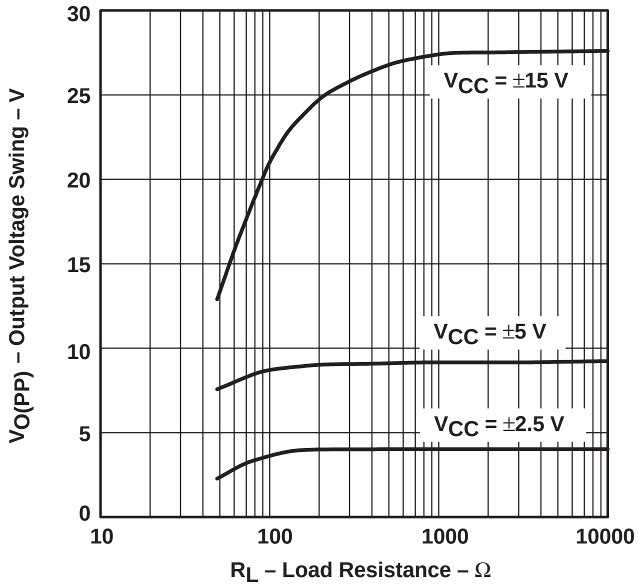


Figure 12

BANDWIDTH (–3 dB) vs FEEDBACK RESISTANCE

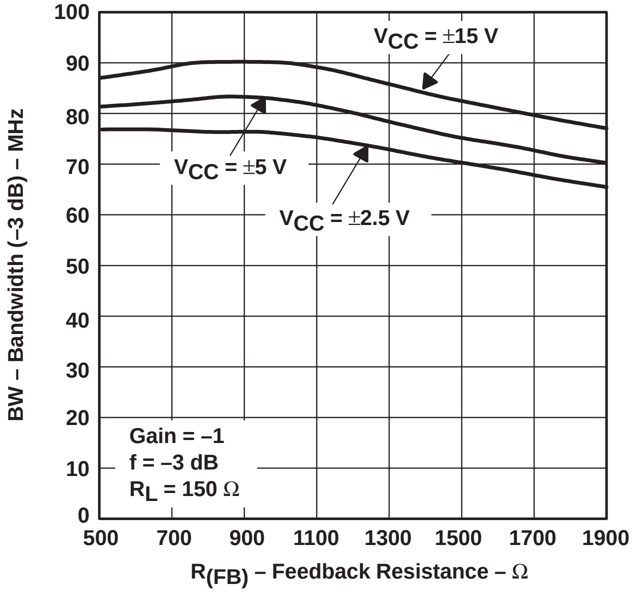


Figure 13

BANDWIDTH (–3 dB) vs FEEDBACK RESISTANCE

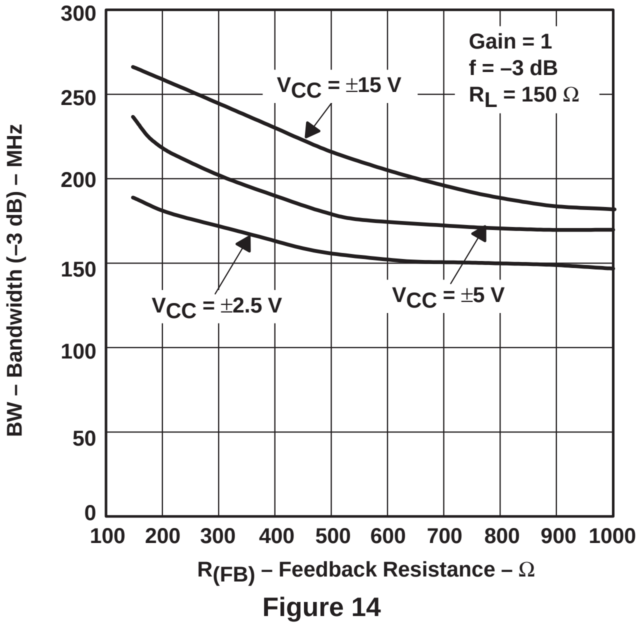


Figure 14

TYPICAL CHARACTERISTICS

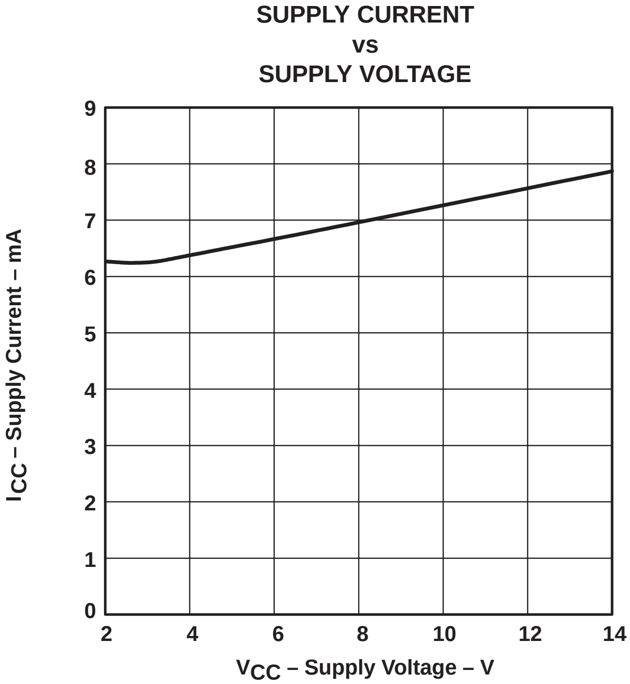


Figure 15

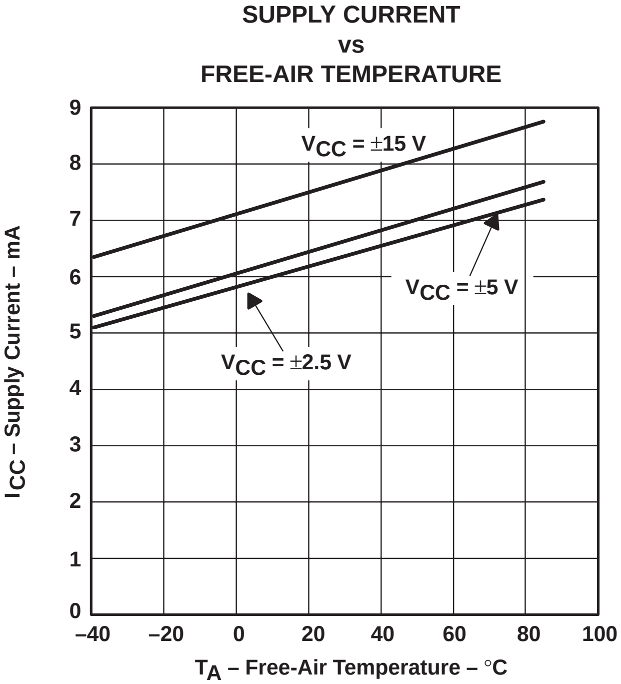


Figure 16

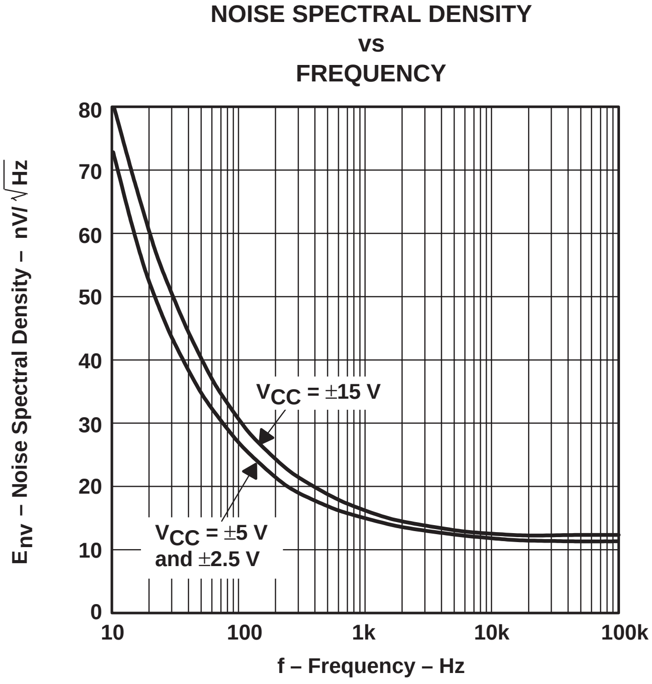


Figure 17

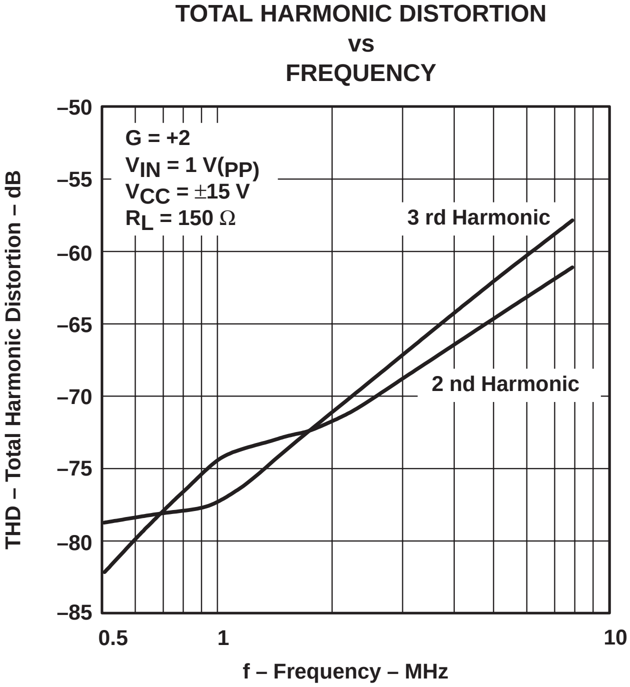


Figure 18

APPLICATION INFORMATION

theory of operation

The THS4001 is a high speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 19.

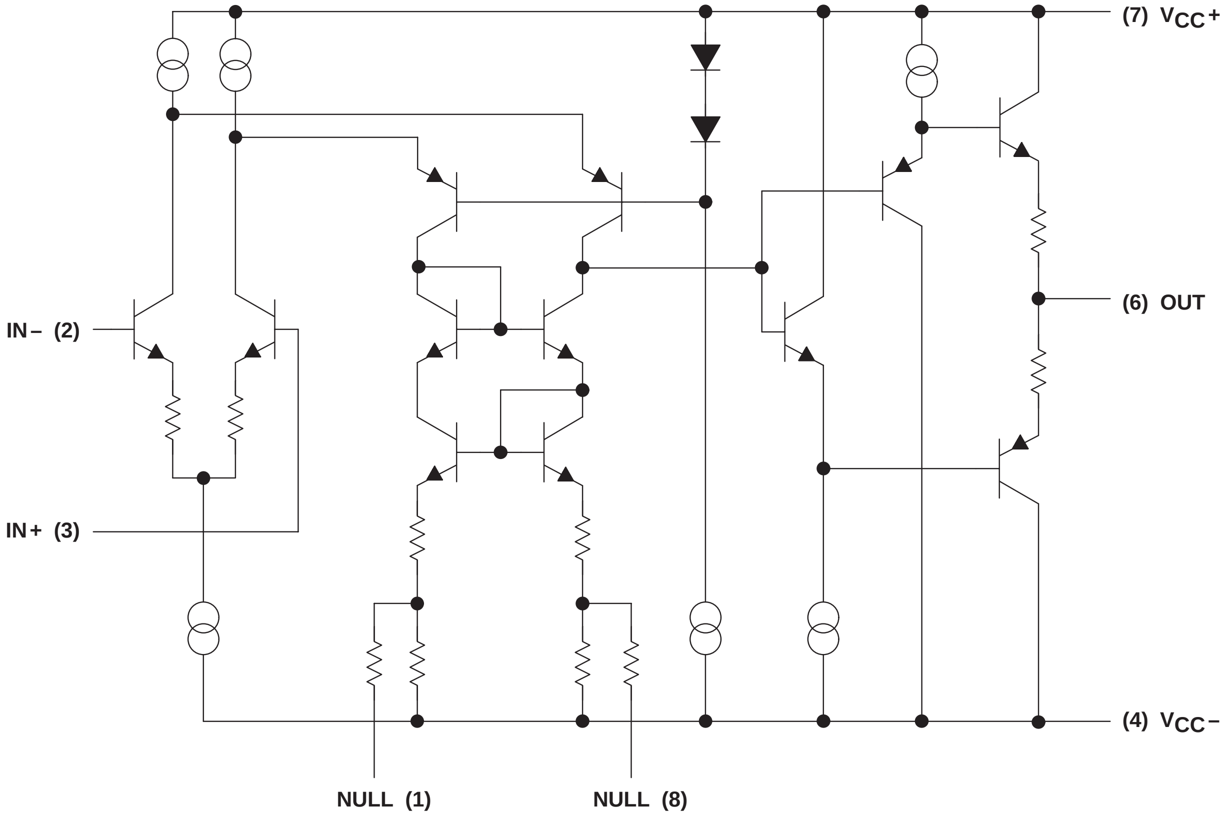


Figure 19. THS4001 Simplified Schematic

APPLICATION INFORMATION

offset nulling

The THS4001 has very low input offset voltage for a high speed amplifier. However, if additional correction is required, an offset nulling function has been provided. By placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply the input offset can be adjusted. This is shown in Figure 20.

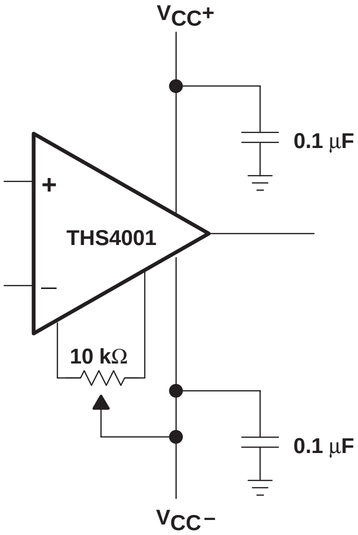


Figure 20. Offset Nulling Schematic

optimizing unity gain response

Internal frequency compensation of the THS4001 was selected to provide very wideband performance yet still maintain stability when operated in a noninverting unity gain configuration. When amplifiers are compensated in this manner there is usually peaking in the closed loop response and some ringing in the step response for very fast input edges, depending upon the application. This is because a minimum phase margin is maintained for the G=+1 configuration. For optimum settling time and minimum ringing, a feedback resistor of 200 Ω should be used as shown in Figure 21. Additional capacitance can also be used in parallel with the feedback resistance if even finer optimization is required.

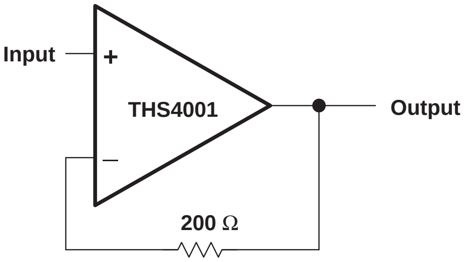


Figure 21. Non-Inverting, Unity Gain Schematic

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS4001 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 22. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

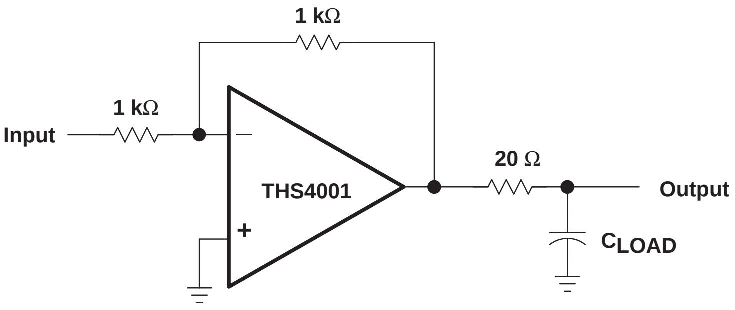


Figure 22. Driving a Capacitive Load

circuit layout considerations

In order to achieve the levels of high frequency performance of the THS4001, it is essential that proper printed circuit board high frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS4001 evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distances increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high speed op amps. The additional lead inductance in the socket pins will often lead to stability problems. Surface mount packages soldered directly to the printed circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.

APPLICATION INFORMATION

circuit layout considerations (continued)

- Surface mount passive components – Using surface mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

evaluation board

An evaluation board is available for the THS4001. This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 23. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. To order the evaluation board contact your local TI sales office or distributor. Refer to literature number SLOP 119.

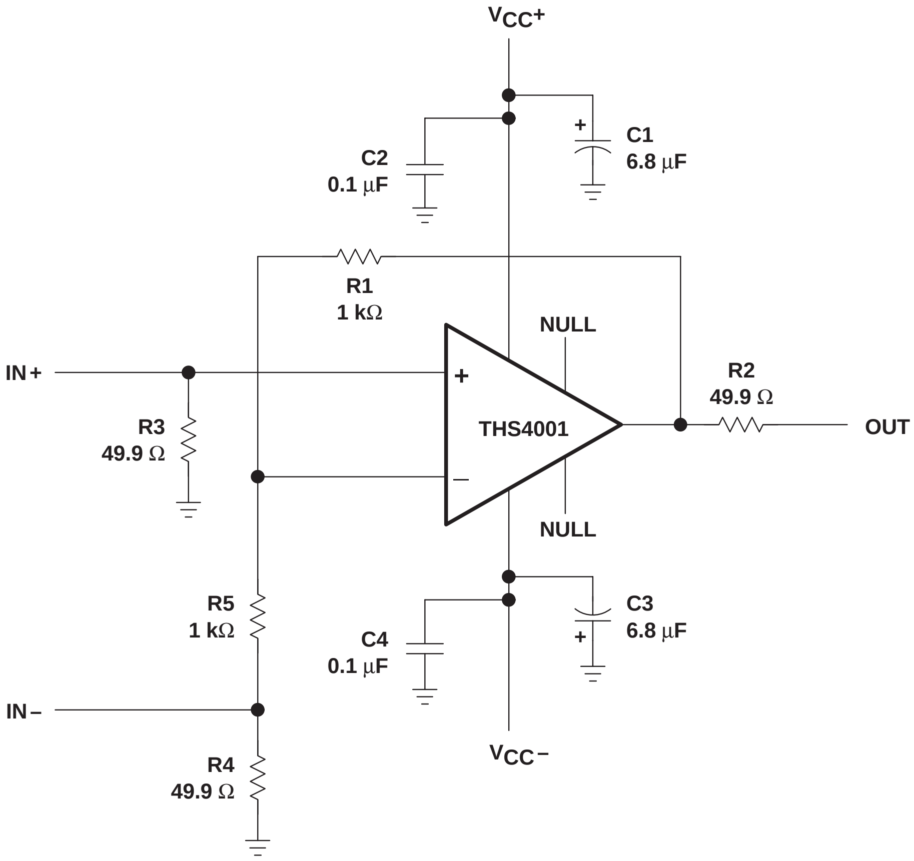
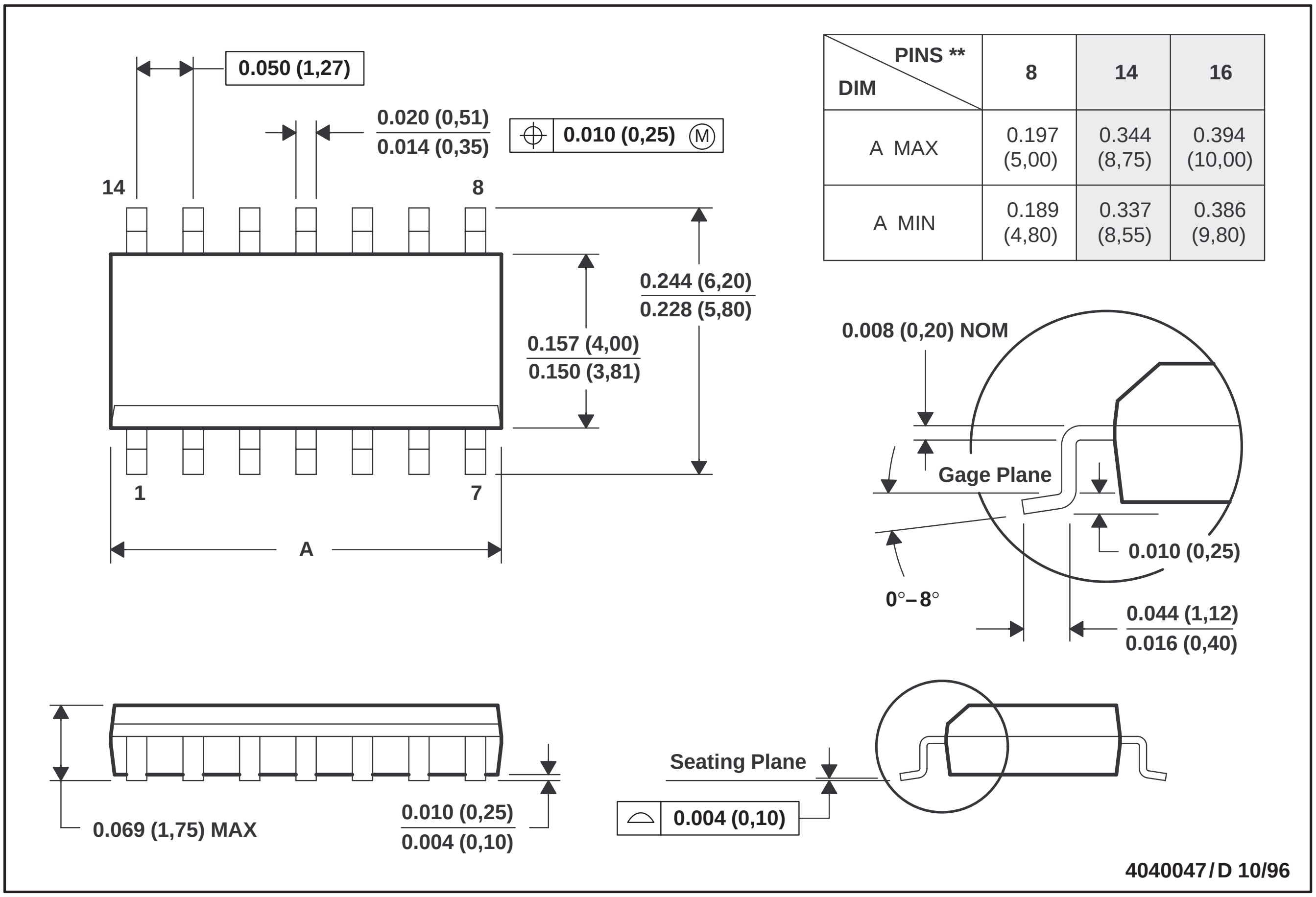


Figure 23.

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

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