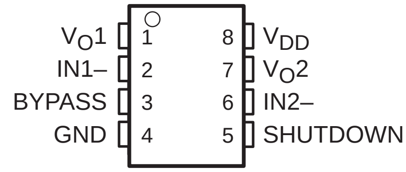
- **150 mW Stereo Output**
- **PC Power Supply Compatible**
  - **Fully Specified for 3.3 V and 5 V Operation**
  - **Operation to 2.5 V**
- **Pop Reduction Circuitry**
- **Internal Mid-Rail Generation**
- **Thermal and Short-Circuit Protection**
- **Surface Mount Packaging**
  - **PowerPAD™ MSOP**
  - **SOIC**
- **Pin Compatible with LM4880 amd LM4881 (SOIC)**

D OR DGN PACKAGE
(TOP VIEW)

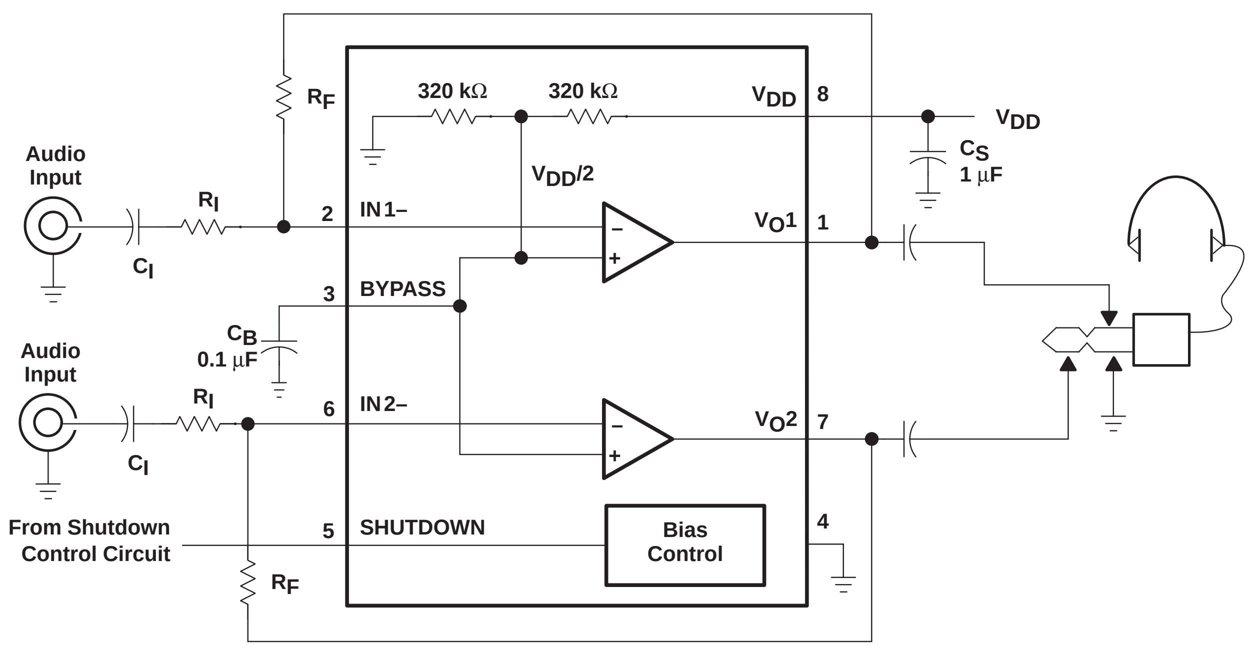


description

The TPA122 is a stereo audio power amplifier packaged in either an 8-pin SOIC, or an 8-pin PowerPAD™ MSOP package capable of delivering 150 mW of continuous RMS power per channel into 8-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10.

THD+N when driving an 8-Ω load from 5 V is 0.1% at 1 kHz, and less than 2% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.06% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz. For 10-kΩ loads, the THD+N performance is 0.01% at 1 kHz, and less than 0.02% across the audio band of 20 Hz to 20 kHz.

typical application circuit



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MSOP Symbolization
	SMALL OUTLINE† (D)	MSOP† (DGN)	
–40°C to 85°C	TPA122D	TPA122DGN	TI AAE

† The D and DGN package is available in left-ended tape and reel only (e.g., TPA122DR, TPA122DGNR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	3	I	Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1 µF to 1 µF low ESR capacitor for best performance.
GND	4	I	GND is the ground connection.
IN1–	2	I	IN1– is the inverting input for channel 1.
IN2–	6	I	IN2– is the inverting input for channel 2.
SHUTDOWN	5	I	Puts the device in a low quiescent current mode when held high
V_{DD}	8	I	V_{DD} is the supply voltage terminal.
V_O1	1	O	V_O1 is the audio output for channel 1.
V_O2	7	O	V_O2 is the audio output for channel 2.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} . . . . 6 V
Input voltage, V_I . . . . –0.3 V to V_{DD} + 0.3 V
Continuous total power dissipation . . . . internally limited
Operating junction temperature range, T_J . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W‡	17.1 mW/°C	1.37 W	1.11 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.5	5.5	V
Operating free-air temperature, T_A	–40	85	°C

dc electrical characteristics at T_A = 25°C, V_{DD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage				5	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		83		dB
$I_{DD(q)}$	Supply current			1.5	3	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode			10	50	µA
Z_I	Input impedance			>1		MΩ

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%			70†		mW
THD+N	Total harmonic distortion + noise	P_O = 70 mW,	20–20 kHz		2%		
B_{OM}	Maximum output power BW	G = 10,	THD <5%		>20		kHz
	Phase margin	Open loop			58°		
S_{VRR}	Supply ripple rejection	f = 1 kHz			68		dB
	Channel/Channel output separation	f = 1 kHz			86		dB
SNR	Signal-to-noise ratio	P_O = 100 mW			100		dB
V_n	Noise output voltage				9.5		µV(rms)

† Measured at 1 kHz

dc electrical characteristics at T_A = 25°C, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage				5	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		76		dB
$I_{DD(q)}$	Supply current			1.5	3	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode			60	100	µA
Z_I	Input impedance			>1		MΩ

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%			70†		mW
THD+N	Total harmonic distortion + noise	P_O = 150 mW,	20–20 kHz		2%		
B_{OM}	Maximum output power BW	G = 10,	THD <5%		>20		kHz
	Phase margin	Open loop			56°		
S_{VRR}	Supply ripple rejection	f = 1 kHz			68		dB
	Channel/Channel output separation	f = 1 kHz			86		dB
SNR	Signal-to-noise ratio	P_O = 150 mW			100		dB
V_n	Noise output voltage				9.5		µV(rms)

† Measured at 1 kHz

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		40†		mW
THD+N	Total harmonic distortion + noise	P_O = 30 mW, 20–20 kHz		0.5%		
B_{OM}	Maximum output power BW	G = 10, THD <2%		>20		kHz
	Phase margin	Open loop		58°		
S_{VRR}	Supply ripple rejection	f = 1 kHz		68		dB
	Channel/Channel output separation	f = 1 kHz		86		dB
SNR	Signal-to-noise ratio	P_O = 100 mW		100		dB
V_n	Noise output voltage			9.5		µV(rms)

† Measured at 1 kHz

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD ≤ 0.1%		40†		mW
THD+N	Total harmonic distortion + noise	P_O = 60 mW, 20–20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 10, THD <2%		>20		kHz
	Phase margin	Open loop		56°		
S_{VRR}	Supply ripple rejection	f = 1 kHz		68		dB
	Channel/Channel output separation	f = 1 kHz		86		dB
SNR	Signal-to-noise ratio	P_O = 150 mW		100		dB
V_n	Noise output voltage			9.5		µV(rms)

† Measured at 1 kHz

TYPICAL CHARACTERISTICS

Table of Graphs

	Output power	vs Load resistance	31, 32
			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1, 2, 4, 5, 7, 8, 10, 11, 13, 14, 16, 17, 34, 36
		vs Power output	3, 6, 9, 12, 15, 18
PSSR	Power supply rejection ratio	vs Frequency	19, 20
V_n	Output noise voltage	vs Frequency	21, 22
	Crosstalk	vs Frequency	23 – 26, 37, 38
	Mute attenuation	vs Frequency	27, 28
	Open-loop gain	vs Frequency	29, 30
	Phase margin	vs Frequency	29
	Phase	vs Frequency	30, 39 – 44
	Output power	vs Load resistance	31, 32
I_{CC}	Supply current	vs Supply voltage	33
SNR	Signal-to-noise ratio	vs Voltage gain	35
	Closed-loop gain	vs Frequency	39 – 44
	Power dissipation	vs Output power	45, 46

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

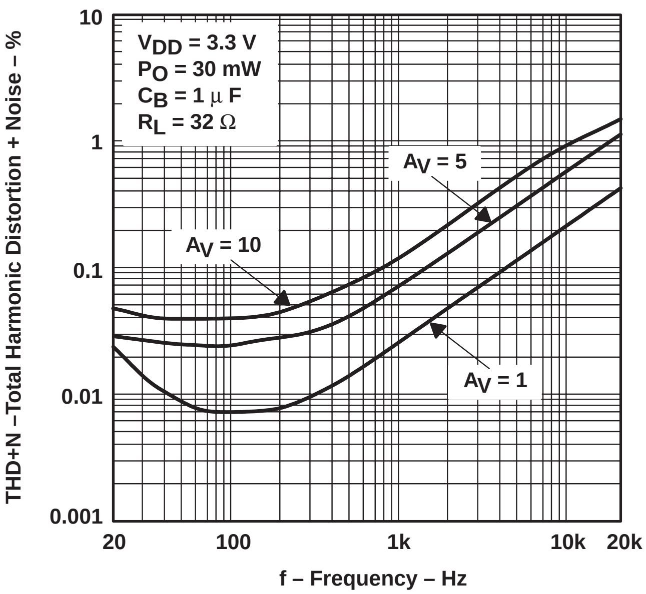


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

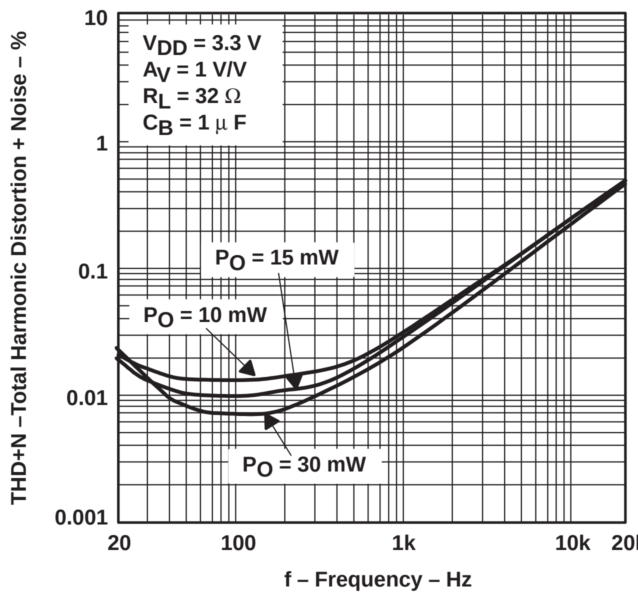


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

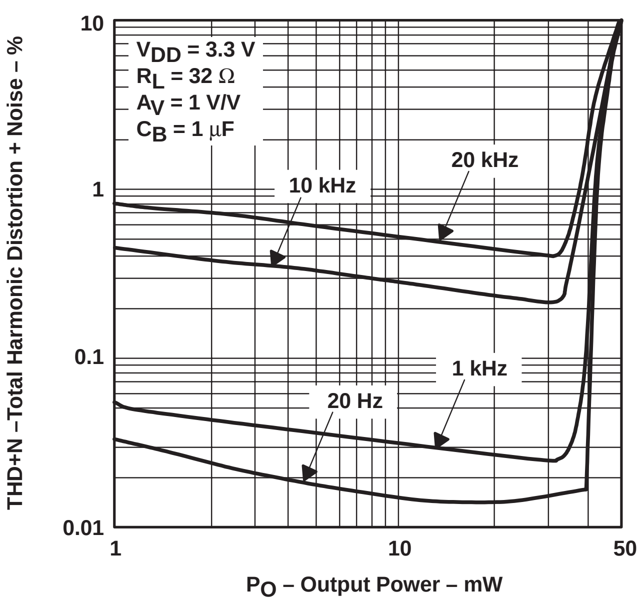


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

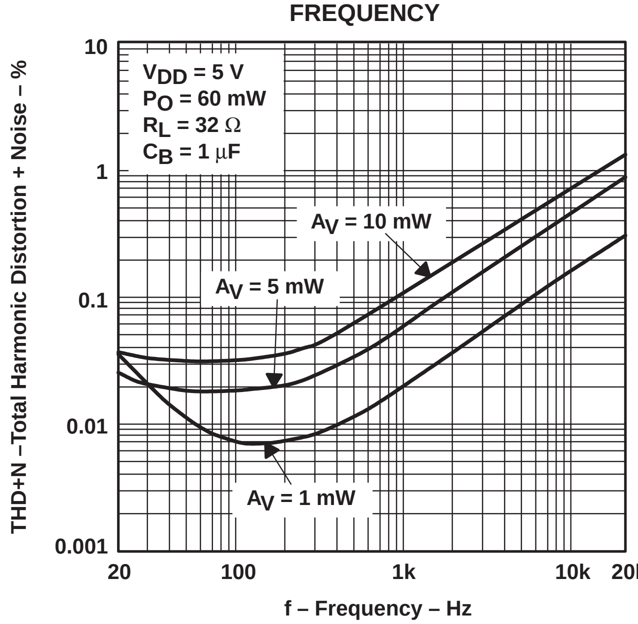


Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

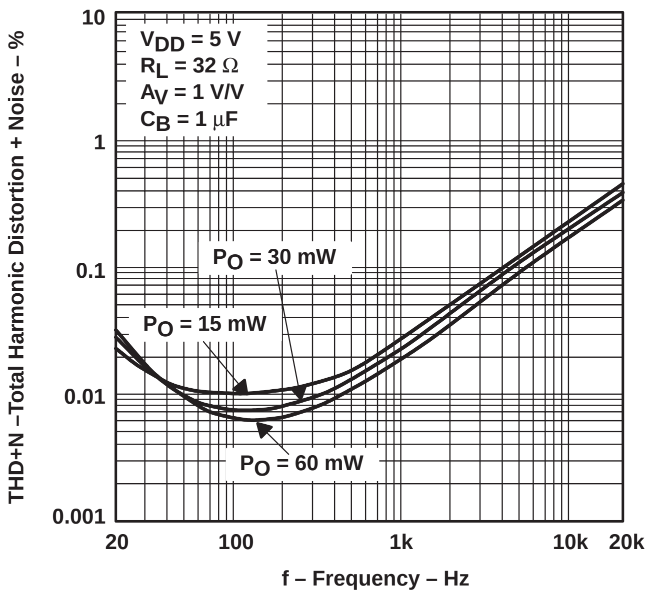


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

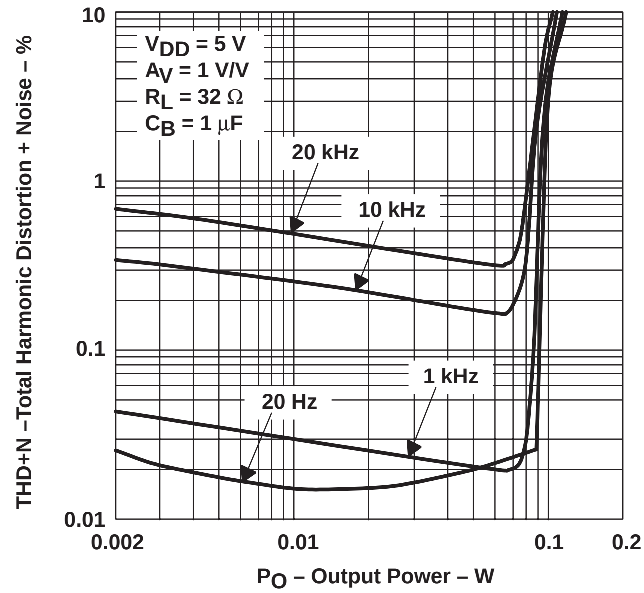


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

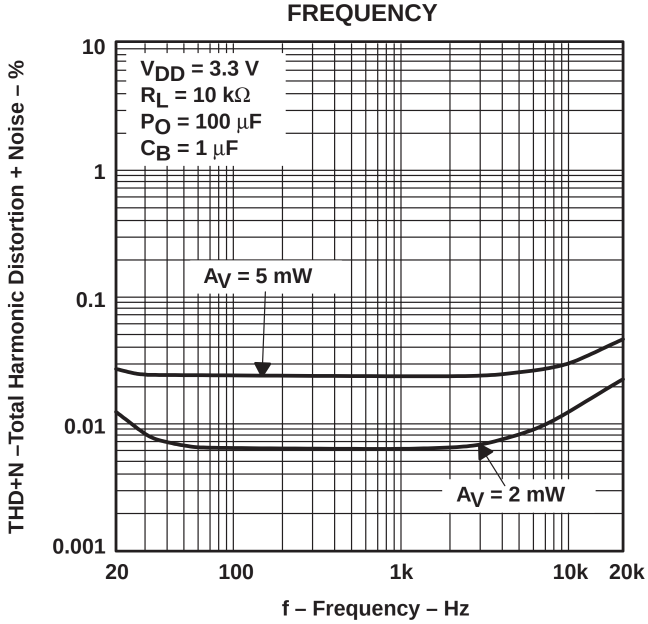


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

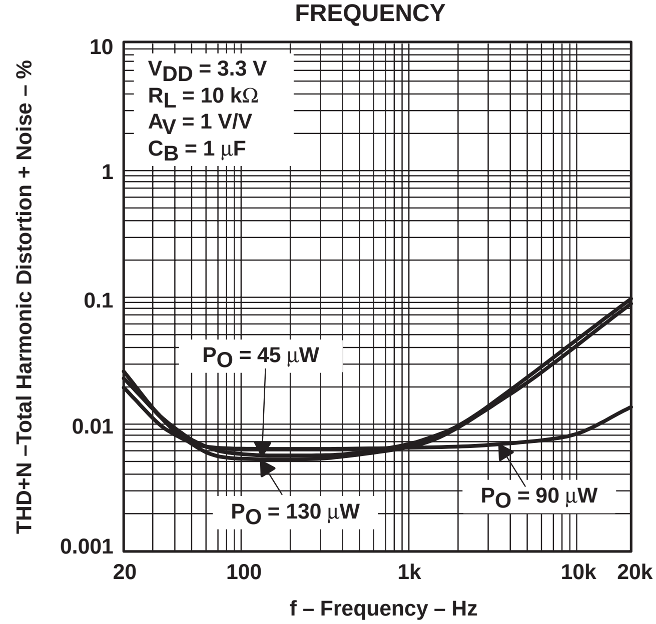


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

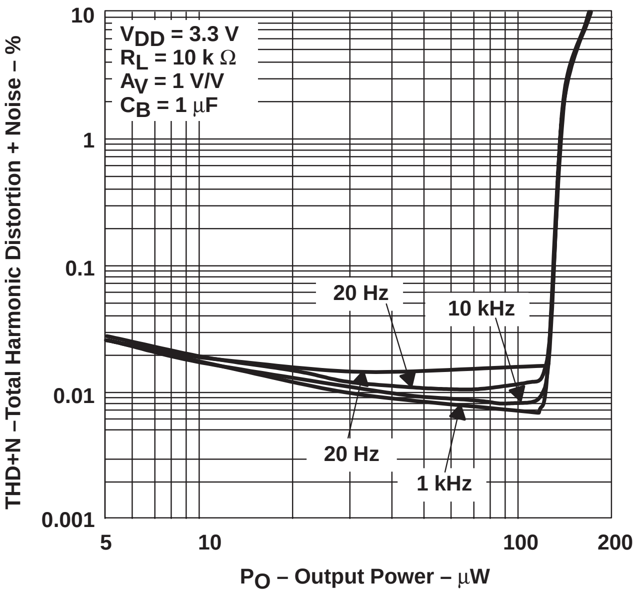


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

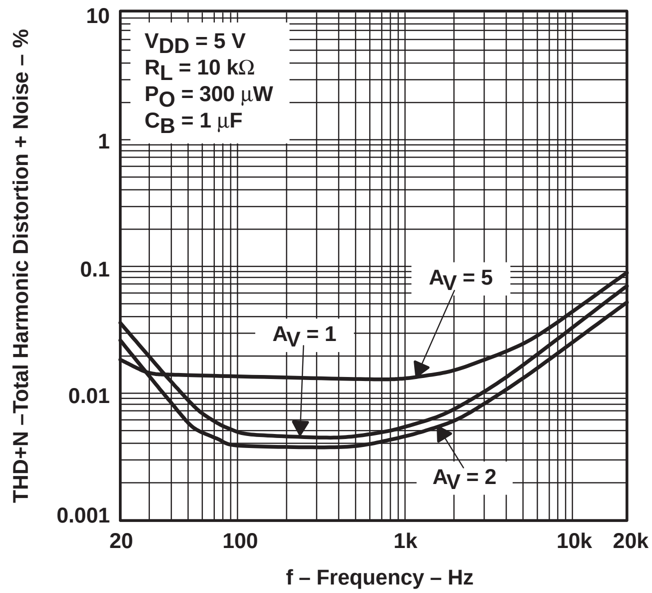


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

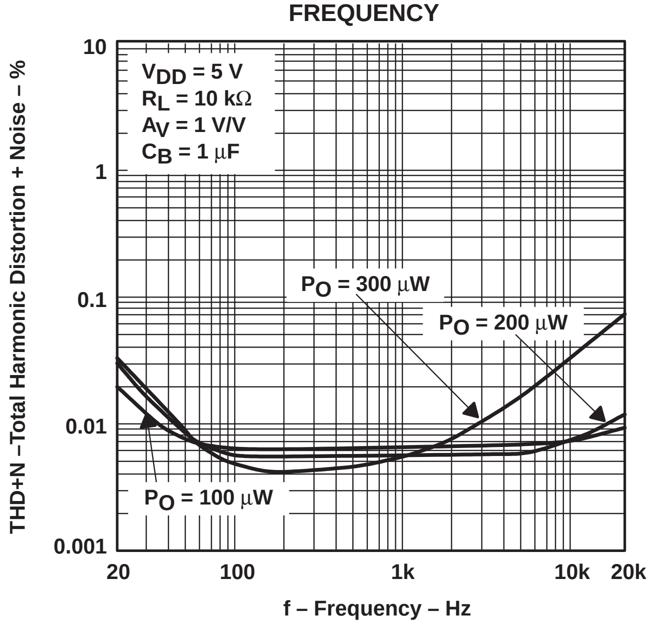


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

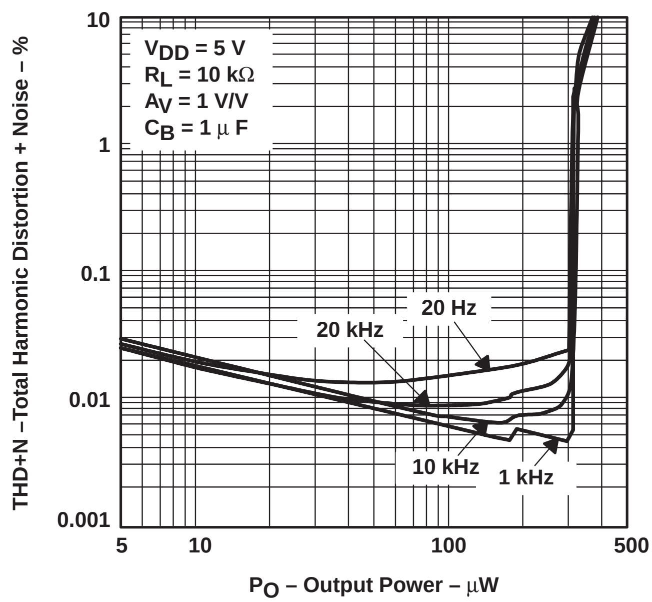


Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

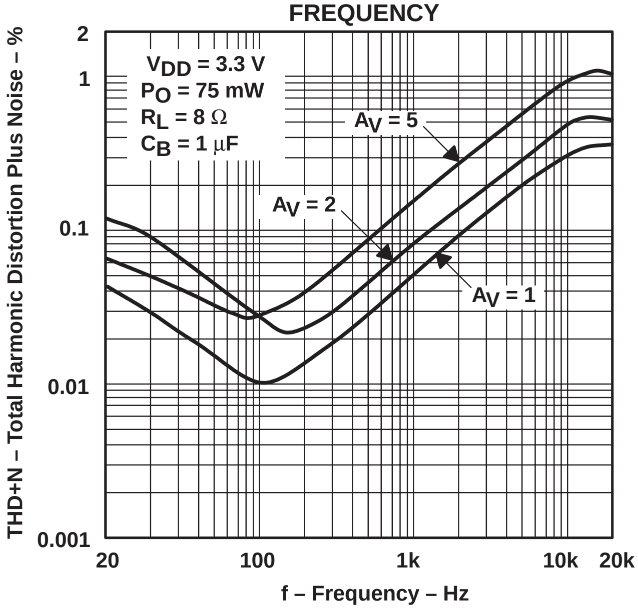


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

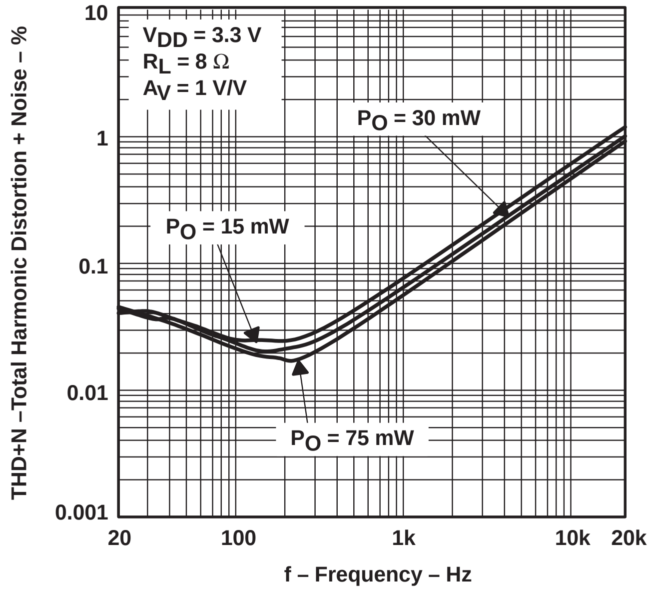


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

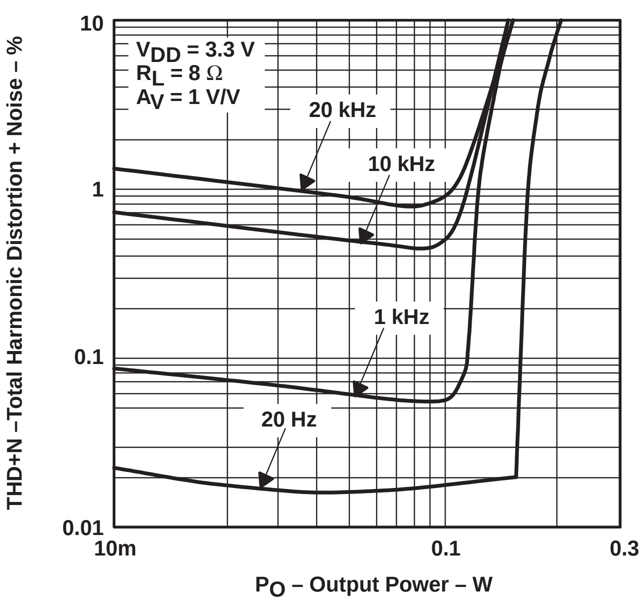


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

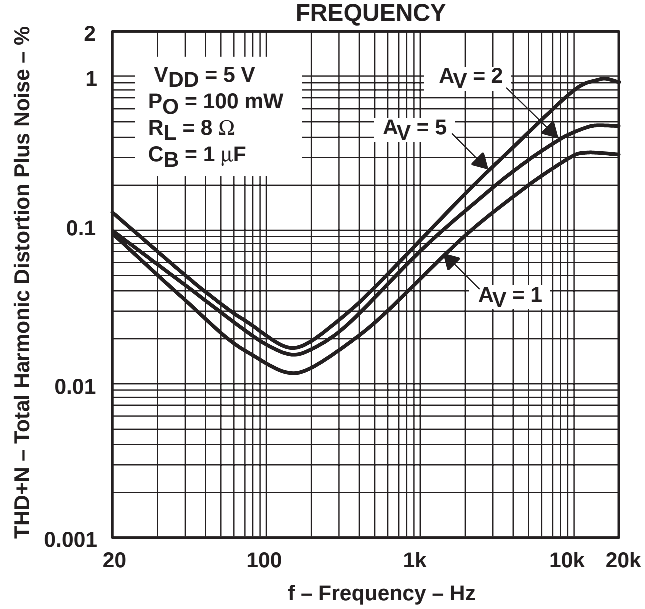


Figure 16

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

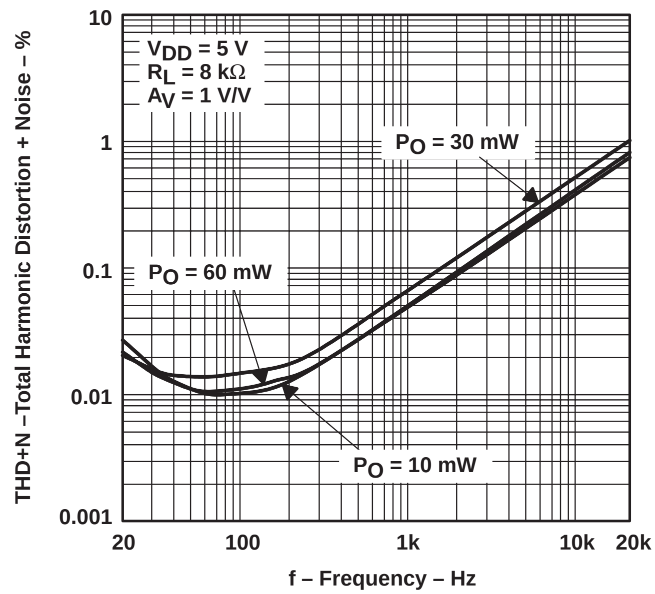


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE vs POWER OUTPUT

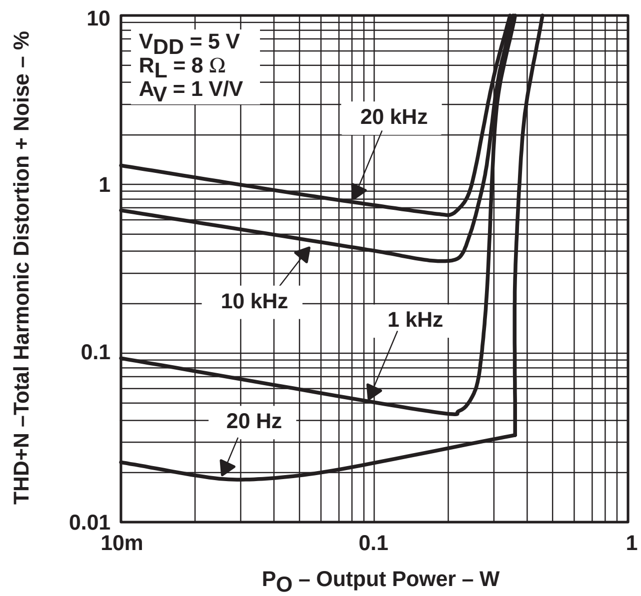


Figure 18

POWER SUPPLY REJECTION RATIO vs FREQUENCY

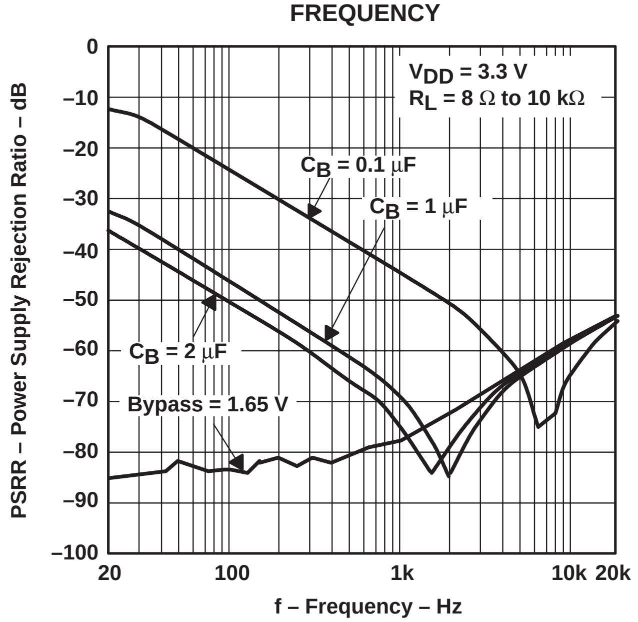


Figure 19

POWER SUPPLY REJECTION RATIO vs FREQUENCY

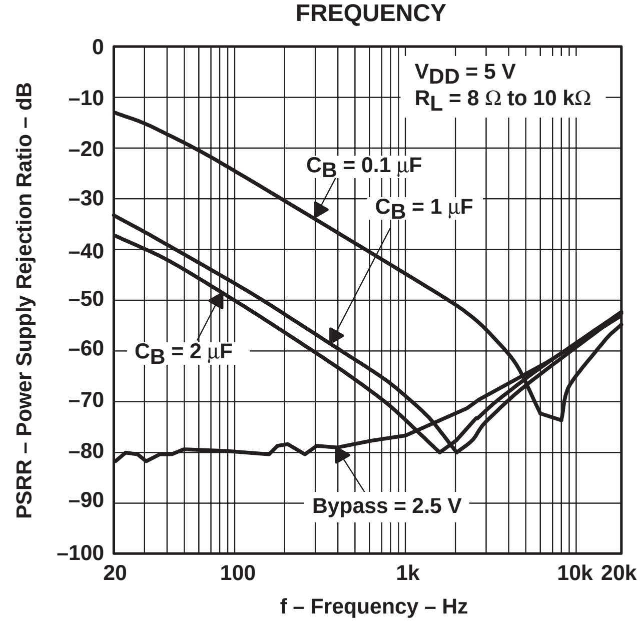


Figure 20

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

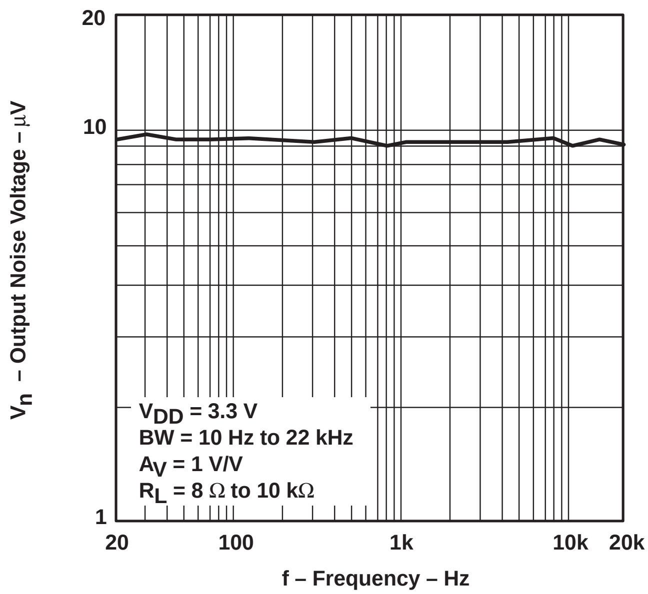


Figure 21

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

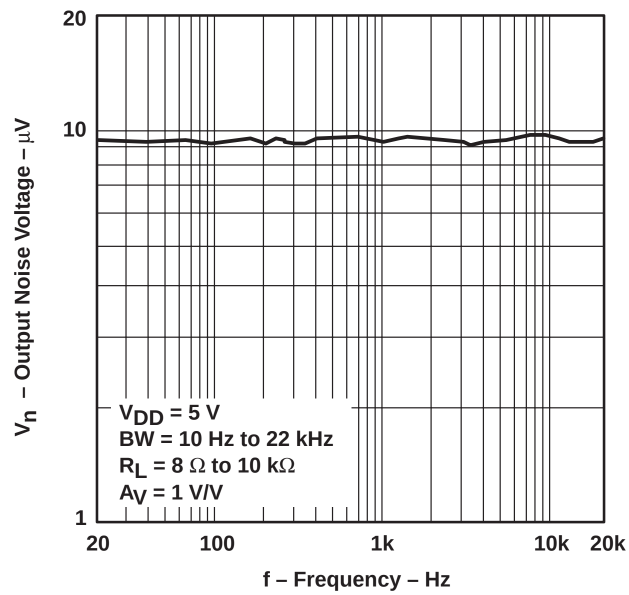


Figure 22

CROSSTALK
vs
FREQUENCY

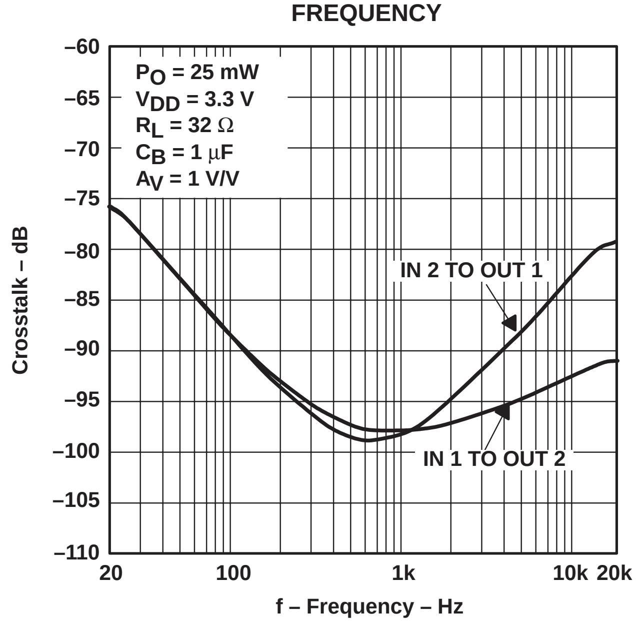


Figure 23

CROSSTALK
vs
FREQUENCY

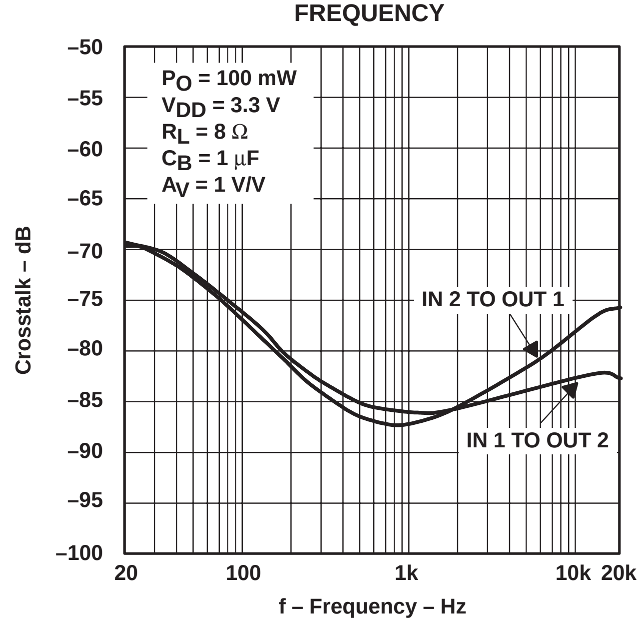


Figure 24

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

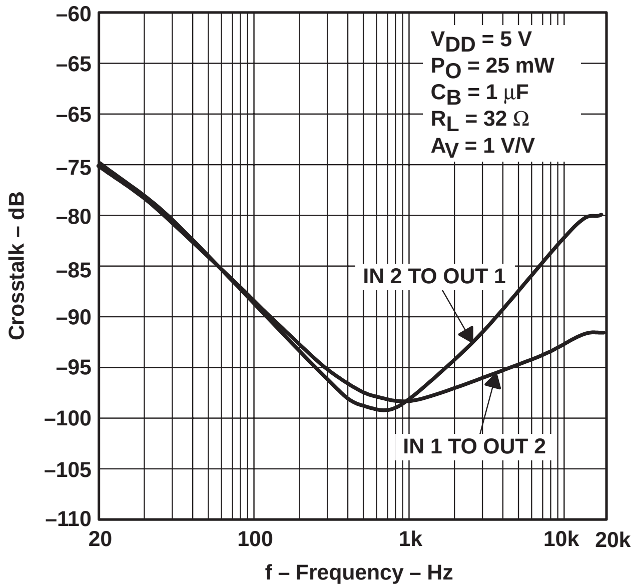


Figure 25

CROSSTALK
vs
FREQUENCY

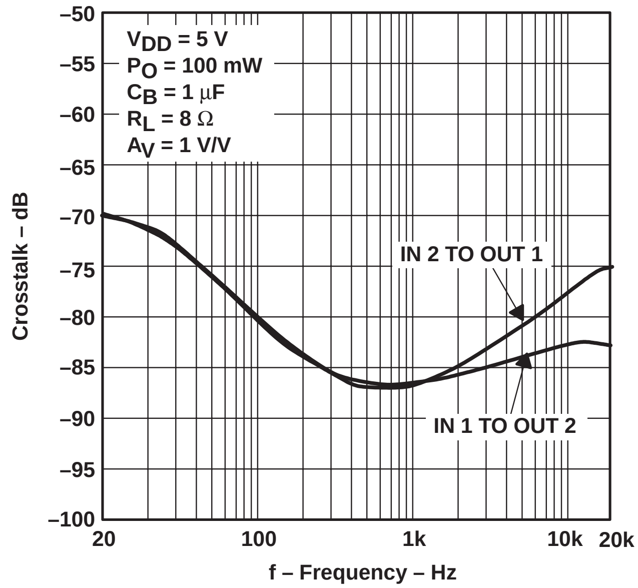


Figure 26

MUTE ATTENUATION
vs
FREQUENCY

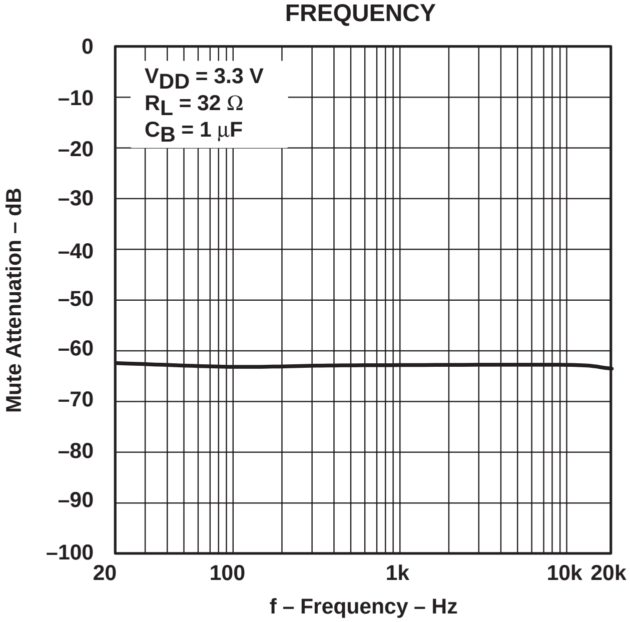


Figure 27

MUTE ATTENUATION
vs
FREQUENCY

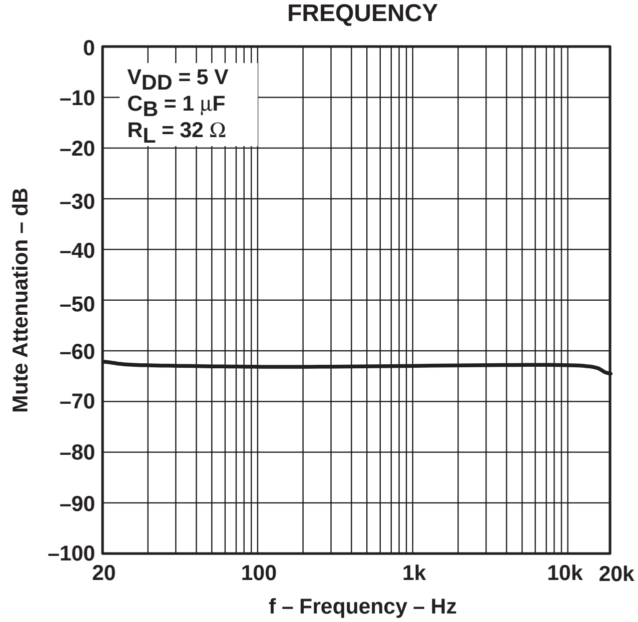


Figure 28

TYPICAL CHARACTERISTICS

**OPEN–LOOP GAIN AND PHASE MARGIN
vs
FREQUENCY**

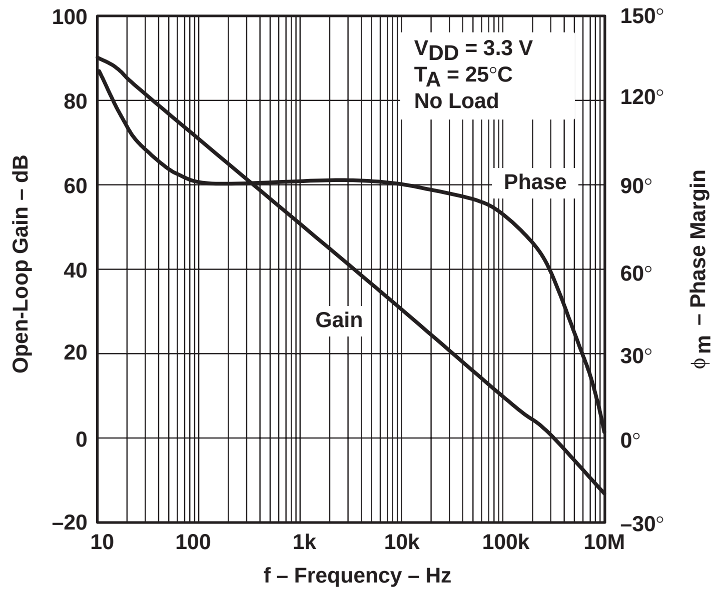


Figure 29

**OPEN–LOOP GAIN AND PHASE MARGIN
vs
FREQUENCY**

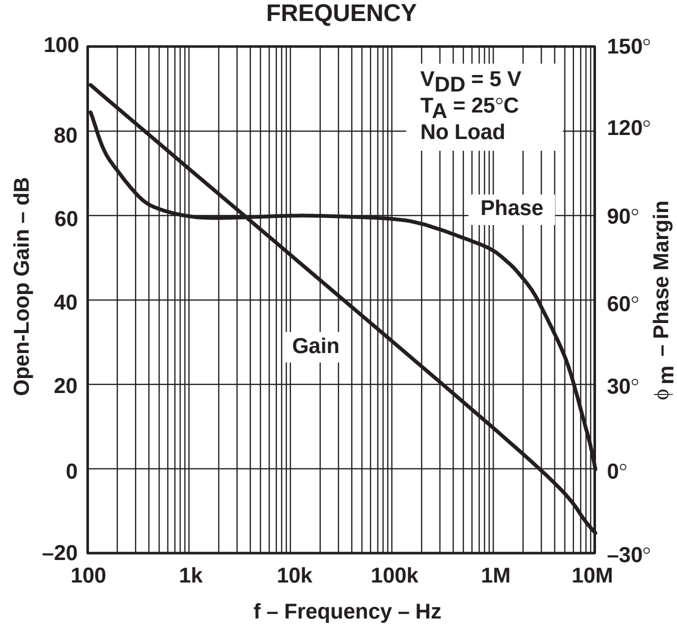


Figure 30

TYPICAL CHARACTERISTICS

OUTPUT POWER vs LOAD RESISTANCE

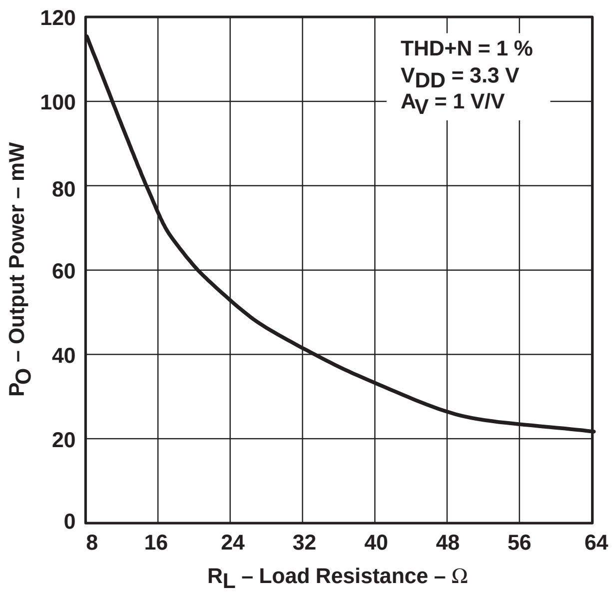


Figure 31

OUTPUT POWER vs LOAD RESISTANCE

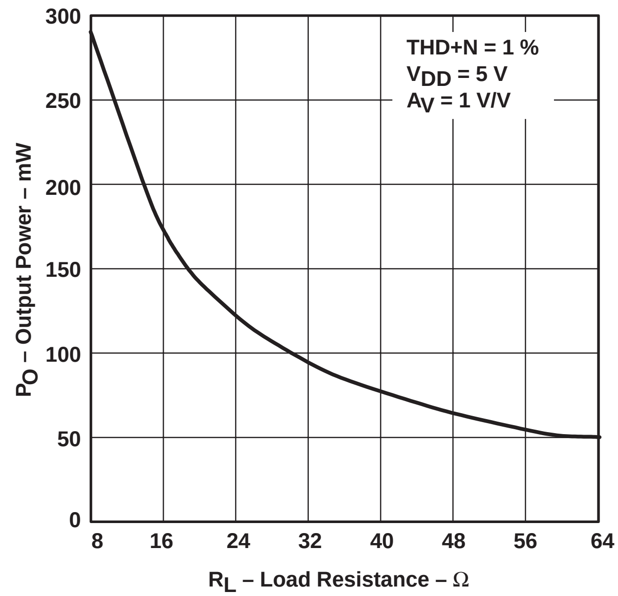


Figure 32

SUPPLY CURRENT vs SUPPLY VOLTAGE

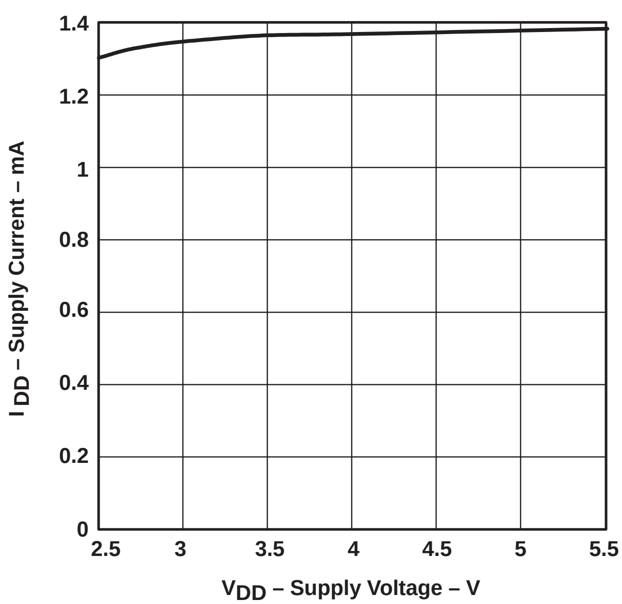


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

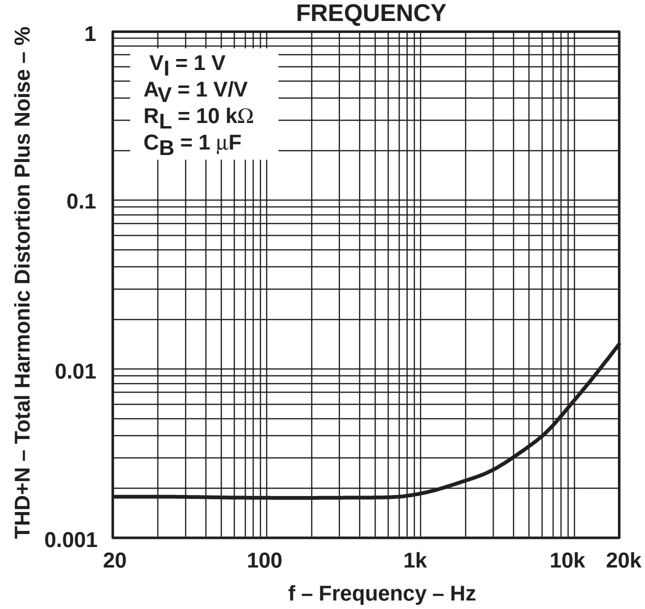


Figure 34

TYPICAL CHARACTERISTICS

SIGNAL–TO–NOISE RATIO vs VOLTAGE GAIN

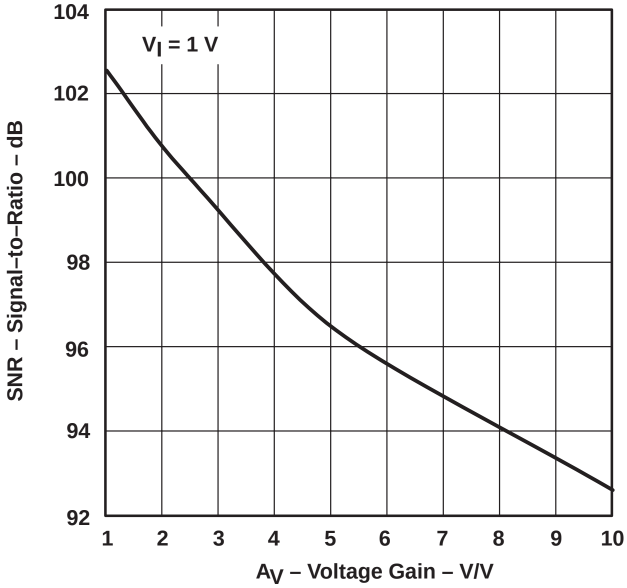


Figure 35

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

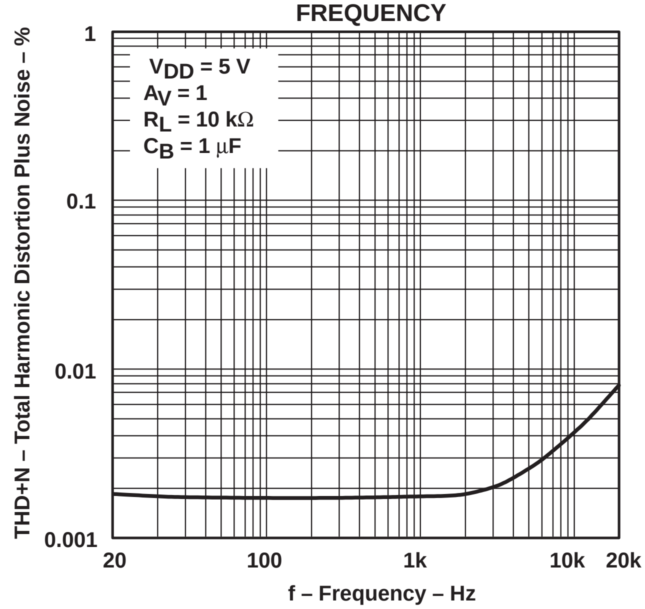


Figure 36

CROSSTALK vs FREQUENCY

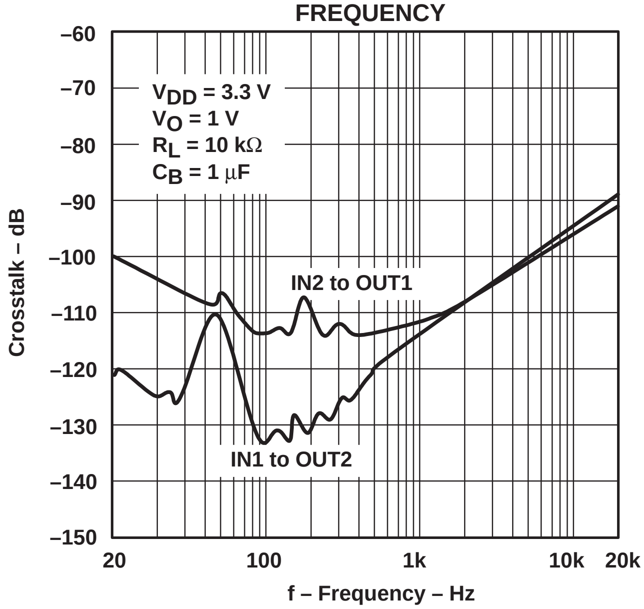


Figure 37

CROSSTALK vs FREQUENCY

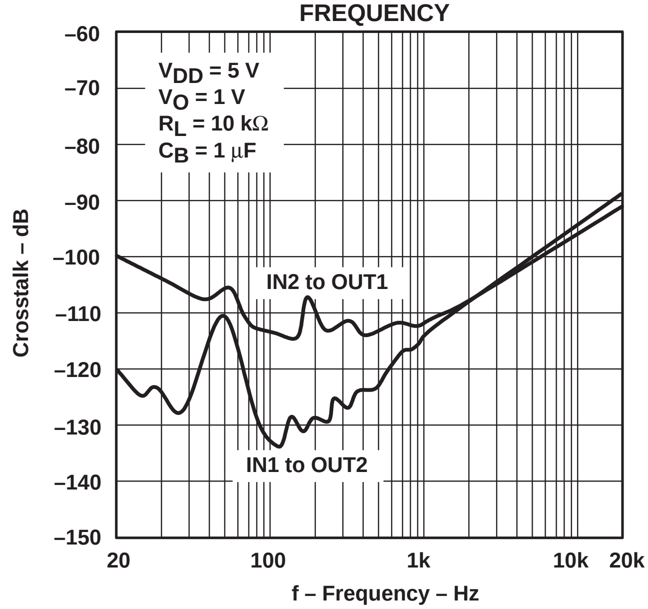


Figure 38

TYPICAL CHARACTERISTICS

CLOSED–LOOP GAIN AND PHASE
vs
FREQUENCY

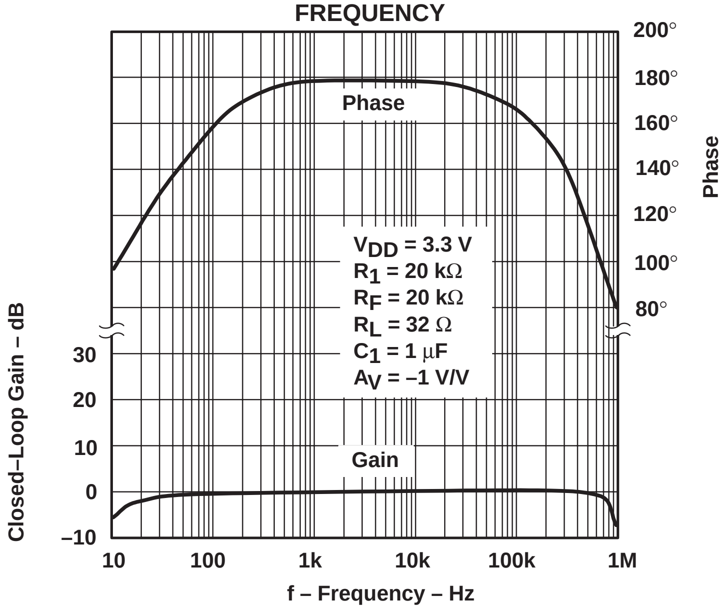


Figure 39

CLOSED–LOOP GAIN AND PHASE
vs
FREQUENCY

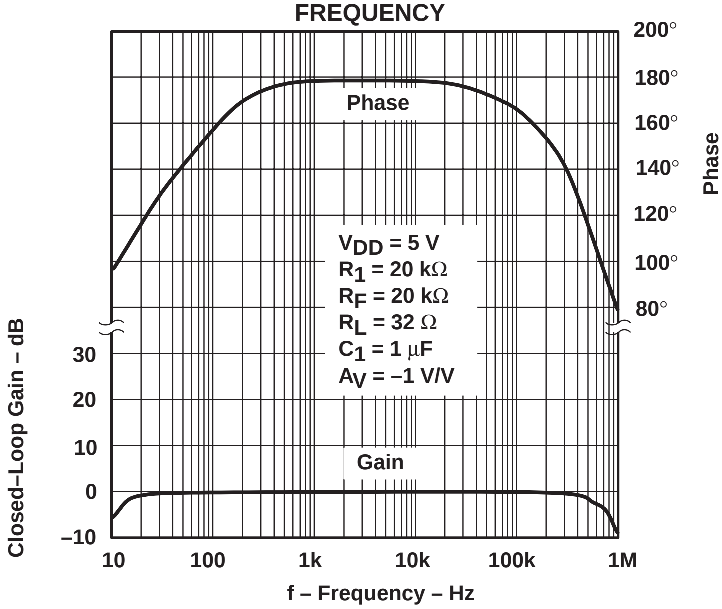


Figure 40

TYPICAL CHARACTERISTICS

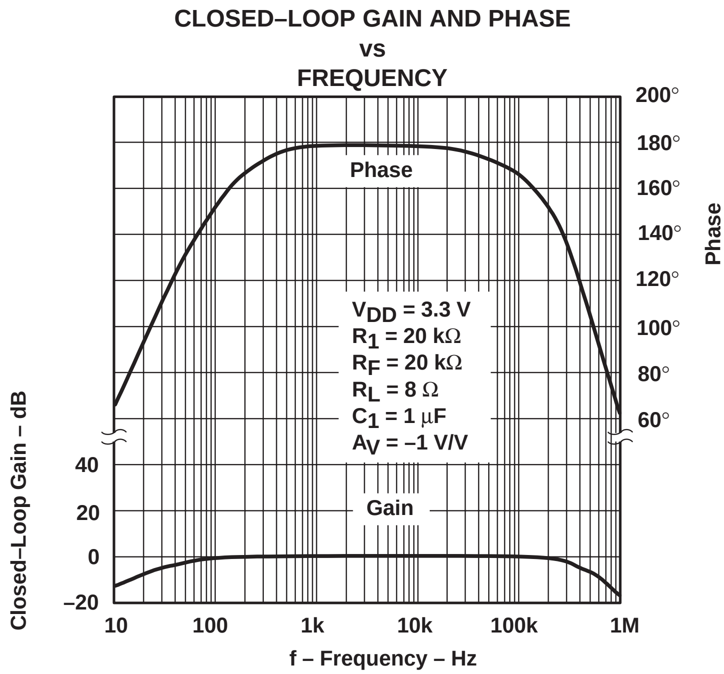


Figure 41

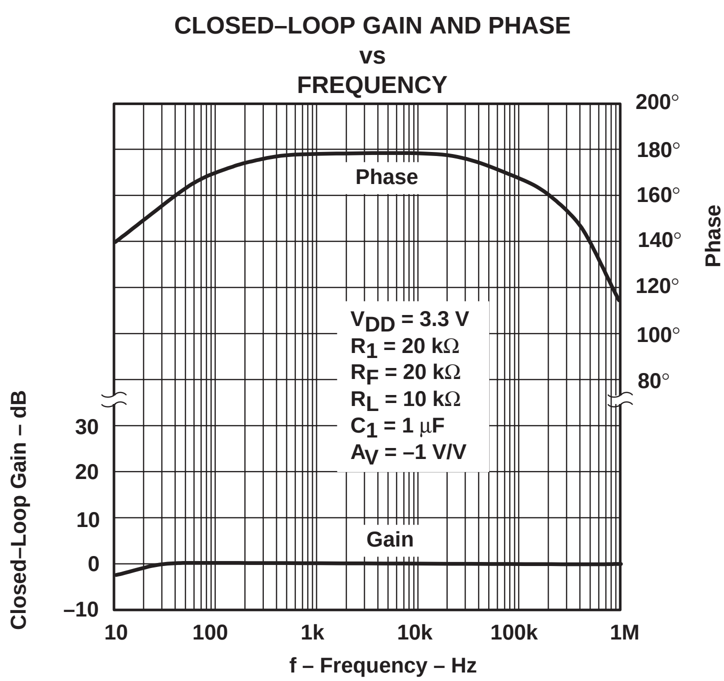


Figure 42

TYPICAL CHARACTERISTICS

**CLOSED–LOOP GAIN AND PHASE
vs
FREQUENCY**

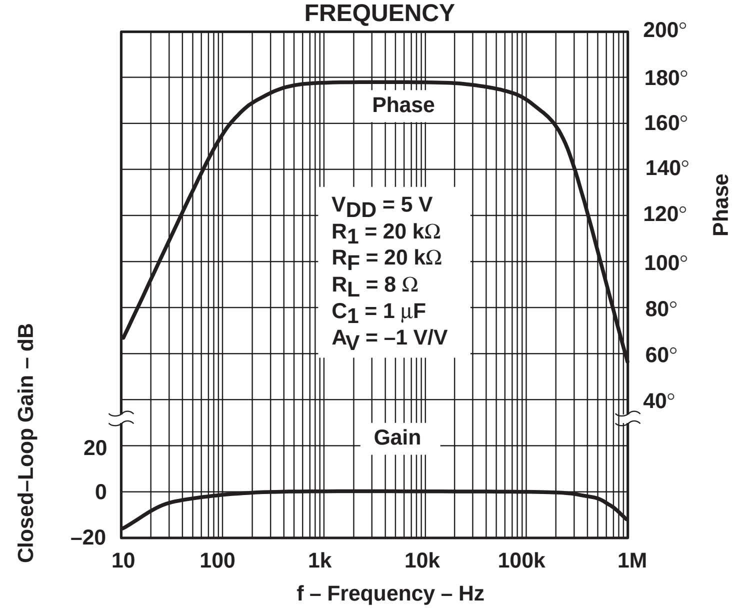


Figure 43

**CLOSED–LOOP GAIN AND PHASE
vs
FREQUENCY**

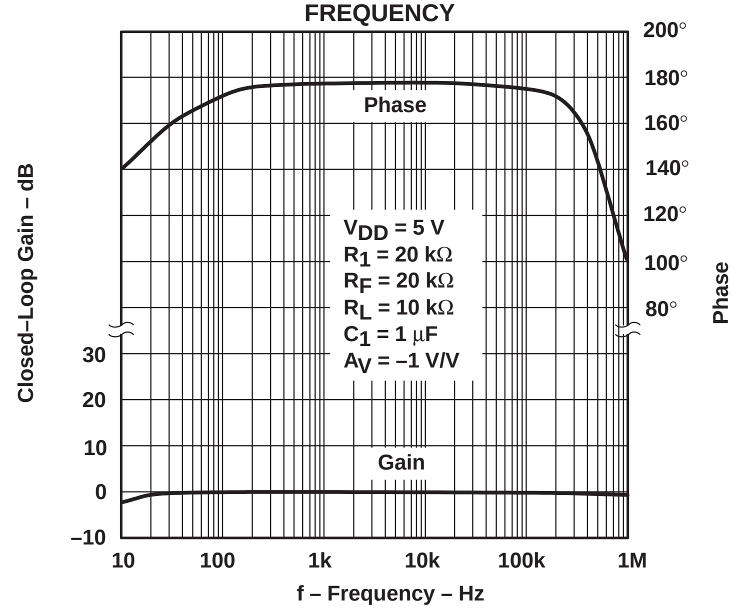


Figure 44

TYPICAL CHARACTERISTICS

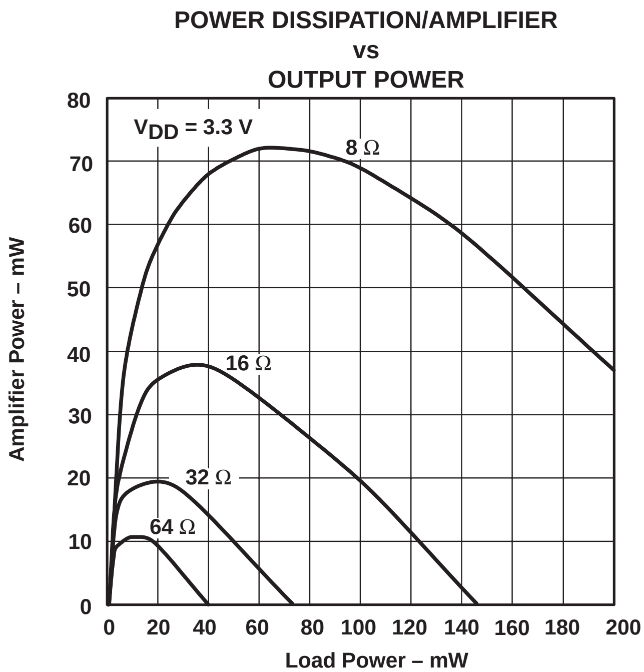


Figure 45

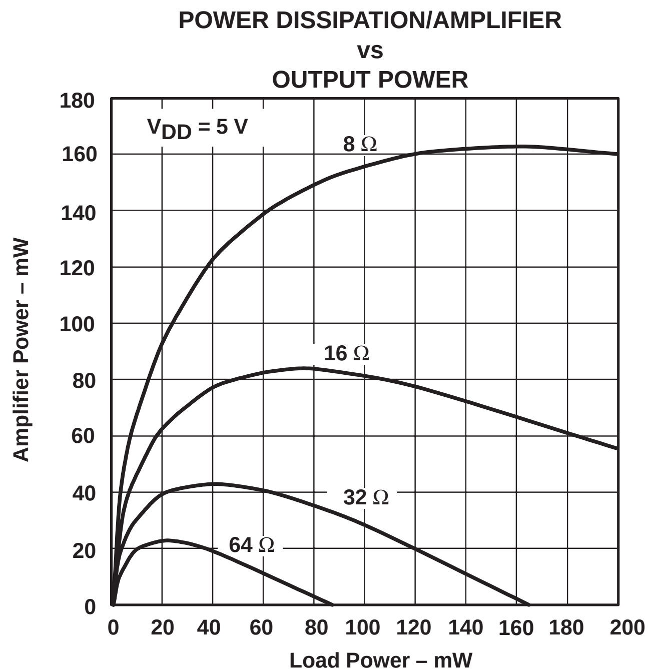


Figure 46

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for the TPA122 is set by resistors R_F and R_I according to equation 1.

$$\text{Gain} = -\left(\frac{R_F}{R_I}\right) \quad (1)$$

Given that the TPA122 is a MOS amplifier, the input impedance is very high. Consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 2.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \quad (2)$$

As an example, consider an input resistance of 20 kΩ and a feedback resistor of 20 kΩ. The gain of the amplifier would be –1 and the effective impedance at the inverting terminal would be 10 kΩ, which is within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F. This, in effect, creates a low-pass filter network with the cutoff frequency defined in equation 3.

$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \quad (3)$$

For example, if R_F is 100 kΩ and C_F is 5 pF then $f_{co(lowpass)}$ is 318 kHz, which is well outside the audio range.

input capacitor, C_I

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 4.

$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \quad (4)$$

The value of C_I is important to consider, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as equation 5.

$$C_I = \frac{1}{2\pi R_I f_{co(highpass)}} \quad (5)$$

In this example, C_I is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (> 10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, C_S

The TPA122 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so slow it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 160-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 6 should be maintained.

$$\frac{1}{\left(C_B \times 160\ \text{k}\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \qquad (6)$$

As an example, consider a circuit where C_B is 1 µF, C_I is 1 µF, and R_I is 20 kΩ. Inserting these values into the equation 9 results in:

$$6.25 \le 50$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 7.

$$f_{(\text{out high})} = \frac{1}{2\pi R_L C_C} \qquad (7)$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 68 µF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

APPLICATION INFORMATION

Table 1. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
32 Ω	68 µF	73 Hz
10,000 Ω	68 µF	0.23 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{\left(C_B \times 160\ \text{k}\Omega\right)} \leq \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \qquad (8)$$

output pull-down resistor, R_C + R_O

Placing a 100-Ω resistor, R_C, from the output side of the coupling capacitor to ground insures the coupling capacitor, C_C, is charged before a plug is inserted into the jack. Without this resistor, the coupling capacitor would charge rapidly upon insertion of a plug, leading to an audible pop in the headphones.

Placing a 20-kΩ resistor, R_O, from the output of the IC to ground insures that the coupling capacitor fully discharges at power down. If the supply is rapidly cycled without this capacitor, a small pop may be audible in 10-kΩ loads.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

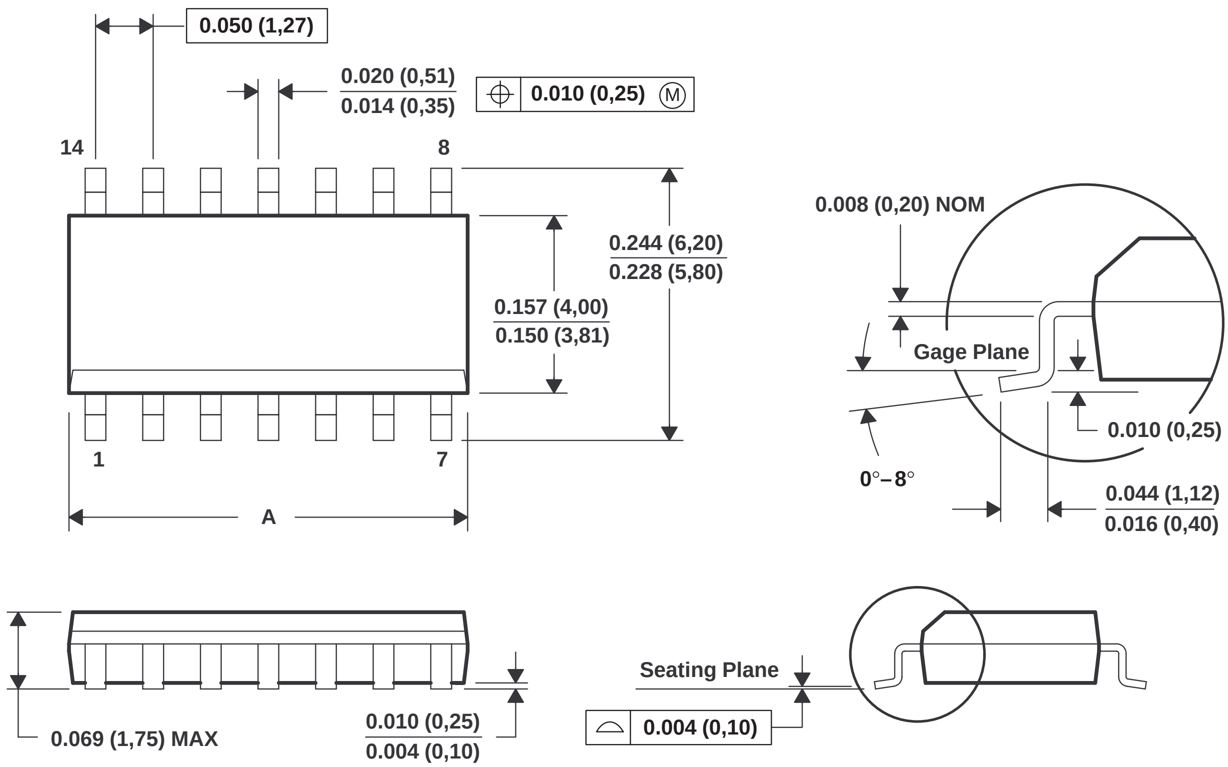
5-V versus 3.3-V operation

The TPA122 was designed for operation over a supply range of 2.7 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation since these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 3.5 mA (typical) to 2.5 mA (typical). The most important consideration is that of output power. Each amplifier in the TPA122 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion begins to become significant.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



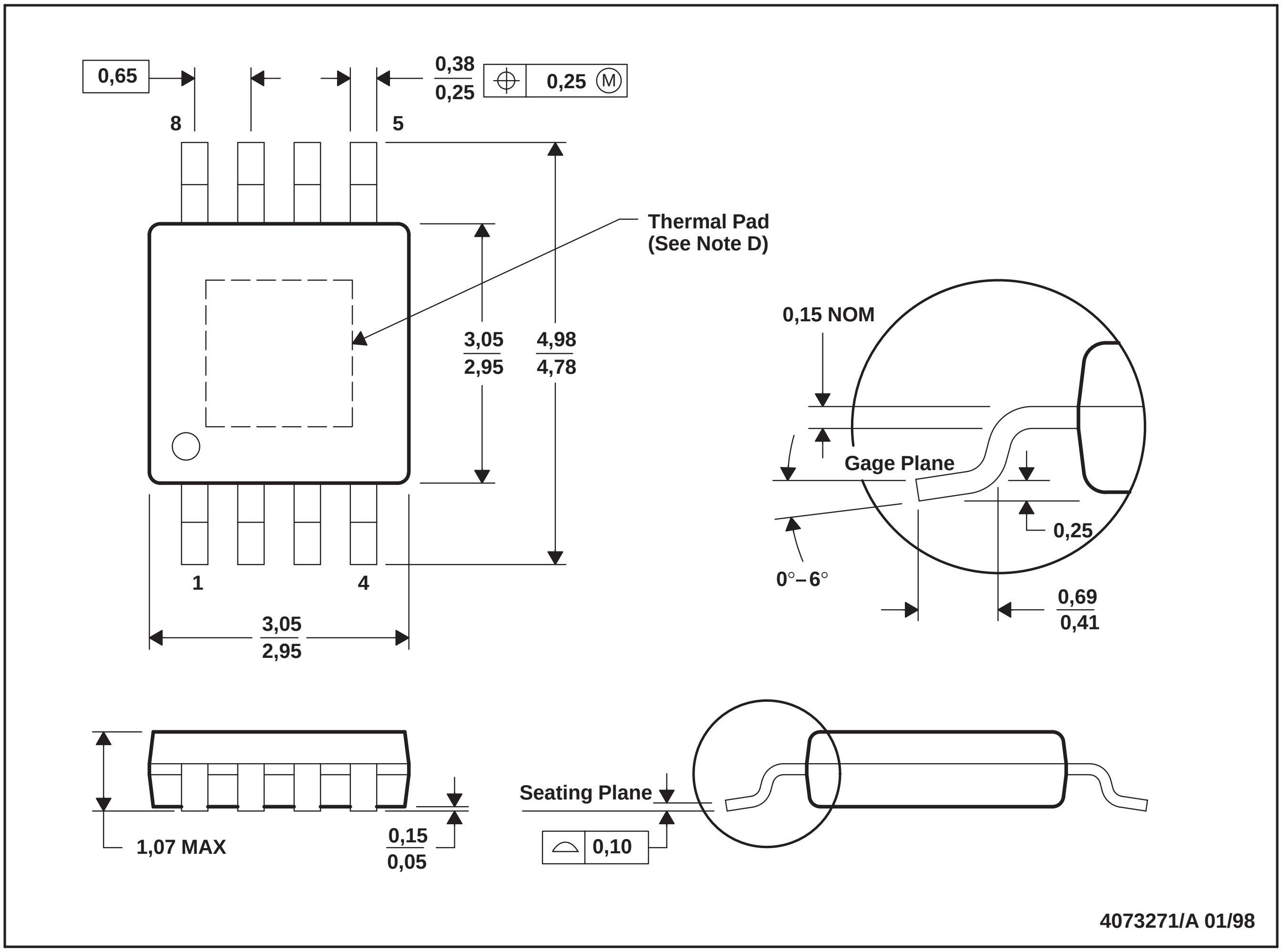
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads. The dimension of the thermal pad is 1.4 mm (height as illustrated) × 1.8 mm (width as illustrated) (maximum). The pad is centered on the bottom of the package.
E. Falls within JEDEC MO-187

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