- **ADSL Differential Receiver**
- **Preamp Features**
  - **Low Voltage Noise . . . 2nV/√Hz**
  - **Accessible Output Pin for External Filtering**
  - **Voltage Feedback, G_{min} = –1, 2**
- **PGA Features**
  - **Digitally Programmable Gain**
  - **Constant –3 dB Bandwidth**
  - **–22 dB to 20 dB Gain/Attenuation Range**
  - **6 dB Step Resolution**
  - **Output Clamp Protection**
- **Separate Low Noise Preamp and PGA Stages**
- **High Speed**
  - **70-MHz Bandwidth (–3 dB)**
  - **200 V/μs Slew Rate**
- **Shutdown Control**
- **Wide Supply Range ±4.5 V to ±16 V**
- **PowerPAD™ Package for Enhanced Thermal Performance**

description

The THS7002 is high-speed programmable-gain amplifier, ideal for applications as an ADSL receiver for both central office and remote terminal, where line impedance can often vary depending on line conditions. Each channel on this device consists of a separate low-noise input preamp and a programmable gain amplifier (PGA). The preamp is a voltage-feedback amplifier offering a low 2-nV/√Hz voltage noise. The output pin of the preamp is accessible so that filters can be easily added to the amplifier.

The 3-bit digitally controlled PGA provides a –22-dB to 20-dB attenuation/gain range with a 6-dB step resolution. In addition, the PGA provides both high and low output clamp protection to prevent the output signal from swinging outside the common-mode input range of an analog-to-digital converter. Both the preamp and the PGA provide a wide 70-MHz (–3 dB) bandwidth, with the PGA bandwidth remaining relatively constant over the entire gain/attenuation range. The THS7002 also provides independent shutdown control for power conservation and multiplexing. This device operates over a wide ±4.5-V to ±16-V supply voltage range.

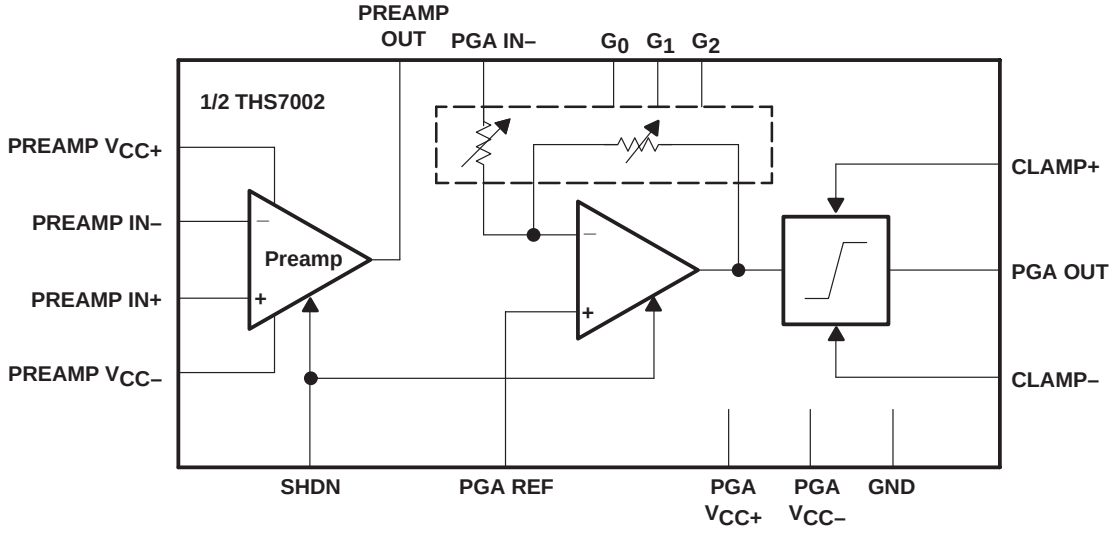


Figure 1. One Channel of the THS7002

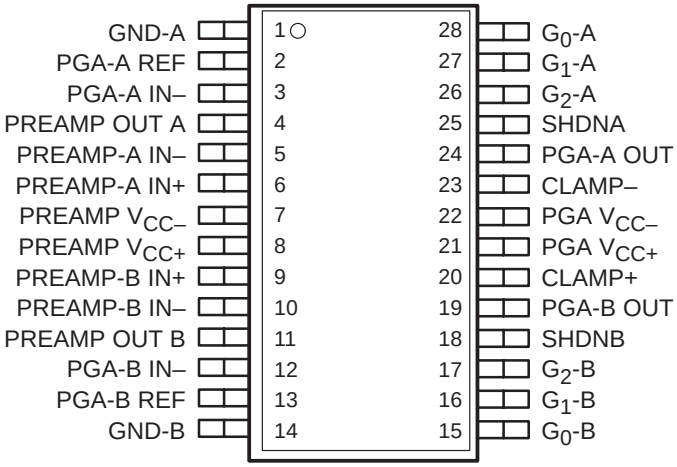
CAUTION: The THS7002 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

THS7002
PWP PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	PowerPAD PLASTIC TSSOP (PWP)
0°C to 70°C	THS7002CPWP
–40°C to 85°C	THS7002IPWP

PRODUCT PREVIEW

block diagram

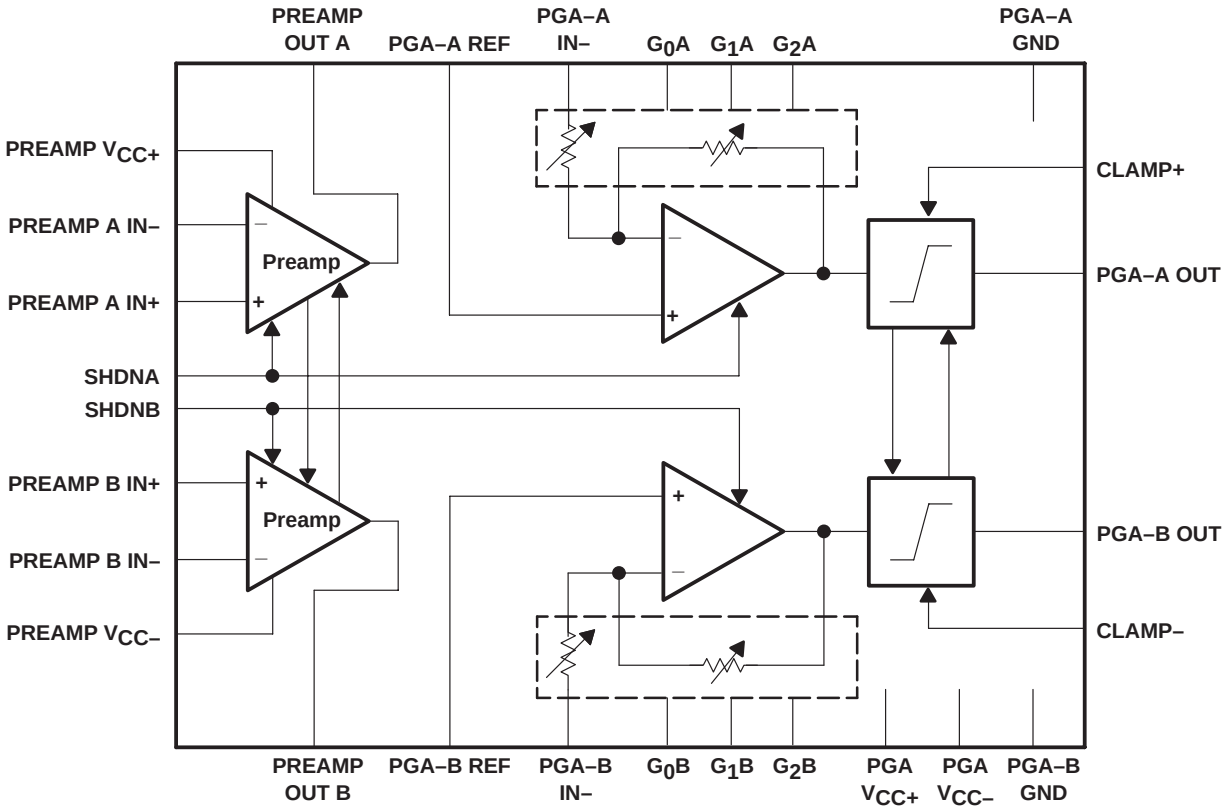


Figure 2. THS7002 Dual Channel PGA

input preamp

To achieve the minimum input equivalent noise, the input preamp is configured as a classic voltage feedback amplifier with a minimum gain of 2 or –1. The output of the preamp is accessible, allowing for adjustment of gain using external resistors and for external filtering between the preamp and the PGA.

programmable gain amplifier (PGA)

The PGA is an inverting, programmable gain amplifier. The gain is digitally programmable using three control bits (TTL-compatible terminals) that are encoded to provide eight distinct levels of gain/attenuation. Nominal gain/attenuation is shown in Table 1.

Table 1. Nominal Gain/Attenuation

G_2	G_1	G_0	PGA GAIN (dB)
0	0	0	–22
0	0	1	–16
0	1	0	–10
0	1	1	–4
1	0	0	2
1	0	1	8
1	1	0	14
1	1	1	20

PRODUCT PREVIEW

output clamping

Output clamping for both upper (VH) and lower (VL) levels for the PGAs is provided. There is only one terminal for the positive output clamp and one for the negative output clamp for both channels.

shutdown control

The SHDN terminals allow for powering down the internal circuitry for power conservation or for multiplexing. Separate shutdown controls are available for each channel. The control levels are TTL compatible.

absolute maximum ratings over operating free-air temperature (see Notes 1 and 2)†

Supply voltage, V_{CC} . . . . . ±16.5 V
Input voltage, V_I . . . . . $\pm V_{CC}$
Output current, I_O (preamp) (see Note 1) . . . . . 150 mA
I_O (PGA) (see Note 1) . . . . . 50 mA
Differential input voltage, V_{ID} . . . . . ±4 V
Total continuous power dissipation at (or below) T_A = 25°C (see Note 2) . . . . . 4.48 W
Operating free-air temperature, T_A . . . . . –40°C to 85°C
Storage temperature, T_{stg} . . . . . –65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The THS7002 incorporates a PowerPAD on the underside of the chip. The PowerPAD acts as a heatsink and must be connected to a thermal dissipation plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which could permanently damage the device. See the *Thermal Information* section of this document for more information about PowerPAD technology.
2. For operation above T_A = 25°C, derate linearly to 2.33 W at the rate of 35.9 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Preamp supply voltage, V_{CC+} and $V_{CC–}$	Split supply	±4.5		±16	V
PGA supply voltage, V_{CC+} and $V_{CC–}$	Split supply	±4.5‡		±16	V
Operating free-air temperature, T_A		–40		85	°C

‡ PGA minimum supply voltage **must be** less than or equal to preamp supply voltage.

PRODUCT PREVIEW

preamp electrical characteristics, G = 2, T_A = 25°C, R_L = 150 Ω, (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Split supply		±4.5		±16.5	V
V_{OM}	Maximum output voltage swing	R_L = 1 kΩ	V_{CC} = ±5 V	±3.4	±3.8		V
			V_{CC} = ±15 V	±13	±13.5		
		R_L = 150 kΩ	V_{CC} = ±5 V	±2.9	±3.3		
			V_{CC} = ±15 V	±12	±12.6		
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1.5	6	mV
			T_A = full range			8	
	Input offset voltage drift				10		µV/°C
V_{ICR}	Common-mode input voltage range	V_{CC} = ±5 V		3.6 –3	4.4 –3.8		V
		V_{CC} = ±15 V		13.5 –13.2	14.8 –14.2		
I_O	Output current (see Note 3)	R_L = 150 Ω	V_{CC} = ±5 V		85		mA
			V_{CC} = ±15 V	80	95		
I_{OC}	Short-circuit output current (see Note 3)	V_{CC} = ±15 V	R_L = 20 Ω		125		mA
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		3	6	µA
			T_A = full range			8	
I_{IO}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		30	175	nA
			T_A = full range			400	
	Input offset current drift				0.3		nA/°C
CMRR	Common-mode rejection ratio	V_{CC} = ±5 V, V_{IC} = ±2.5 V	T_A = 25°C	85	95		dB
			T_A = full range	80			
		V_{CC} = ±15 V, V_{IC} = ±12 V	T_A = 25°C	85	95		
			T_A = full range	80			
	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	85	95		dB
			T_A = full range	80			
R_I	Input resistance				1		MΩ
C_I	Input capacitance				1.2		pF
R_O	Output resistance	Open loop			12		Ω
	Channel-to-channel crosstalk	V_{CC} = ±5 V or ±15 V, f = 1 MHz, V_O = 200 mV		60	70		dB
I_{CC}	Quiescent current (per channel)	V_{CC} = ±5 V	T_A = 25°C		6	8	mA
			T_A = full range			9	
		V_{CC} = ±15 V	T_A = 25°C		7	9	
			T_A = full range			10	

† Full range for the THS7002C is 0°C to 70°C. Full range for the THS7002I is –40°C to 85°C.

NOTE 3: A heatsink may be required to keep the junction temperature below absoulte maximum when an output is heavily loaded or shorted. (See absolute maximum ratings and thermal information section.)

PRODUCT PREVIEW

preamp operating characteristics, G = 2, T_A = 25°C, R_L = 150 Ω, (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
SR	Slew rate (see Note 4)	G = –1	V_O = ±2 V, V_{CC} = ±5 V		175		V/µs
			V_O = ±10 V, V_{CC} = ±15 V		200		
t_s	Settling time to 0.1%	G = –1, V_I = 0 V to 2 V Step	V_{CC} = ±5 V		50		ns
		G = –1, 0 V to 10 V Step	V_{CC} = ±15 V		60		
	Settling time to 0.01%	G = –1, 0 V to 10 V Step	V_{CC} = ±15 V		85		ns
THD	Total harmonic distortion	V_{CC} = ±15 V, V_O = 1 $V_{O(PP)}$	f_c = 1 MHz,		–84		dBc
V_n	Input noise voltage	V_{CC} = ±5 V or ±15 V,	f = 10 kHz		2		nV/√Hz
I_n	Input noise current	V_{CC} = ±5 V or ±15 V,	f = 10 kHz		1.5		pA/√Hz
BW	Small-signal bandwidth (–3 dB)	G = 2	V_{CC} = ±5 V		60		MHz
			V_{CC} = ±15 V		70		
	Bandwidth for 0.1 dB flatness	G = 2	V_{CC} = ±5 V		15		MHz
			V_{CC} = ±15 V		20		
	Full power bandwidth (see Note 5)	V_{CC} = ±5 V,	V_O = 5 $V_{O(PP)}$		11		MHz
		V_{CC} = ±15 V,	V_O = 20 $V_{O(PP)}$		3.2		
A_D	Differential gain error	G = 2, ±100 IRE, NTSC	V_{CC} = ±5 V		0.02%		
			V_{CC} = ±15 V		0.06%		
ϕ_D	Differential phase error	G = 2, ±100 IRE, NTSC	V_{CC} = ±5 V		0.10°		
			V_{CC} = ±15 V		0.20°		
	Open loop gain	V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 500 Ω	T_A = 25°C	15	35		V/mV
			T_A = full range	10			
		V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	18	45		
			T_A = full range	12			

† Full range for the THS7002C is 0°C to 70°C. Full range for the THS7002I is –40°C to 85°C.

NOTES: 4. Slew rate is measured from an output level range of 25% to 75%.
5. Full power bandwidth = slew rate/2π $V_{(PP)}$.

shutdown characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{O(OFF)}$	Output current, disabled	V_{CC} = ±5 V or ±15 V,	$V_{I(SHDN)}$ = 2.5 V		10	20	µA
$V_{IH(SHDN)}$	Shutdown voltage for power-up	V_{CC} = ±5 V or ±15 V,	Relative to GND			0.8	V
$V_{IL(SHDN)}$	Shutdown voltage for power-down			2			V
$I_{IH(SHDN)}$	Shutdown input current high	V_{CC} = ±5 V or ±15 V,	$V_{I(SHDN)}$ = 5 V		200	400	µA
$I_{IL(SHDN)}$	Shutdown input current low		$V_{I(SHDN)}$ = 0.5 V		5	15	µA

PRODUCT PREVIEW

PGA electrical characteristics, T_A = 25°C, Gain = 2 dB, R_L = 1 kΩ, (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	Split supply		±4.5‡		±16.5	V
V_{OM}	Maximum output voltage swing	R_L = 2 kΩ	V_{CC} = ±5 V	±3.4	±3.8		V
			V_{CC} = ±15 V	±13	±13.5		
		R_L = 1 kΩ	V_{CC} = ±5 V	±2.9	±3.3		
			V_{CC} = ±15 V	±12	±13.5		
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		3	8	mV
			T_A = full range			10	
	Input offset voltage drift				10		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		3	6	µA
			T_A = full range			8	
I_{IO}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		30	175	nA
			T_A = full range			400	
	Input offset current drift				0.3		nA/°C
CMMR	Common-mode rejection ratio	V_{CC} = ±5 V, V_{IC} = ±2.5 V	T_A = 25°C	75	85		dB
			T_A = full range	70			
		V_{CC} = ±15 V, V_{IC} = ±10 V	T_A = 25°C	85	95		
			T_A = full range	80			
I_O	Output current	R_L = 150 Ω	V_{CC} = ±5 V	13	23		mA
			V_{CC} = ±15 V	15	25		
I_{OS}	Short-circuit output current	V_{CC} = ±15 V,	R_L = 5 Ω		55		mA
	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	78	90		dB
			T_A = full range	73			
R_I	Input resistance	Gain = 20 dB			0.27		kΩ
		Gain = –22 dB			3		
C_I	Input capacitance				1.5		pF
R_O	dc output resistance				0.05		Ω
I_{CC}	Quiescent current (per channel)	V_{CC} = ±5 V	T_A = 25°C		8	11	mA
			T_A = full range			12	
		V_{CC} = ±15 V	T_A = 25°C		9	12	
			T_A = full range			13	

† Full range for the THS7002C is 0°C to 70°C. Full range for the THS7002I is –40°C to 85°C.
‡ PGA minimum supply voltage **must be** less than or equal to preamp supply voltage.

PRODUCT PREVIEW

output limiting characteristics

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Clamp accuracy	V_{CC} = ±15 V, V_I = ±10 V, Gain = 2 dB	VH = 10 V, VL = –10 V,	T_A = 25°C		±150	±200	mV
			T_A = full range			±225	
	V_{CC} = ±5 V, V_I = ±2.5 V, Gain = 2 dB	VH = 2 V, VL = –2 V,	T_A = 25°C		±100	±200	
			T_A = full range			±225	
Clamp overshoot	V_{CC} = ±15 V, V_I = ±10 V,	VH = 10 V, t_r and t_f = 1 ns	V_L = 10 V,		10%		
	V_{CC} = ±5 V, V_I = ±2.5 V,	VH = 2 V, t_r and t_f = 1 ns	V_L = 2 V,		7.5%		
Overdrive recovery time	V_{CC} = ±15 V, V_I = ±10 V	VH = 10 V,	V_L = 10 V,		5		nS
	V_{CC} = ±5 V, V_I = ±2.5 V	VH = 2 V,	V_L = 2 V,		4		
Negative clamp range	V_{CC} = ±5 V				–5 to 2		V
	V_{CC} = ±15 V				–15 to 2		
Positive clamp range	V_{CC} = ±5 V				–2 to 5		V
	V_{CC} = ±15 V				–2 to 15		
Clamp input bias current	V_{CC} = ±5 V, ±15 V		T_A = full range		50		µA
					75		

† Full range for the THS7002C is 0°C to 70°C. Full range for the THS7002I is –40°C to 85°C.

PGA electrical characteristics, T_A = 25°C, Gain = 2 dB, R_L = 1 kΩ, (unless otherwise noted) (continued)

digital gain characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	Relative to GND	2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input current	V_{IH} = 5 V		2	20	µA
I_{IL}	Low-level input current	V_{IL} = 0.5 V		1	10	µA

PRODUCT PREVIEW

PGA operating characteristics, T_A = 25°C, Gain = 2 dB, R_L = 1 kΩ, (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
SR	Slew rate (see Note 4)	V_{CC} = ±5 V,	V_O = ±2 V		175		V/µs
		V_{CC} = ±15 V,	V_O = ±10 V		200		
t_s	Settling time to 0.1%	0 V to 10 V Step	V_{CC} = ±15 V		60		ns
		V_I = 0 V to 10 V Step	V_{CC} = ±5 V		50		
t_s	Settling time to 0.01%	0 V to 10 V Step	V_{CC} = ±15 V		85		ns
THD	Total harmonic distortion	V_{CC} = ±15 V, f_C = 1 MHz	$V_{O(PP)}$= 2 V,		–80		dBc
BW	Small-signal bandwidth (–3 dB)	Gain = 20 dB	V_{CC} = ±15 V		60		MHz
			V_{CC} = ±5 V		50		
		Gain = 2 dB	V_{CC} = ±15 V		65		
			V_{CC} = ±5 V		55		
		Gain = –22 dB	V_{CC} = ±15 V		70		
			V_{CC} = ±5 V		60		
	Bandwidth for 0.1 dB flatness	Gain = 2 dB	V_{CC} = ±15 V		15		MHz
			V_{CC} = ±5 V		12		
	Full power bandwidth (see Note 5)	V_O = 5 $V_{O(PP)}$,	V_{CC} = ±5 V		11		MHz
		V_O = 20 $V_{O(PP)}$,	V_{CC} = ±15 V		3.2		
A_D	Differential gain error	G = 8 dB, ±100 IRE, NTSC	V_{CC} = ±5 V		0.02%		
			V_{CC} = ±15 V		0.06%		
ϕ_D	Differential phase error	G = 8 dB, ±100 IRE, NTSC	V_{CC} = ±15 V		0.20°		
			V_{CC} = ±5 V		0.10°		
	Open loop gain (see Note 6)	Gain = –22 dB to 20 dB, All 8 steps, V_{CC} = ±5 V or ±15 V	T_A = 25°C	–4%	0%	4%	
			T_A = full range	–6%		6%	
	dc nonlinearity	V_I = –2 to 2 V	V_{CC} = ±5 V		0.05%		
		V_I = –8 to 8 V	V_{CC} = ±15 V		0.05%		
V_n	Input noise voltage	V_{CC} = ±5 V or ±15 V, Gain = 20 dB	f = 10 kHz,		10		nV/√Hz
I_n	Input noise current	V_{CC} = ±5 V or ±15 V, Gain = 20 dB	f = 10 kHz,		1.5		pA/√Hz

† Full range for the THS7002C is 0°C to 70°C. Full range for the THS7002I is –40°C to 85°C.

NOTES: 4. Slew rate is measured from an output level range of 25% to 75%.
5. Full power bandwidth = slew rate/2π V_{PEAK}
6. Specified as –100 × (output voltage – (input voltage × gain))/(input voltage × gain)

shutdown characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dis}	Disable time (see Note 7)			100		ns
t_{en}	Enable time (see Note 7)			50		ns

NOTE 7: Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.

digital gain characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Gain change delay (see Note 8)			1		µs

NOTE 8: Gain change delay is the time needed to reach 90% of its final gain value.

PRODUCT PREVIEW

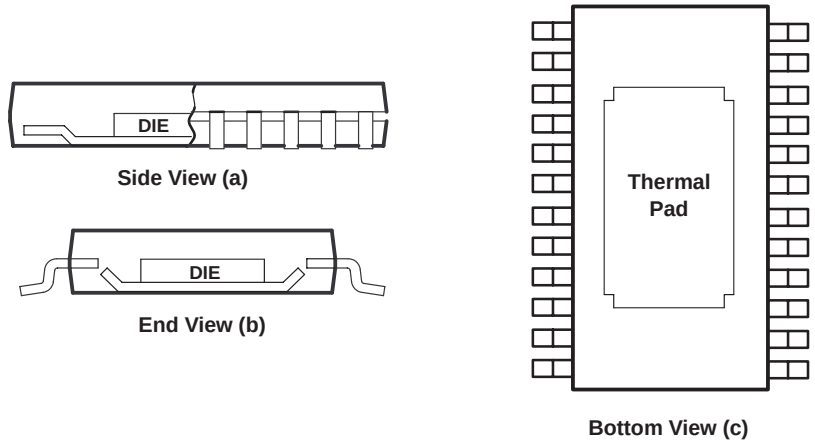
APPLICATION INFORMATION

thermal information

The THS7002 is supplied in a thermally-enhanced PWP package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 3(a) and Figure 3(b)]. This arrangement exposes the lead frame as a thermal pad on the underside of the package [see Figure 3(c)]. Because this pad has direct contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area requirement and ease of assembly of surface mount with the heretofore awkward mechanical methods of heatsinking.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

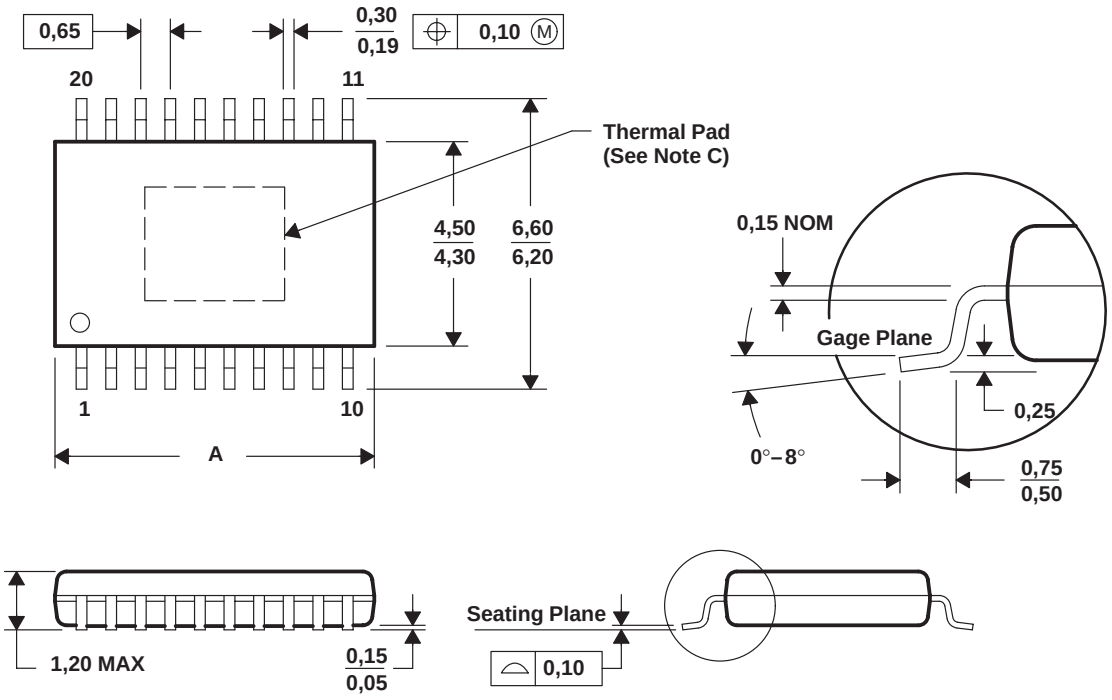
Figure 3. Views of Thermally Enhanced PWP Package

PRODUCT PREVIEW

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

20-PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/E 03/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This solderable pad is electrically and thermally connected to the backside of the die and possibly selected leads. The maximum pad size on the printed circuit board should be equal to the package body size – 2,0 mm.

PowerPAD is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.