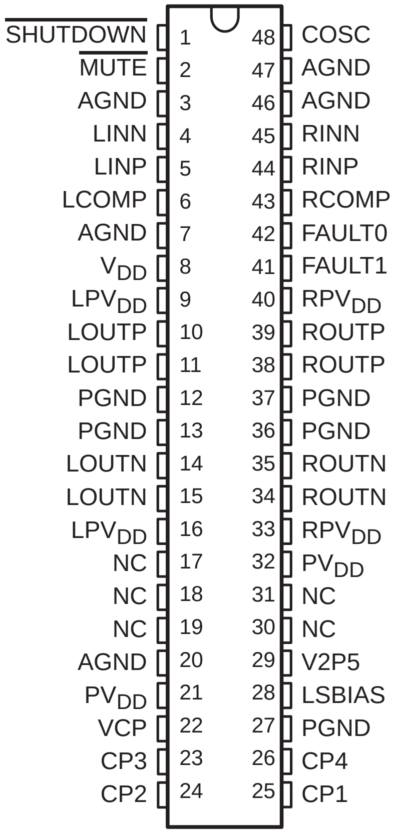
- **Extremely Efficient Class-D Stereo Operation**
- **Drives L and R Channels**
- **2-W BTL Output into 4 Ω**
- **5-W Peak Music Power**
- **Fully Specified for 5-V Operation**
- **Low Quiescent Current**
- **Shutdown Control**
- **Thermally-Enhanced PowerPAD™ Surface Mount Packaging**
- **Thermal and Under-Voltage Protection**

DCA PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPA005D02 is a monolithic power IC stereo audio amplifier. It operates in extremely efficient Class-D operation, using the high switching speed of power DMOS transistors. These transistors replicate the analog signal through high-frequency switching of the output state. This allows the TPA005D02 to be configured as a bridge-tied load (BTL) amplifier

When configured as a BTL amplifier, the TPA005D02 is capable of delivering up to 2 W of continuous average power into a 4-Ω load at 0.5% THD+N from a 5-V power supply in the high fidelity range (20 Hz to 20 kHz).

A BTL configuration eliminates the need for external coupling capacitors on the output. A chip-level shutdown control limits total supply current to 400 μA. This makes the device ideal for battery-powered applications.

Protection circuitry increases device reliability: thermal and under-voltage shutdown, with two status feedback terminals for use when any error condition is encountered.

The high switching frequency of the TPA005D02 allows the output filter to consist of three small capacitors and two small inductors per channel. The high switching frequency also allows for good THD+N performance.

The TPA005D02 is offered in the thermally enhanced 48-pin PowerPAD TSSOP surface-mount package (designator DCA).

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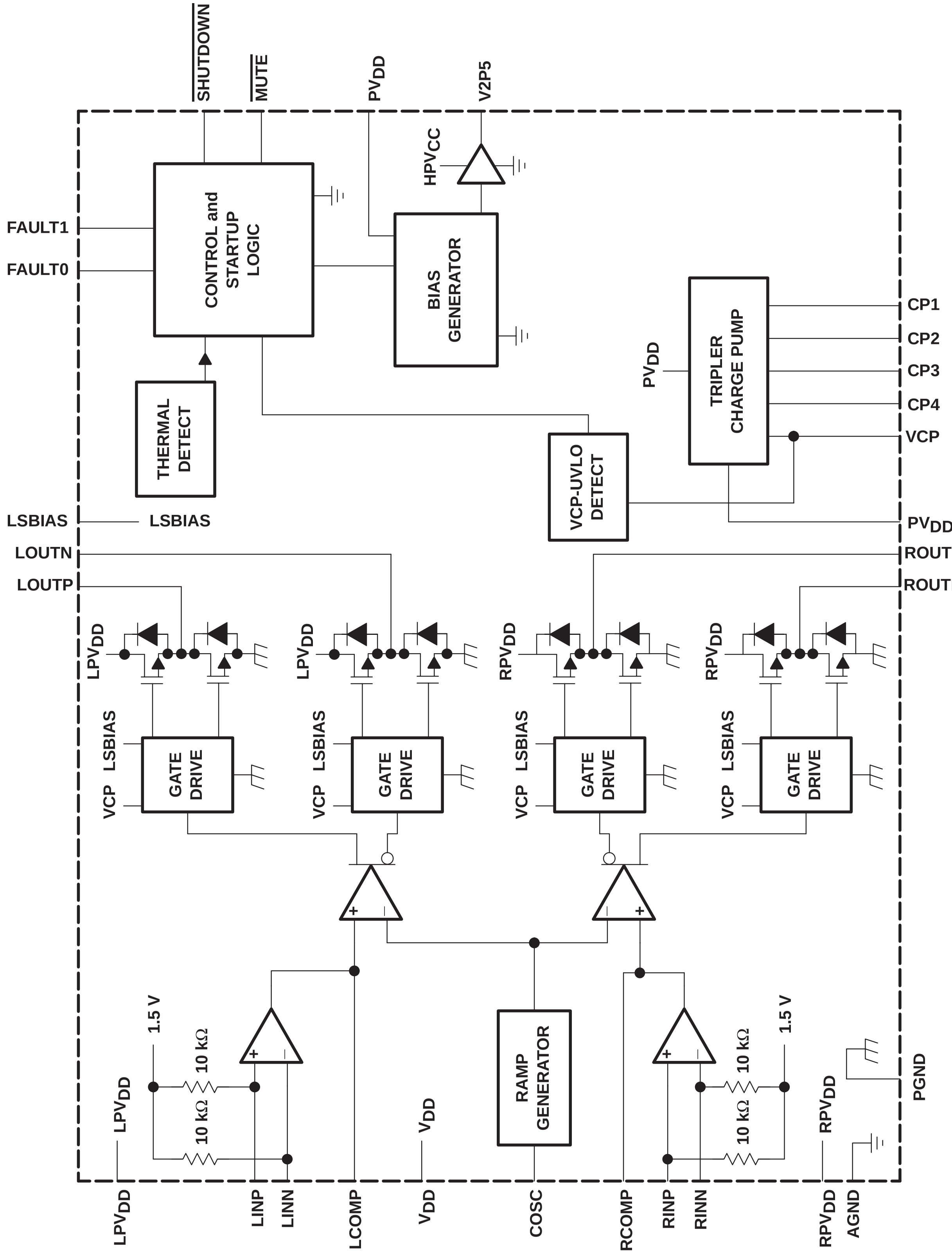
TEXAS INSTRUMENTS

schematic



NOTE A: LPV_{DD}, RPV_{DD}, V_{DD}, and PV_{DD} are externally connected. AGND and PGND are externally connected.

Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	3, 7, 20, 46, 47	Analog ground for analog sections
COSC	48	Capacitor I/O for ramp generator. Adjust the capacitor size to change the switching frequency.
CP1	25	First diode node for charge pump
CP2	24	First inverter switching node for charge pump
CP3	23	Second diode node for charge pump
CP4	26	Second inverter switching node for charge pump
FAULT0	42	Logic level fault0 output signal. Lower order bit of the two fault signals with open drain output.
FAULT1	41	Logic level fault1 output signal. Higher order bit of the two fault signals with open drain output.
LCOMP	6	Compensation capacitor terminal for left-channel Class-D amplifier
LINN	4	Class-D left-channel negative input
LINP	5	Class-D left-channel positive input
LOUTN	14, 15	Class-D amplifier left-channel negative output of H-bridge
LOUTP	10, 11	Class-D amplifier left-channel positive output of H-bridge
LPV$_{DD}$	9, 16	Class-D amplifier left-channel power supply
LSBIAS	28	Level-shifter power supply, to be tied to VCP
$\overline{\text{MUTE}}$	2	Active-low logic-level mute input signal. When $\overline{\text{MUTE}}$ is held low, the selected amplifier is muted. When $\overline{\text{MUTE}}$ is held high, the device operates normally. When the Class-D amplifier is muted, the low-side output transistors are turned on, shorting the load to ground.
NC	17, 18, 19, 30, 31	No internal connection
PGND	12, 13	Power ground for left-channel H–bridge only
PGND	27	Power ground for charge pump only
PGND	36, 37	Power ground for right-channel H-bridge only
PV$_{DD}$	21, 32	V$_{DD}$ supply for charge-pump and internal logic circuitry
RCOMP	43	Compensation capacitor terminal for right-channel Class-D amplifier
RINN	45	Class-D right-channel negative input
RINP	44	Class-D right-channel positive input
RPV$_{DD}$	33, 40	Class-D amplifier right-channel power supply
ROUTN	34, 35	Class-D amplifier right-channel negative output of H-bridge
ROUTP	38, 39	Class-D amplifier right-channel positive output of H-bridge
$\overline{\text{SHUTDOWN}}$	1	Active-low logic-level shutdown input signal. When $\overline{\text{SHUTDOWN}}$ is held low, the device goes into shutdown mode. When $\overline{\text{SHUTDOWN}}$ is held at logic high, the device operates normally.
V2P5	29	2.5V internal reference bypass
VCP	22	Storage capacitor terminal for charge pump
V$_{DD}$	8	V$_{DD}$ bias supply for analog circuitry. This terminal needs to be well filtered to prevent degrading the device performance.

Class-D amplifier faults

Table 1. Amplifier Fault Table

FAULT 0[†]	FAULT 1[†]	DESCRIPTION
1	1	No fault — The device is operating normally.
1	0	Charge pump under-voltage lock-out (VCP-UV) fault — All low-side transistors are turned on, shorting the load to ground. Once the charge pump voltage is restored, normal operation resumes, but FAULT1 is still active. FAULT1 is cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.
0	0	Thermal fault — All the low-side transistors are turned on, shorting the load to ground. Once the junction temperature drops 20°C, normal operation resumes. But the FAULTx terminals are still set and are cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.

[†] These logic levels assume a pull up to PV_{DD} from the open-drain outputs.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP[†] (DCA)
–40°C to 125°C	TPA005D02DCA

[†] The DCA package is available in left-ended tape and reel. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA005D02DCAR).

absolute maximum ratings over operating free-air temperature range, T_C = 25°C (unless otherwise noted)[‡]

Supply voltage, V_{DD} (PV_{DD}, LPV_{DD}, RPV_{DD}, V_{DD}) . . . . 5.5 V
Bias voltage (LSBIAS) . . . . 12 V to 20 V
Input voltage, V_I ($\overline{\text{SHUTDOWN}}$, $\overline{\text{MUTE}}$, MODE) . . . . –0.3 V to 5.8 V
Output current, I_O (FAULT0, FAULT1), open drain terminated . . . . 1 mA
Charge pump voltage, V_{CP} . . . . PV_{DD} + 20 V
Continuous H-bridge output current . . . . 2 A
Pulsed H-Bridge output current, each output, I_{max} (see Note 1) . . . . 5 A
Continuous total power dissipation, T_C = 25°C . . . . 4.5 W[§]
Operating virtual junction temperature range, T_J . . . . –40°C to 150°C
Operating case temperature range, T_C . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[§] Thermal shutdown activates when T_J = 125°C.

NOTE 1: Pulse duration = 10 ms, duty cycle ≤ 2%

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$[¶] POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
DCA	5.6 W	44.8 mW/°C	3.6 W	2.9 W	1.1 W

[¶] Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, PV_{DD}, LPV_{DD}, RPV_{DD}, V_{DD}	4.5		5.5	V
High-level input voltage, V_{IH}	4.25			V
Low-level input voltage, V_{IL}			0.75	V
Audio inputs, LINN, LINP, RINN, RINP, HPLIN, HPRIN, differential input voltage			1	V_{RMS}
PWM frequency	100		500	kHZ

electrical characteristics, $V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 5$ V, $R_L = 4\ \Omega$, $T_C = 25°C$, See Figure 1 (resistive load) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSSR	Power supply rejection ratio	$V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 4.9$ V to 5.1 V		40		dB
I_{DD}	Supply current	No load or output filter		25	40	mA
$I_{DD(MUTE)}$	Supply current, mute mode	$\overline{\text{MUTE}} = 0$ V		10	15	mA
$I_{DD(S/D)}$	Supply current, shutdown mode	$\overline{\text{SHUTDOWN}} = 0$ V		400	2000	µA
I_{IH}	High-level input current	$V_{IH} = 5.3$ V			10	µA
I_{IL}	Low-level input current	$V_{IL} = -0.3$ V			–10	µA
$r_{DS(on)}$	Total static drain-to-source on-state resistance (low-side plus high-side FETs)	$I_D = 0.5$ A		620	750	mΩ
$r_{DS(on)}$	Matching		95%	99.5%		

operating characteristics, $V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 5$ V, $R_L = 4\ \Omega$, $T_C = 25°C$, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	RMS output power, THD = 0.5%, per channel			2		W
THD+N	Total harmonic distortion plus noise	$P_O = 1$ W, f = 1 kHz		0.2%		
	Efficiency	$R_L = 8\ \Omega$		80%		
A_V	Gain			24		dB
	Left/right channel gain matching			95%		
	Noise floor			60		dB
	Dynamic range			70		dB
	Crosstalk	f = 1 kHz		55		dB
	Frequency response bandwidth, post output filter, –3 dB		20		20,000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JP}$	Thermal resistance, junction-to-pad				10	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-pad†			22.3		°C/W

† Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

PARAMETER MEASUREMENT INFORMATION

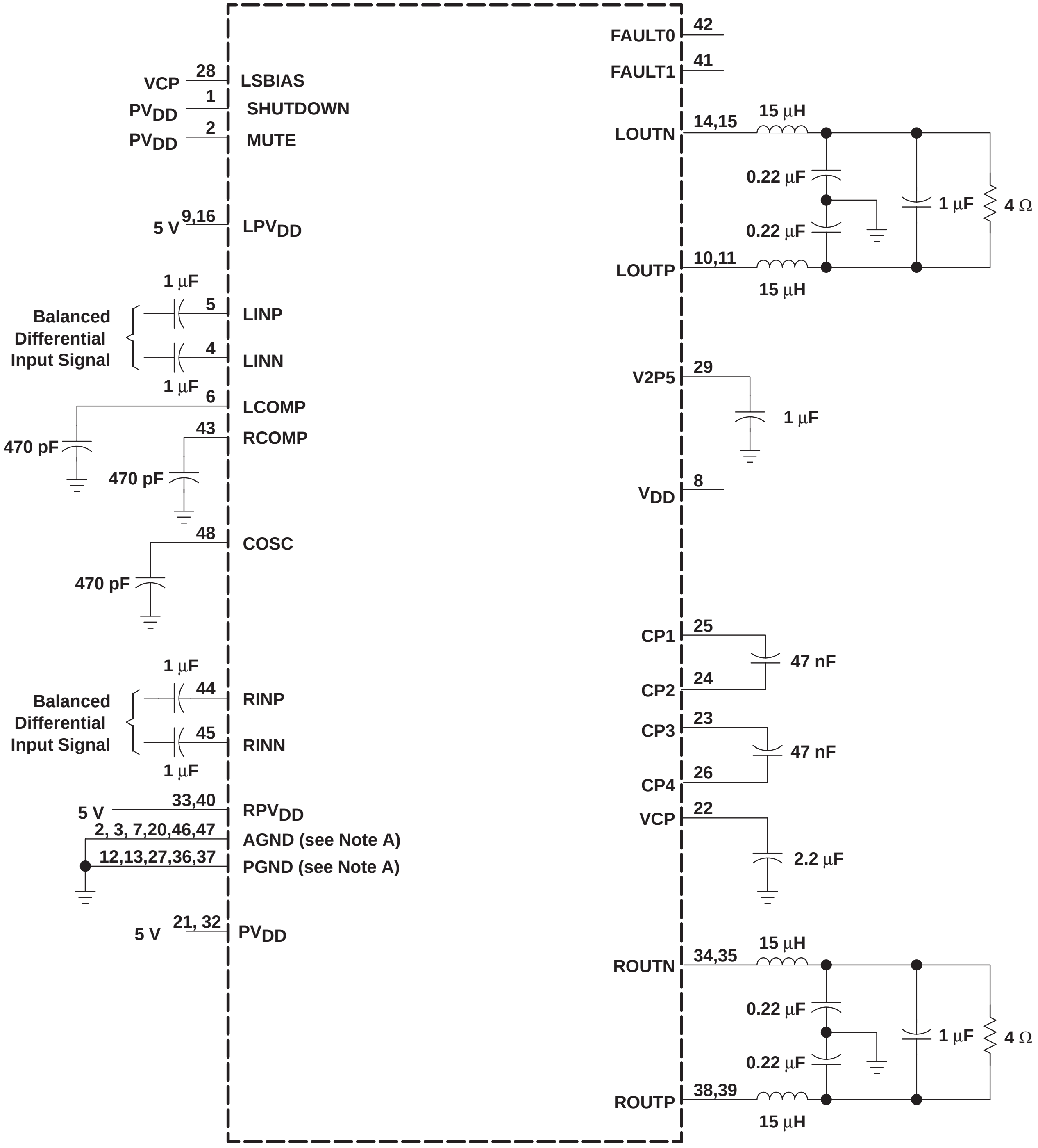


Figure 1. 5-V, 4-Ω Test Circuit

APPLICATION INFORMATION

class-D output filter design

The output filter attenuates the high switching frequency. A 2nd order Butterworth low-pass filter is chosen for its flat pass band, nice phase response, and it only requires an inductor and a capacitor. The normalized transfer for the Butterworth filter is shown in equation 1.

$$H(s) = \frac{1}{s^2 + \sqrt{2}\,s + 1} \tag{1}$$

The next step is to realize the circuit and develop a transfer function. The filter for a single-ended application is shown in Figure 2.

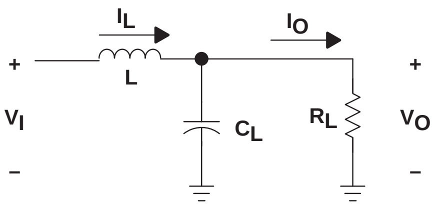


Figure 2. Single-Ended Class-D Output Filter

The transfer function is easily derived by using a voltage divider equation with the load voltage being a parallel combination of R_L and C_L. This transfer function is reduced in equation 2.

$$\frac{V_O(s)}{V_I(s)} = \frac{\frac{1}{LC_L}}{s^2 + \frac{1}{R_L C_L} \times s + \frac{1}{LC_L}} \tag{2}$$

The next step is to set the terms of the circuit transfer function equal to the terms of the normalized 2nd order Butterworth low-pass filter and solve for L and C_L in terms of R_L. This yields formulas 3 and 4.

$$C_L = \frac{1}{\sqrt{2} \times R_L} \tag{3}$$

$$L = \sqrt{2} \times R_L \tag{4}$$

These values will give a cut-off frequency at $\omega_0 = 1$ radian/second, which means that the components must be frequency scaled. To frequency scale, each component is divided by $\omega_0 = 2 \times \pi \times f_c$ and f_c is the desired cut-off frequency in Hertz.

$$C_{SE} = \frac{1}{\sqrt{2} \times P_L \times \omega 0} \tag{5}$$

$$L_{SE} = \frac{\sqrt{2} \times R_L}{\omega_o} \tag{6}$$

$$\omega_0 = 2 \times \pi \times f_c \tag{7}$$

Because the TPA005D02 is a bridged amplifier, this filter is needed at both the positive and negative output. This means that R_L must be split between each filter, so for a bridged application, R_L must be divided by 2 in the component calculations. One capacitor can be used in place of the two capacitors in the output filters if the capacitor is placed across R_L instead of from each side of R_L to ground. The resulting circuit can be seen in Figure 3.

APPLICATION INFORMATION

class-D output filter design (continued)

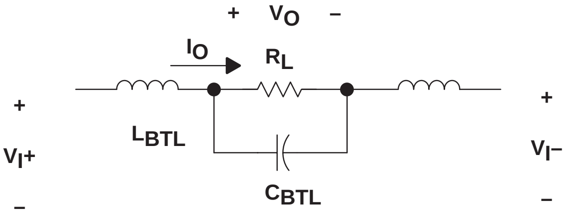


Figure 3. Low-Pass Filter for Bridged Application

The component equations adjusted for bridged amplifiers are shown in equations 8 and 9.

$$C_{BTL} = \frac{1}{\sqrt{2} \times R_L \times \omega_0} \tag{8}$$

$$L_{BTL} = \frac{\sqrt{2} \times R_L}{2 \times \omega_0} \tag{9}$$

To find component values, let $f_c = 30$ kHz, which yields $\omega_0 = 188495.6$ radians/second. If a 4-Ω speaker is used, let $R_L = 4\ \Omega$. This yields $L_{BTL} = 15\ \mu H$ and $C_{BTL} = 0.94\ \mu F$. Additional capacitors can be added from each side to R_L to ground to provide a high-frequency short to ground. These additional capacitors should be approximately 10% of $2C_{BTL}$. The resulting output filter is shown in Figure 4 with the components rounded to standard values.

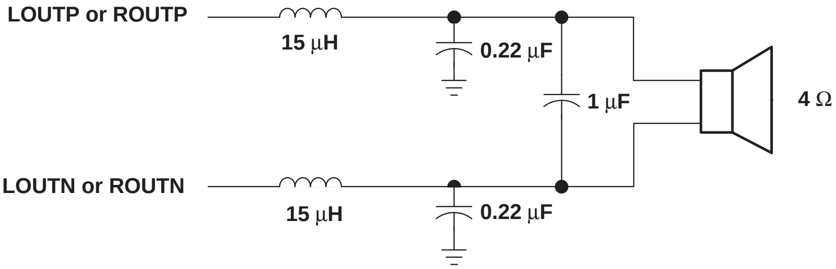


Figure 4. Resulting Bridged Output Filter

filter components

inductors

The output inductors are key elements in the performance of the class-D audio system. It is important that these inductors have a high enough current rating and a relatively constant inductance over frequency and temperature. If the inductor is not able to handle high current, the output can be greatly distorted at high power. Q shielded inductor may be required if the class-D amplifier is placed in an EMI sensitive system; however, the switching frequency is around 250 kHz, and should not be an issue in most systems.

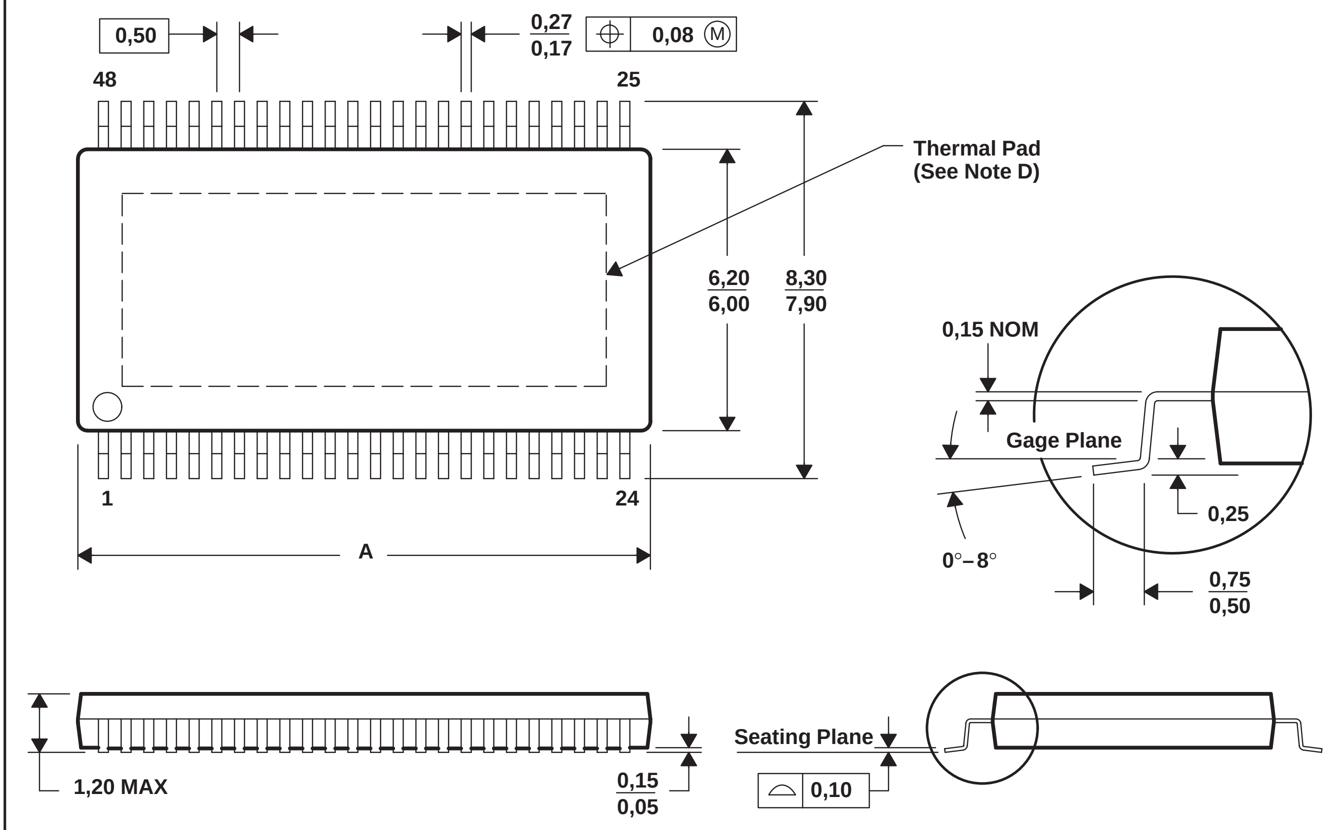
capacitors

Capacitors are key in attenuating the switching frequency and high frequency noise. It is better to use capacitors with lower equivalent-series-resistance (ESR) and equivalent-series-inductance (ESL). A higher ESL shifts the cut-off frequency. A higher ESR decreases the roll-off of the filter. Each of these parameter cause the switching frequency attenuation to be less. However, switching frequency attenuation is not a major issue for most audio applications because the human ear cannot hear sounds above 22 kHz and the switching frequency is at 250 kHz.

MECHANICAL DATA

DCA (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

48-PIN SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4073259/A 01/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly leads 14, 15, 36, and 37. The dimension of the thermal pad is 3.05 mm (height as illustrated × 6.35 mm (width as illustrated) (maximum). The pad is centered on the bottom of the package.
E. Falls within JEDEC MO-153

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