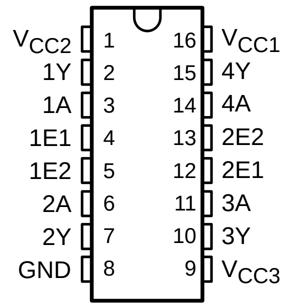
SN75374 QUADRUPLE MOSFET DRIVER

- **Quadruple Circuits Capable of Driving High-Capacitance Loads at High Speeds**
- **Output Supply Voltage Range From 5 V to 24 V**
- **Low Standby Power Dissipation**
- **V_{CC3} Supply Maximizes Output Source Voltage**

D OR N PACKAGE
(TOP VIEW)



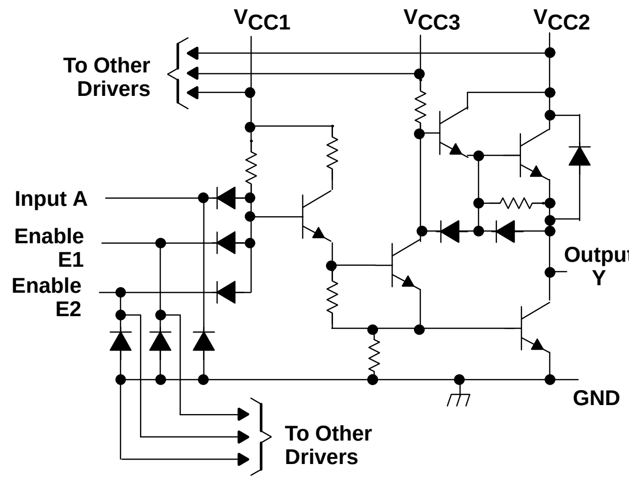
description

The SN75374 is a quadruple NAND interface circuit designed to drive power MOSFETs from TTL inputs. It provides the high current and voltage necessary to drive large capacitive loads at high speeds.

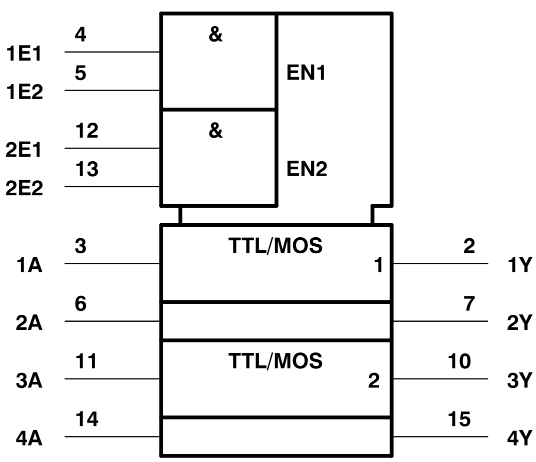
The outputs can be switched very close to the V_{CC2} supply rail when V_{CC3} is about 3 V higher than V_{CC2}. V_{CC3} can also be tied directly to V_{CC2} when the source voltage requirements are lower.

The SN75374 is characterized for operation from 0°C to 70°C.

schematic (each driver)



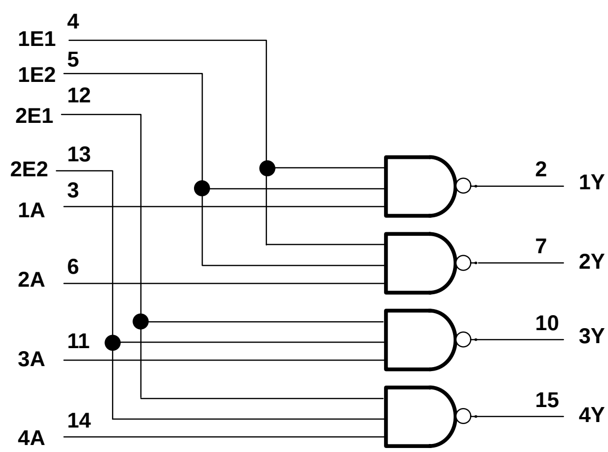
logic symbol†



(7–48)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . –0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . –0.5 V to 25 V
Supply voltage range of V_{CC3} . . . . –0.5 V to 30 V
Input voltage, V_I . . . . 5.5 V
Peak output current, I_I (t_w < 10 ms, duty cycle < 50%) . . . . 500 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
Supply voltage, V_{CC3}	V_{CC2}	24	28	V
Voltage difference between supply voltages: $V_{CC3} - V_{CC2}$	0	4	10	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			–10	mA
High-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3}, and operating free-air temperature (unless otherwise noted)

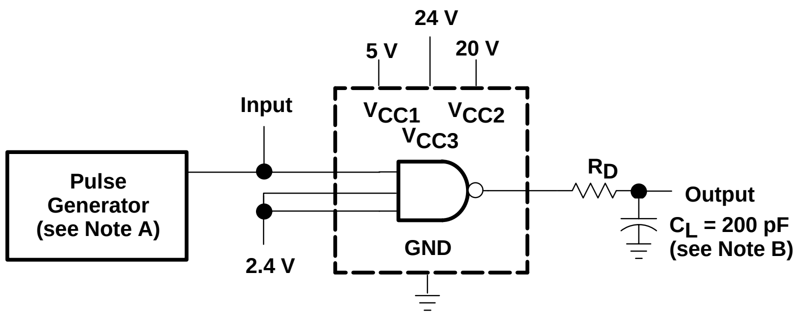
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -12$ mA			−1.5	V
V_{OH}	High-level output voltage		$V_{CC3} = V_{CC2} + 3$ V, $V_{IL} = 0.8$ V, $I_{OH} = -100$ µA	$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
			$V_{CC3} = V_{CC2} + 3$ V, $V_{IL} = 0.8$ V, $I_{OH} = -10$ mA	$V_{CC2}-1.3$	$V_{CC2}-0.9$		
			$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8$ V, $I_{OH} = -50$ µA	$V_{CC2}-1$	$V_{CC2}-0.7$		
			$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8$ V, $I_{OH} = -10$ mA	$V_{CC2}-2.5$	$V_{CC2}-1.8$		
V_{OL}	Low-level output voltage		$V_{IH} = 2$ V, $I_{OL} = 10$ mA		0.15	0.3	V
			$V_{CC2} = 15$ V to 28 V, $V_{IH} = 2$ V, $I_{OL} = 40$ mA		0.25	0.5	
V_F	Output clamp-diode forward voltage		$V_I = 0$, $I_F = 20$ mA			1.5	V
I_I	Input current at maximum input voltage		$V_I = 5.5$ V			1	mA
I_{IH}	High-level input current	Any A	$V_I = 2.4$ V			40	µA
		Any E				80	
I_{IL}	low-level input current	Any A	$V_I = 0.4$ V		−1	−1.6	mA
		Any E			−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high		$V_{CC1} = 5.25$ V, $V_{CC2} = 24$ V, $V_{CC3} = 28$ V, All inputs at 0 V, No load		4	8	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high				−2.2	0.25	
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high				2.2	3.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low		$V_{CC1} = 5.25$ V, $V_{CC2} = 24$ V, $V_{CC3} = 28$ V, All inputs at 5 V, No load		31	47	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low					2	
$I_{CC3(L)}$	Supply current from V_{CC1}, all outputs low				16	27	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high		$V_{CC1} = 5.25$ V, $V_{CC2} = 24$ V, $V_{CC3} = 24$ V, All inputs at 0 V, No load			0.25	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high					0.5	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition		$V_{CC1} = 0$, $V_{CC2} = 24$ V, $V_{CC3} = 24$ V, All inputs at 0 V, No load			0.25	mA
$I_{CC3(S)}$	Supply current from V_{CC3}, standby condition					0.5	

† All typical values are at $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $V_{CC3} = 24$ V, and $T_A = 25°C$ except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

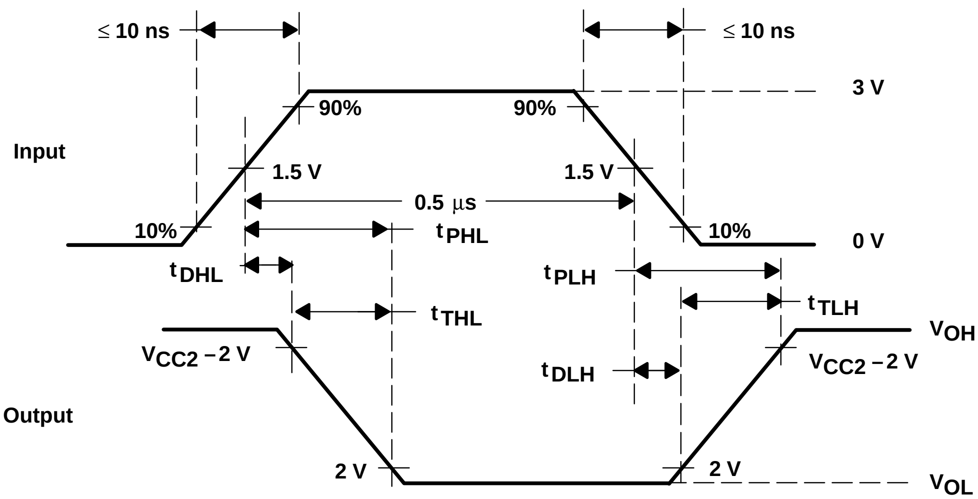
switching characteristics, $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $V_{CC3} = 24$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	$C_L = 200$ pF, $R_D = 24\ \Omega$, See Figure 1		20	30	ns
t_{DHL}	Delay time, high-to-low-level output			10	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	30	50	ns
t_{TLH}	Transition time, low-to-high-level output			20	30	ns
t_{THL}	Transition time, high-to-low-level output			20	30	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 1. Test Circuit and Voltage Waveforms, Each Driver

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

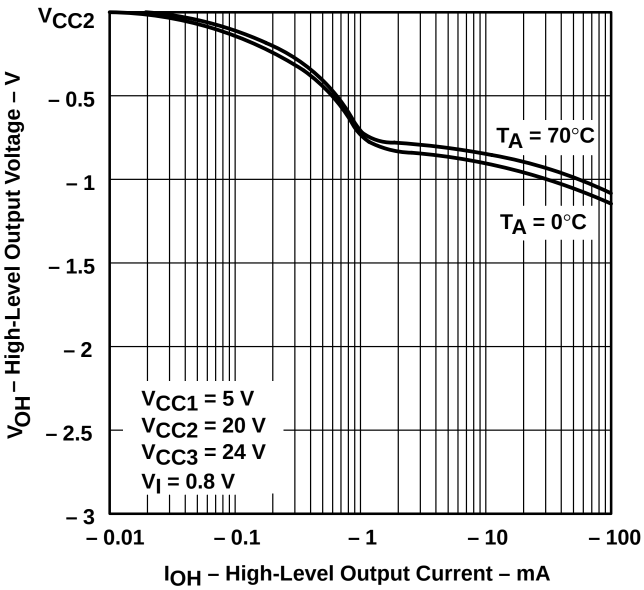


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

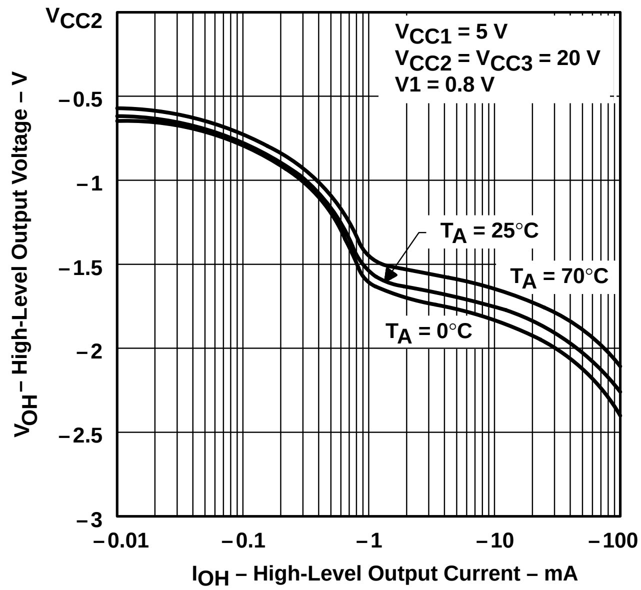


Figure 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

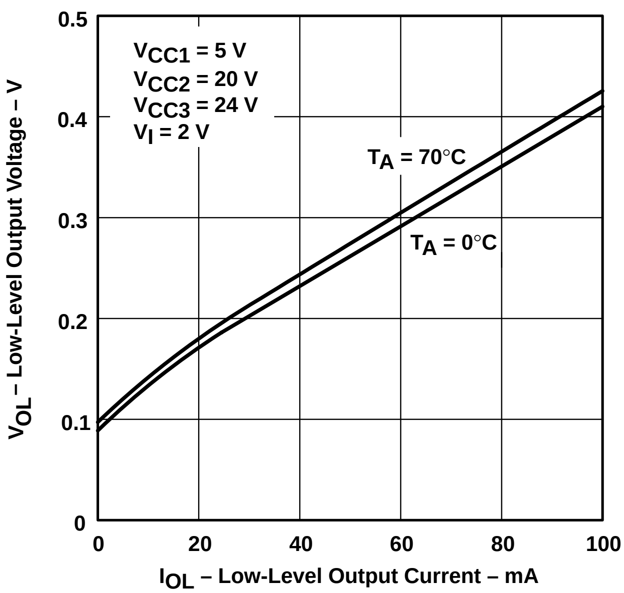


Figure 4

VOLTAGE TRANSFER CHARACTERISTICS

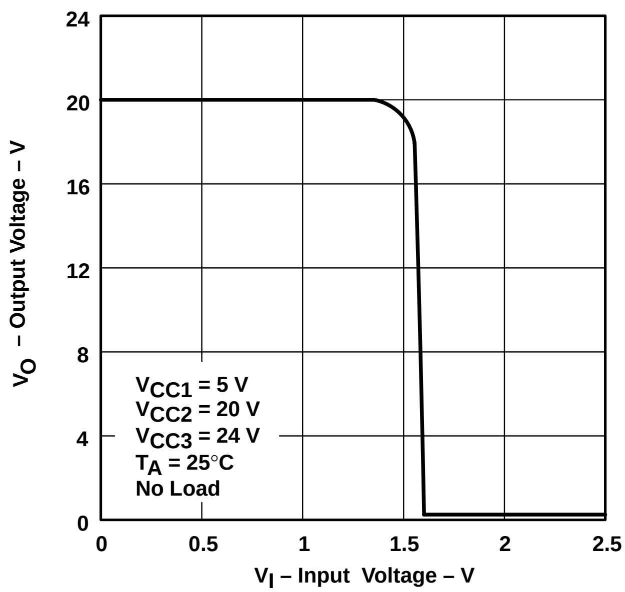


Figure 5

TYPICAL CHARACTERISTICS

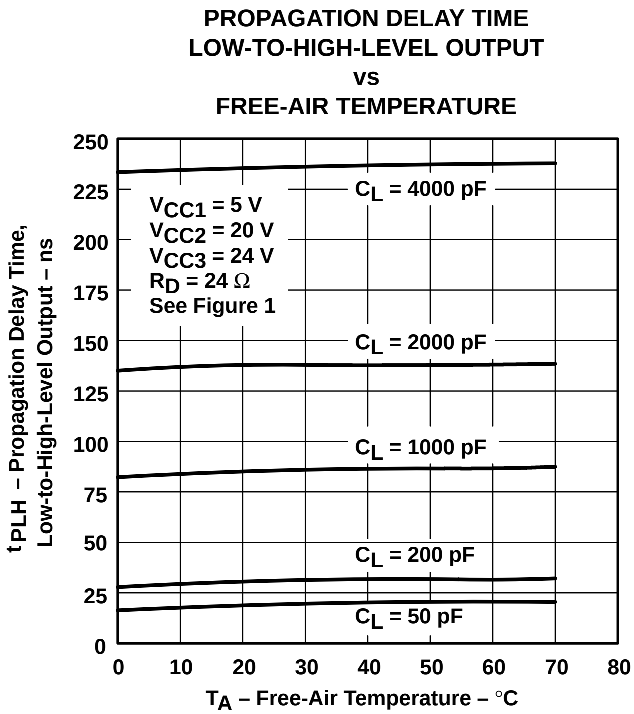


Figure 6

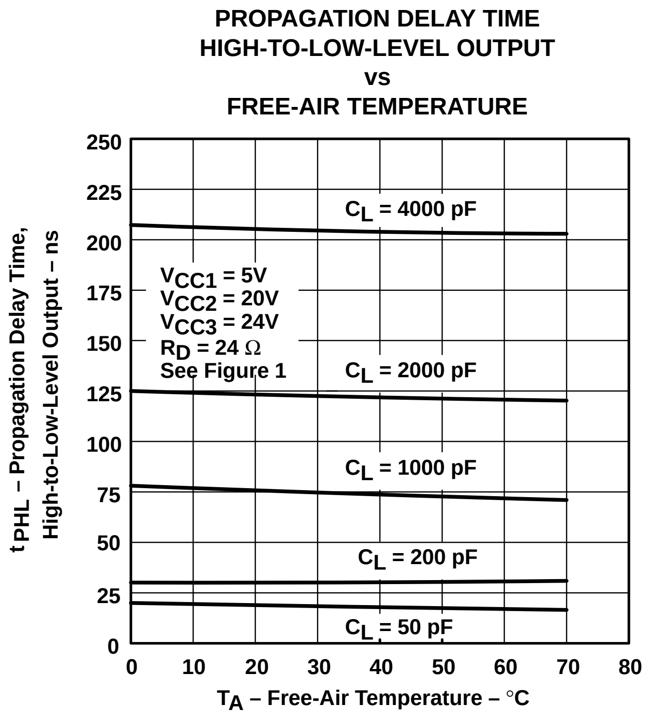


Figure 7

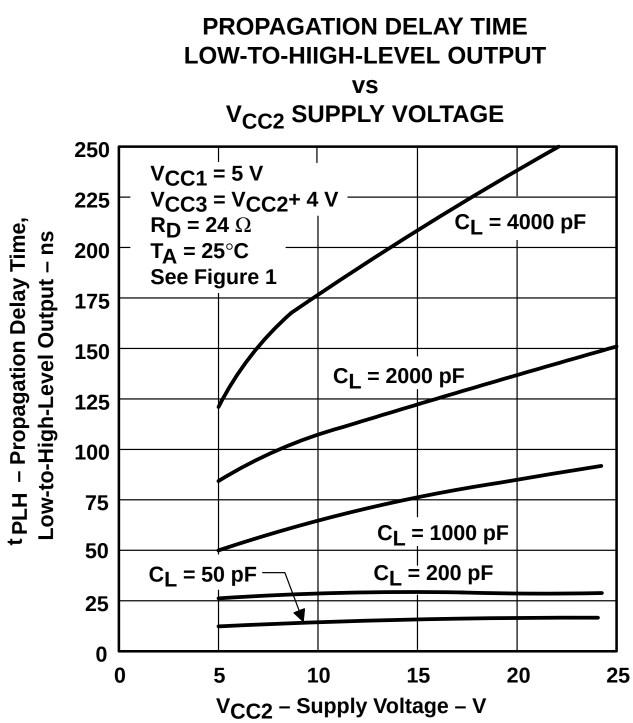


Figure 8

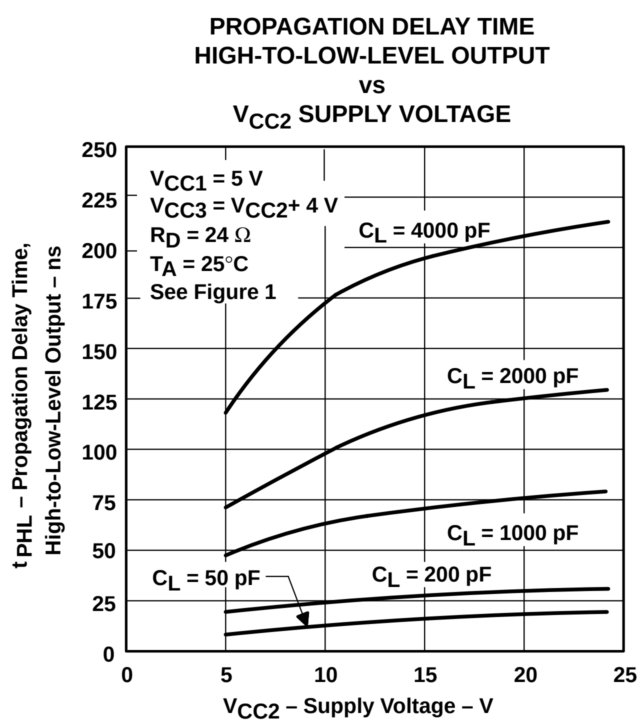


Figure 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME LOW-TO-HIGH-LEVEL OUTPUT vs LOAD CAPACITANCE

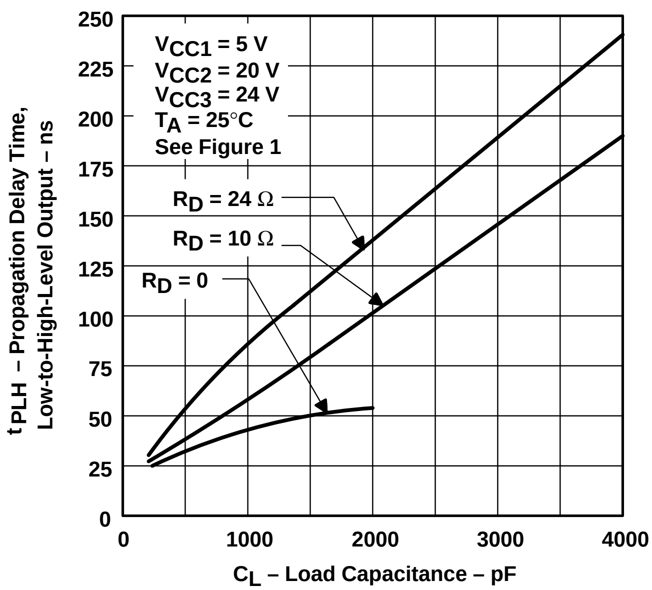


Figure 10

PROPAGATION DELAY TIME HIGH-TO-LOW-LEVEL OUTPUT vs LOAD CAPACITANCE

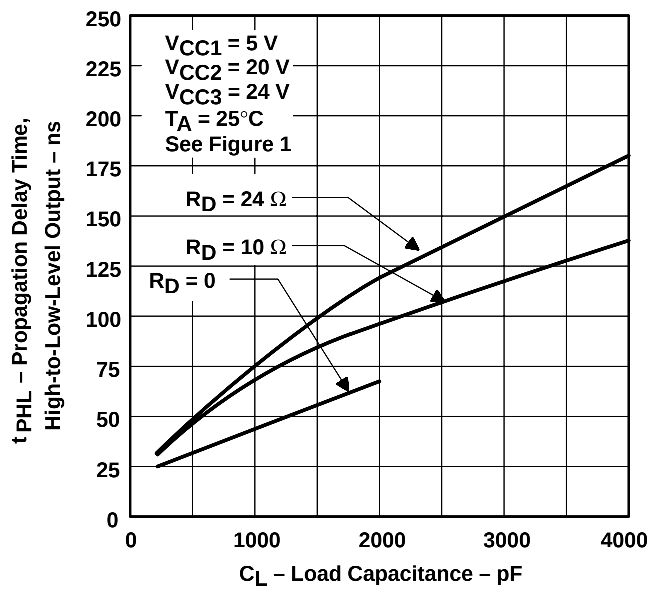


Figure 11

POWER DISSIPATION (ALL DRIVERS) vs FREQUENCY

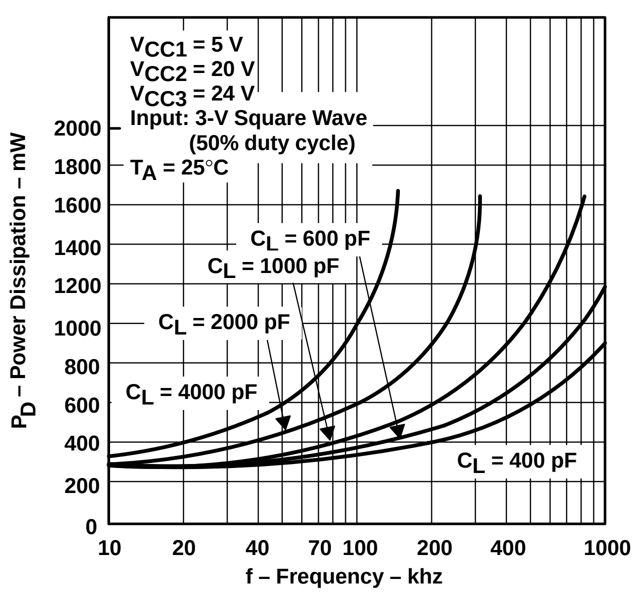


Figure 12

NOTE: For $R_D = 0$, operation with $C_L > 2000$ pF violates absolute maximum current rating.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75374 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 12 shows the power dissipated in a typical SN75374 as a function of frequency and load capacitance. Average power dissipated by this driver is derived from the equation

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_H t_H + P_L t_L}{T}$$

$$P_{C(AV)} \approx C\, V^2{}_C f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

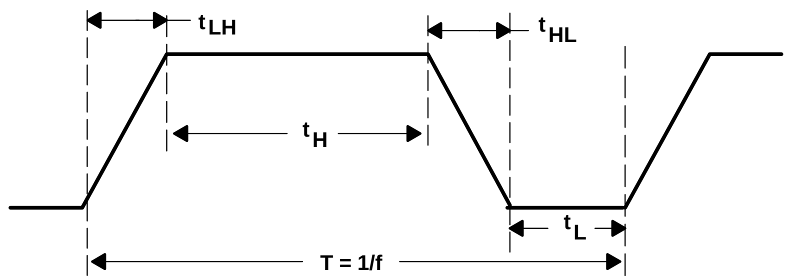


Figure 13. Output Voltage Waveform

where the times are as defined in Figure 15.

THERMAL INFORMATION

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation, C is the load capacitance. V_C is the voltage across the load capacitance during the charge cycle shown by the equation

$$V_C = V_{OH} - V_{OL}$$

$P_{S(AV)}$ may be ignored for power calculations at low frequencies.

In the following power calculation, all four channels are operating under identical conditions: f = 0.2 MHz, V_{OH} = 19.9 V and V_{OL} = 0.15 V with V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, V_C = 19.75 V, C = 1000 pF, and the duty cycle = 60%. At 0.2 MHz for C_L < 2000 pF, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is low, I_{CC2} is negligible and can be ignored.

On a per-channel basis using data sheet values,

$$P_{DC(AV)} = \left[(5\ V)\left(\frac{4\ mA}{4}\right) + (20\ V)\left(\frac{-\ 2.2\ mA}{4}\right) + (24\ V)\left(\frac{2.2\ mA}{4}\right)\right](0.6) + \left[(5\ V)\left(\frac{31\ mA}{4}\right) + (20\ V)\left(\frac{0\ mA}{4}\right) + (24\ V)\left(\frac{16\ mA}{4}\right)\right](0.4)$$

$$P_{DC(AV)} = 58.2 \text{ mW per channel}$$

Power during the charging time of the load capacitance is

$$P_{C(AV)} = (1000 \text{ pF})\ (19.75 \text{ V})^2\ (0.2 \text{ MHz}) = 78 \text{ mW per channel}$$

Total power for each driver is

$$P_{T(AV)} = 58.2 \text{ mW} + 78 \text{ mW} = 136.2 \text{ mW}$$

The total package power is

$$P_{T(AV)} = (136.2)\ (4) = 544.8 \text{ mW}$$

APPLICATION INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pullup resistor is not satisfactory for high-speed applications. In Figure 13(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470-Ω pullup resistor. The input capacitance (C_{ISS}) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the product of input capacitance and the pullup resistor is shown in Figure 13(b).

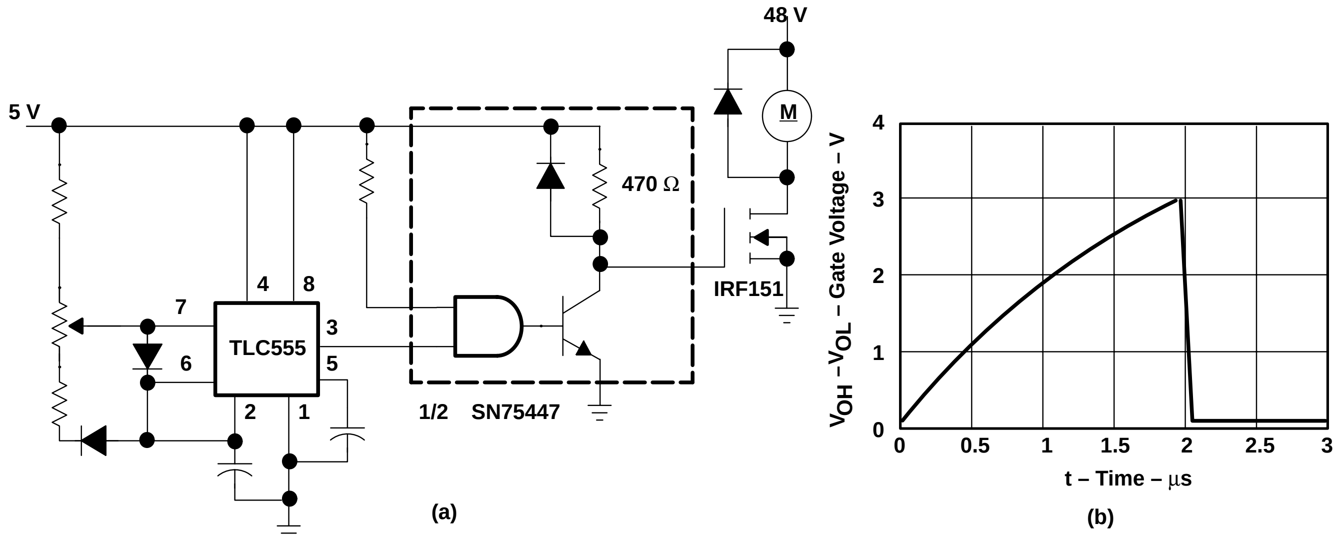


Figure 14. Power MOSFET Drive Using SN75447

A faster, more efficient drive circuit uses an active pull-up as well as an active pull-down output configuration, referred to as a totem-pole output. The SN75374 driver provides the high-speed totem-pole drive desired in an application of this type, see Figure 14(a). The resulting faster switching speeds are shown in Figure 14(b).

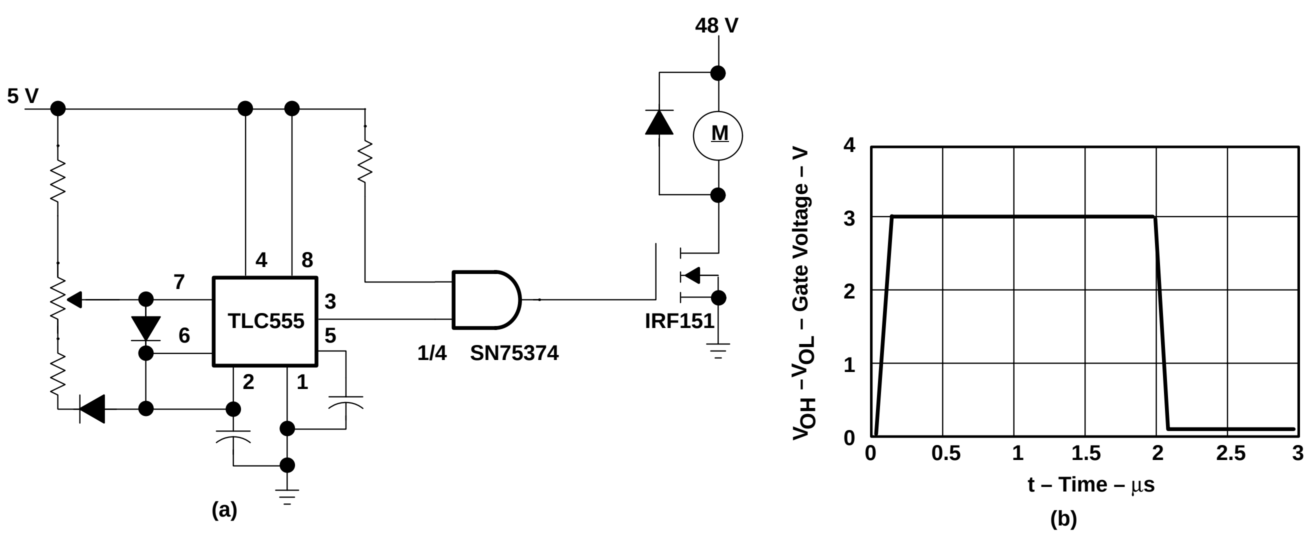


Figure 15. Power MOSFET Drive Using SN75374

APPLICATION INFORMATION

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{PK} = \frac{VC}{t_r}$$

where C is the capacitive load, and t_r is the desired rise time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 14(a), V is found by the equation

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 14(a) is

$$I_{PK} = \frac{(3 - 0)4(10^{-9})}{100(10^{-9})} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a V_{CC} of 5 V and assuming worst-case conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, V_{CC3} should be at least 3 V higher than V_{CC2}.

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