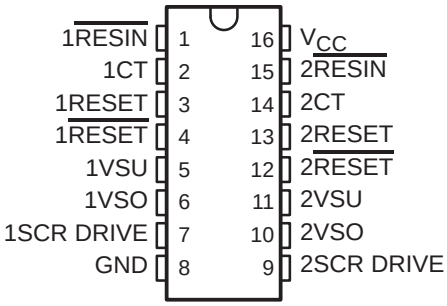
- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **$\overline{\text{RESET}}$ Defined When V_{CC} Exceeds 1 V**
- **Wide Supply-Voltage Range . . . 3.5 V to 18 V**
- **Precision Overvoltage and Undervoltage Sensing**
- **250-mA Peak Output Current for Driving SCR Gates**
- **2-mA Active-Low SCR Gate Drive for False-Trigger Protection**
- **Temperature-Compensated Voltage Reference**
- **True and Complementary Reset Outputs**
- **Externally Adjustable Output Pulse Duration**

DW OR N PACKAGE
(TOP VIEW)



description

The TL7770 is a monolithic integrated-circuit system supervisor designed for use as a reset controller in microcomputer and microprocessor power-supply systems. This device contains two independent supply-voltage supervisors that monitor the supplies for overvoltage and undervoltage conditions at the VSO and VSU terminals, respectively. When V_{CC} attains the minimum voltage of 1 V during powerup, the $\overline{\text{RESET}}$ output becomes active (low). As V_{CC} approaches 3.5 V, the delay timer function activates, latching RESET and $\overline{\text{RESET}}$ active (high and low, respectively) for a time delay, t_d, after system voltages have achieved normal levels. Above V_{CC} = 3.5 V, taking $\overline{\text{RESIN}}$ low activates the time delay function, RESET and $\overline{\text{RESET}}$, during normal system-voltage levels. To ensure that the microcomputer system has reset, the outputs remain active until the voltage at VSU exceeds the threshold value, V_{IT+}, for a time delay, t_d, which is determined by an external timing capacitor such that:

$$t_d \approx 20 \times 10^3 \times \text{capacitance}$$

where t_d is in seconds and capacitance is in farads.

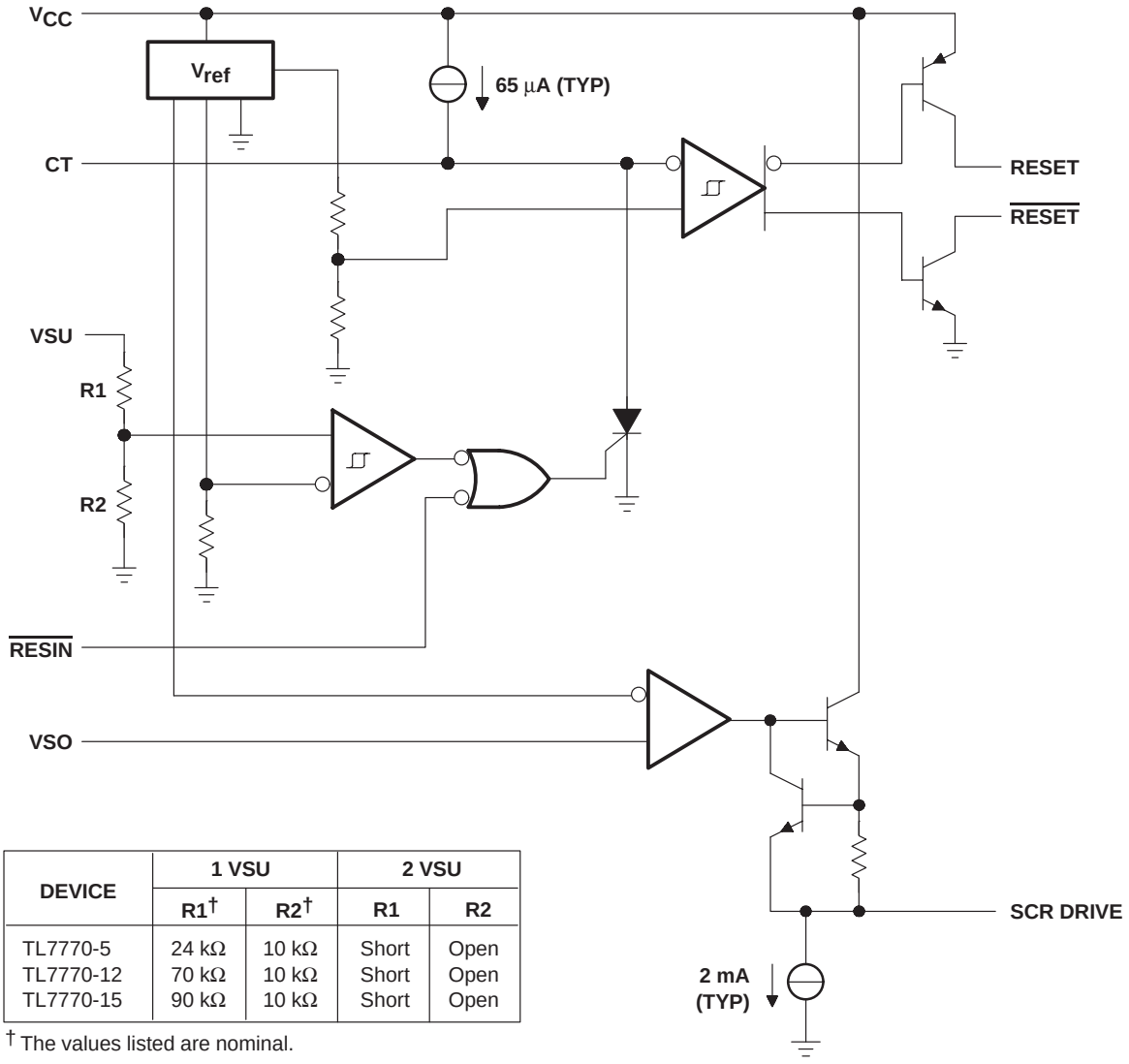
The overvoltage-detection circuit is programmable for a wide range of designs. During an overvoltage condition, an internal silicon-controlled rectifier (SCR) is triggered, providing 250-mA peak instantaneous current and 25-mA continuous current to the SCR gate drive terminal, which can drive an external high-current SCR gate or an overvoltage-warning circuit.

The TL7770C is characterized for operation from 0°C to 70°C. The TL7770I series is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (DW)	PLASTIC DIP (N)	
0°C to 70°C	TL7770-5CDW TL7770-12CDW TL7770-15CDW	TL7770-5CN TL7770-12CN TL7770-15CN	TL7770-5Y TL7770-12Y TL7770-15Y
–40°C to 85°C	TL7770-5IDW TL7770-12IDW TL7770-15IDW	TL7770-5IN TL7770-12IN TL7770-15IN	— — —

functional block diagram (each channel)



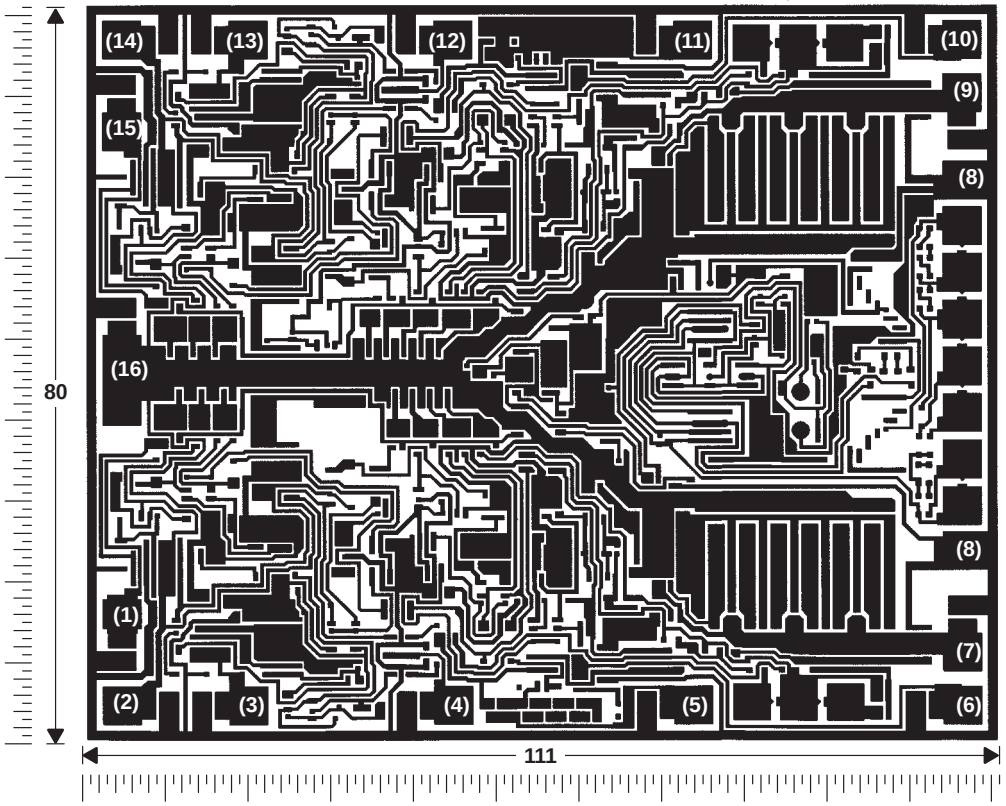
DEVICE	1 VSU		2 VSU	
	R1†	R2†	R1	R2
TL7770-5	24 kΩ	10 kΩ	Short	Open
TL7770-12	70 kΩ	10 kΩ	Short	Open
TL7770-15	90 kΩ	10 kΩ	Short	Open

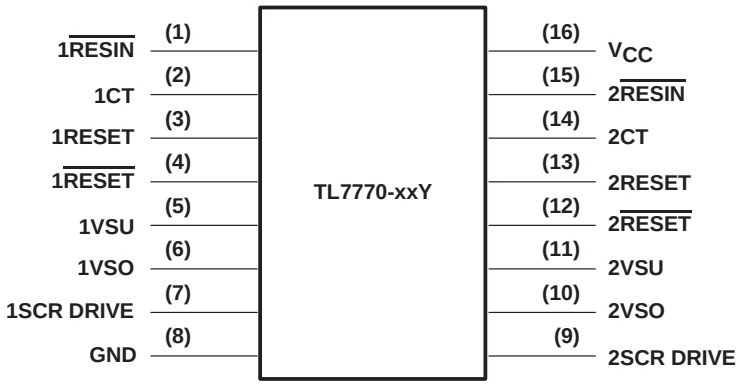
† The values listed are nominal.

TL7770-xxY chip information

These chips, when properly assembled, have characteristics similar to the TL7770-xxC. Thermal compression or ultrasonic bonding can be used on the doped-aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.

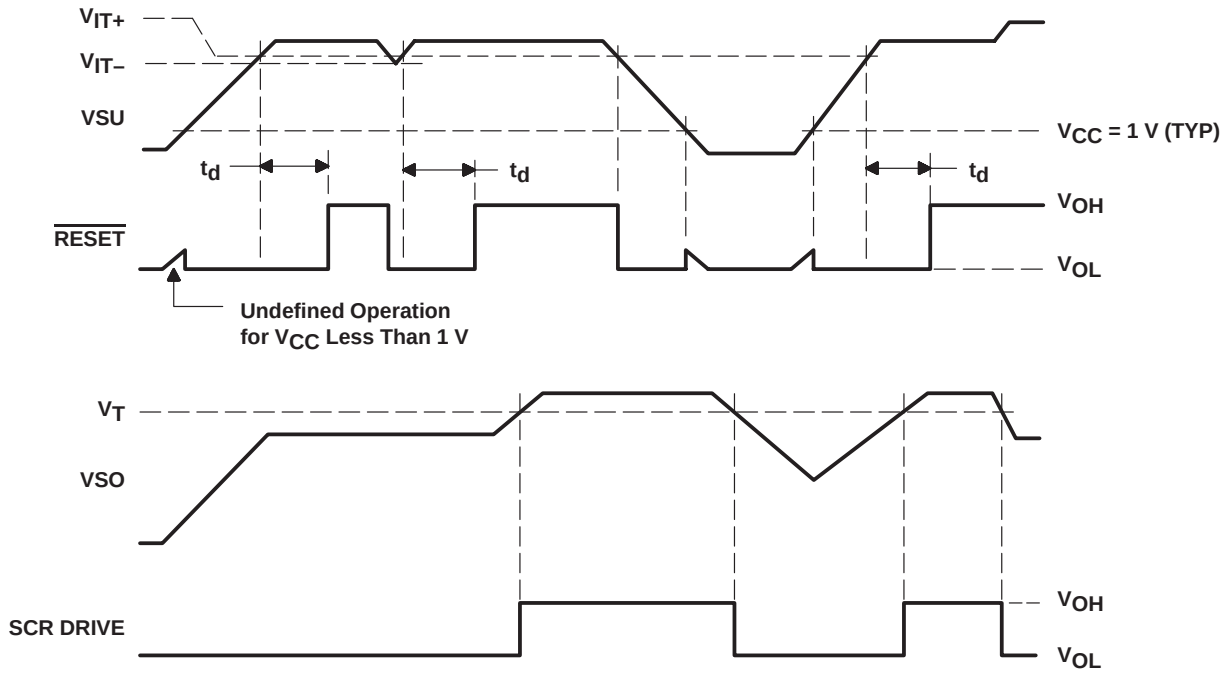
Bonding-Pad Assignments





Chip Thickness: 15 Mils Typical
Bonding Pads: 4 × 4 Mils Minimum
T_J(max) = 150°C
Tolerances Are ±10%.
All Dimensions Are in Mils.

timing requirements



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 20 V
Input voltage range, V_I: 1VSU, 2VSU, 1VSO, and 2VSO (see Note 1) . . . . . –0.3 V to 18 V
Low-level output current (1$\overline{\text{RESET}}$ and 2$\overline{\text{RESET}}$), I_{OL} . . . . . 20 mA
High-level output current (1RESET and 2RESET), I_{OH} . . . . . –20 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . . 105°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: DW or N package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	18	V
Input voltage range, V_I (see Note 3)	1VSU, 2VSU, 2VSO, 1VSO	0	18	V
Output voltage, V_O (1CT, 2CT)			5	V
High-level input voltage range, V_{IH} ($1\overline{RESIN}$, $2\overline{RESIN}$)		2	18	V
Low-level input voltage range, V_{IL} ($1\overline{RESIN}$, $2\overline{RESIN}$)		0	0.8	V
Output sink current, I_O (1CT, 2CT)			50	μA
High-level output current, I_{OH} (1RESET, 2RESET)			–16	mA
Low-level output current, I_{OL} ($1\overline{RESET}$, $2\overline{RESET}$)			16	mA
Continuous output current, I_O (1SCR DRIVE, 2SCR DRIVE)			25	mA
Timing capacitor, C_T			10	μF
Operating free-air temperature, T_A	TL7770C series	0	70	°C
	TL7770I series	–40	85	

NOTE 3: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage, input voltage, output current, and free-air temperature (unless otherwise noted)

supply supervisor section

PARAMETER			TEST CONDITIONS†	TL7770-5C, TL7770-12C TL7770-15C, TL7770-5I TL7770-12I, TL7770-15I			UNIT
				MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	RESET	I_{OH} = –15 mA	V_{CC}–1.5			V
		SCR DRIVE	I_{OH} = –20 mA	V_{CC}–1.5			
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	I_{OL} = 15 mA			0.4	V
$V_{IT–}$	Undervoltage input threshold at VSU (negative-going)	TL7770-5 (5-V sense, 1VSU)	T_A = 25°C	4.5	4.55	4.6	V
		TL7770-12 (12-V sense, 1VSU)		10.8	10.9	11.02	
		TL7770-15 (15-V sense, 1VSU)		13.5	13.64	13.77	
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)		1.485	1.5	1.515	
		TL7770-5 (5-V sense, 1VSU)	T_A = MIN to MAX	4.46		4.64	
		TL7770-12 (12-V sense, 1VSU)		10.68		11.12	
		TL7770-15 (15-V sense, 1VSU)		13.36		13.91	
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)		1.47		1.53	
V_{hys}	Hysteresis at VSU ($V_{IT+} – V_{IT–}$)	TL7770-5 (5-V sense, 1VSU)	T_A = 25°C		15		mV
		TL7770-12 (12-V sense, 1VSU)			36		
		TL7770-15 (15-V sense, 1VSU)			45		
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)			5		
V_T	Overvoltage threshold at VSO	TL7770-5, TL7770-12, TL7770-15 (VSO)	T_A = 25°C	2.53	2.58	2.63	V
			T_A = MIN to MAX	2.48		2.68	
I_I	Input current	$\overline{\text{RESIN}}$	V_I = 5.5 V or 0.4 V			–10	µA
		VSO	V_I = 2.4 V		0.5	2	
I_{OH}	High-level output current	$\overline{\text{RESET}}$	V_O = 18 V			50	µA
I_{OL}	Low-level output current	RESET	V_O = 0			–50	µA
I_{OH}	Peak output current	SCR DRIVE	Duration = 1 ms	250			mA

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

total device

PARAMETER		TEST CONDITIONS†		TL7770-5C TL7770-12C TL7770-15C TL7770-5I TL7770-12I TL7770-15I			UNIT
				MIN	TYP‡	MAX	
V_{res}§	Power-up reset voltage	V_{CC} = VSU			0.8	1	V
I_{CC}	Supply current	1VSU = 18 V, 2VSU = 2 V, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC}, 1VSO and 2VSO at 0 V	T_A = 25°C			5	mA
			T_A = MIN to MAX			6.5	

† For conditions shown as MIN or MAX, use the appropriate value specified in the recommended operating conditions.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

electrical characteristics over recommended ranges of supply voltage, input voltage, and output current (unless otherwise noted)

supply supervisor section

PARAMETER			TEST CONDITIONS	TL7770-5Y TL7770-12Y TL7770-15Y			UNIT
				MIN	TYP†	MAX	
V_{IT-}	Undervoltage input threshold at VSU (negative-going)	TL7770-5 (5-V sense, 1VSU)	T_A = 25°C	4.5	4.55	4.6	V
		TL7770-12 (12-V sense, 1VSU)		10.8	10.9	11.02	
		TL7770-15 (15-V sense, 1VSU)		13.5	13.64	13.77	
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)		1.485	1.5	1.515	
V_{hys}	Hysteresis at VSU ($V_{IT+} - V_{IT-}$)	TL7770-5 (5-V sense, 1VSU)	T_A = 25°C		15		mV
		TL7770-12 (12-V sense, 1VSU)			36		
		TL7770-15 (15-V sense, 1VSU)			45		
		TL7770-5, TL7770-12, TL7770-15 (programmable sense, 2VSU)			5		
V_T	Overvoltage threshold at VSO	TL7770-5, TL7770-12, TL7770-15 (VSO)	T_A = 25°C	2.53	2.58	2.63	V
I_I	Input current	VSO	V_I = 2.4 V		0.5		µA

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

total device

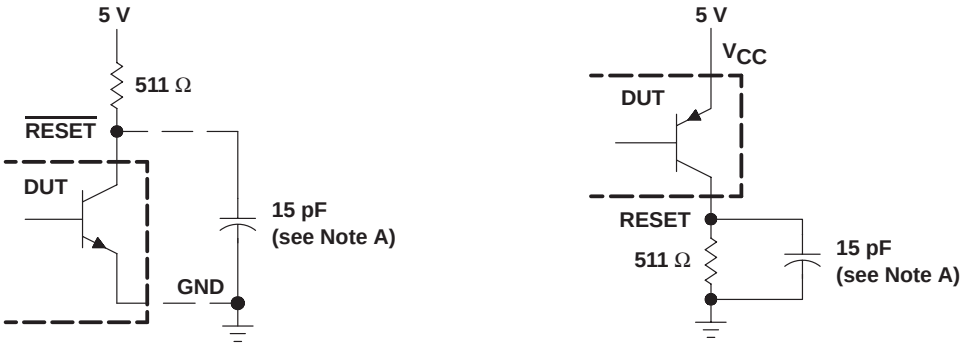
PARAMETER		TEST CONDITIONS		TL7770-5Y TL7770-12Y TL7770-15Y			UNIT
				MIN	TYP†	MAX	
V_{res}‡	Power-up reset voltage	V_{CC} = VSU,	V_{OL} = 0.4 V, I_{OL} = 1 mA		0.8		V
I_{CC}	Supply current	1$\overline{\text{VSU}}$ = 18 V, 2$\overline{\text{VSU}}$ = 2 V, 1$\overline{\text{RESIN}}$ and 2$\overline{\text{RESIN}}$ at V_{CC}, 1VSO and 2VSO at 0 V	T_A = 25°C			5	mA

† Typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active.

switching characteristics, V_{CC} = 5 V, C_T open, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$\overline{\text{RESIN}}$	RESET	See Figure 1		270	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output	$\overline{\text{RESIN}}$	$\overline{\text{RESET}}$			270	500	ns
t_r	Rise time		RESET				75	ns
t_f	Fall time					150		
t_r	Rise time		$\overline{\text{RESET}}$			75		ns
t_f	Fall time						50	
$t_{w(min)}$	Minimum effective pulse duration	$\overline{\text{RESIN}}$		See Figure 2a		150		ns
		VSU		See Figure 2b		100		

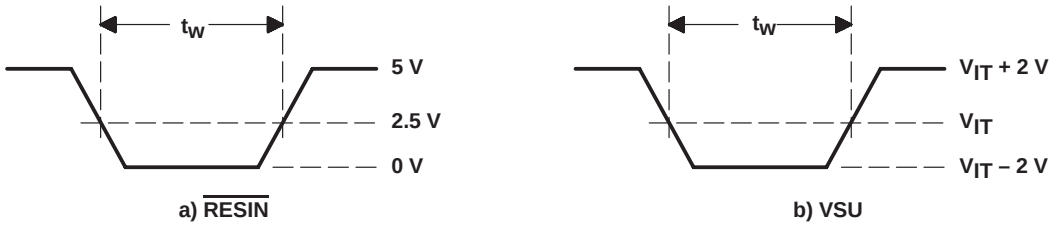
PARAMETER MEASUREMENT INFORMATION



$\overline{\text{RESET}}$ OUTPUT CONFIGURATION **RESET OUTPUT CONFIGURATION**

NOTE A: This includes jig and probe capacitance.

Figure 1. $\overline{\text{RESET}}$ and RESET Output Configurations

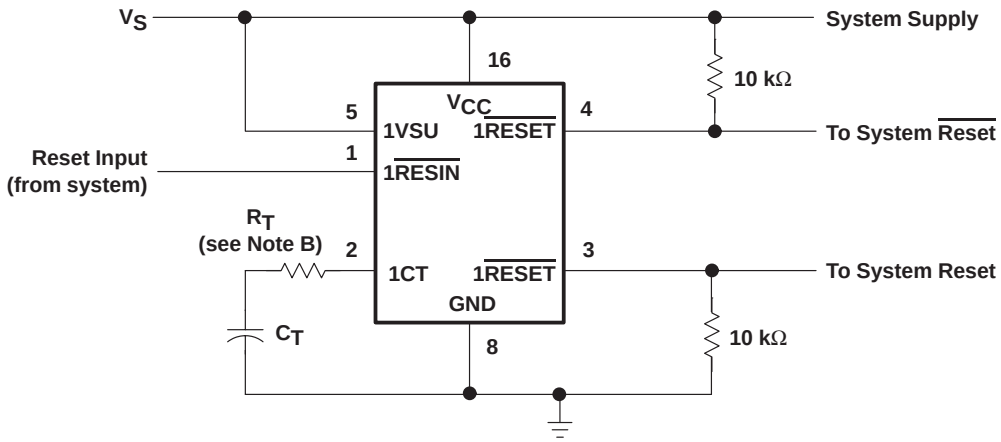


a) $\overline{\text{RESIN}}$ **b) VSU**

WAVEFORMS

Figure 2. Input Pulse Definition

APPLICATION INFORMATION



NOTE B: When V_{CC} and 1VSU are connected to the same point, it is recommended that series resistance (R_T) be added between the time-delay programming capacitor (C_T) and the voltage-supervisor device terminal (1CT). The suggested R_T value is given by:

$$R_T > \frac{V_I - V_{IT-}}{1 \times 10^{-3}}, \text{ where } V_I = \left(\text{the lesser of 7.1 V or } V_S\right)$$

When this series resistor is used, the t_d calculation is as follows:

$$t_d = \frac{1.3 - \left[\left((6.5E-5) \times 10^{-5}\right) \times R_T\right]}{6.5 \times 10^{-5}} \times C_T$$

Figure 3. System Reset Controller With Undervoltage Sensing

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