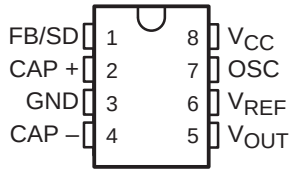
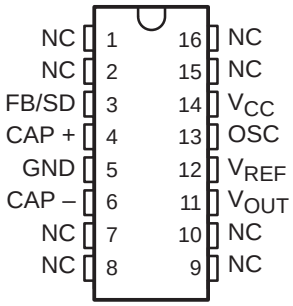
- **Output Current . . . 100 mA**
- **Low Loss . . . 1.1 V at 100 mA**
- **Operating Range . . . 3.5 V to 15 V**
- **Reference and Error Amplifier for Regulation**
- **External Shutdown**
- **External Oscillator Synchronization**
- **Devices Can Be Paralleled**
- **Pin Compatible With the LTC1044/7660**

P PACKAGE
(T0P VIEW)



DW PACKAGE
(T0P VIEW)



NC – No internal connection

description

The LT1054 is a monolithic, bipolar, switched-capacitor voltage converter with regulator. It provides higher output current and significantly lower voltage losses than previously available converters. An adaptive-switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage drop at 100-mA output current is typically 1.1 V. This holds true over the full supply-voltage range of 3.5 V to 15 V. Quiescent current is typically 2.5 mA.

The LT1054 also provides regulation, a feature not previously available in switched-capacitor voltage converters. By adding an external resistive divider, a regulated output can be obtained. This output is regulated against changes in both input voltage and output current. The LT1054 also can be shut down by grounding the feedback terminal. Supply current in shutdown is typically 100 μA.

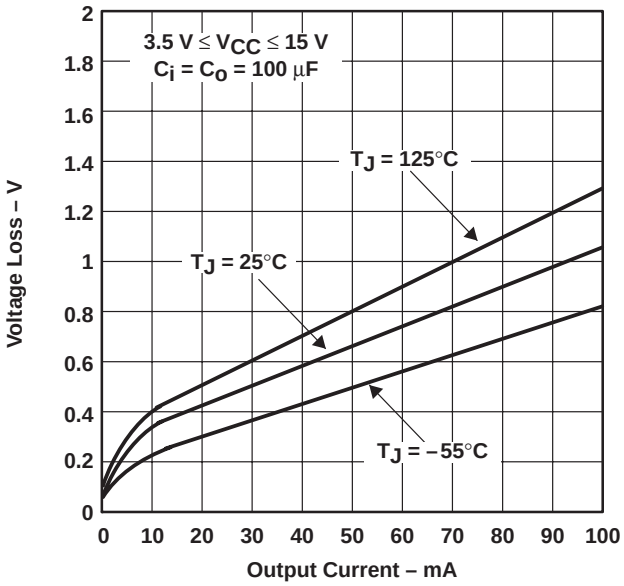
The internal oscillator of the LT1054 runs at a nominal frequency of 25 kHz. The oscillator terminal can be used to adjust the switching frequency or to externally synchronize the LT1054.

AVAILABLE OPTIONS

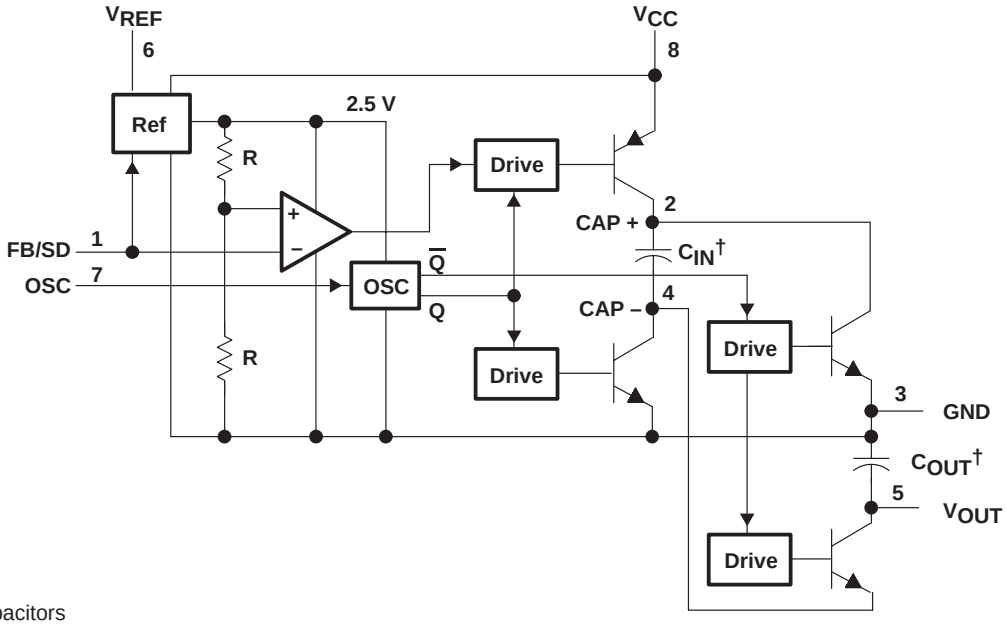
T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (DW)	PLASTIC DIP (P)	
0°C to 70°C	LT1054CDW	LT1054CP	LT1054Y
–40°C to 85°C	LT1054IDW	LT1054IP	—

The DW package is available taped and reeled. Add the suffix R to the device type, (i.e., LT1054CDWR).

VOLTAGE LOSS
vs
OUTPUT CURRENT



functional block diagram

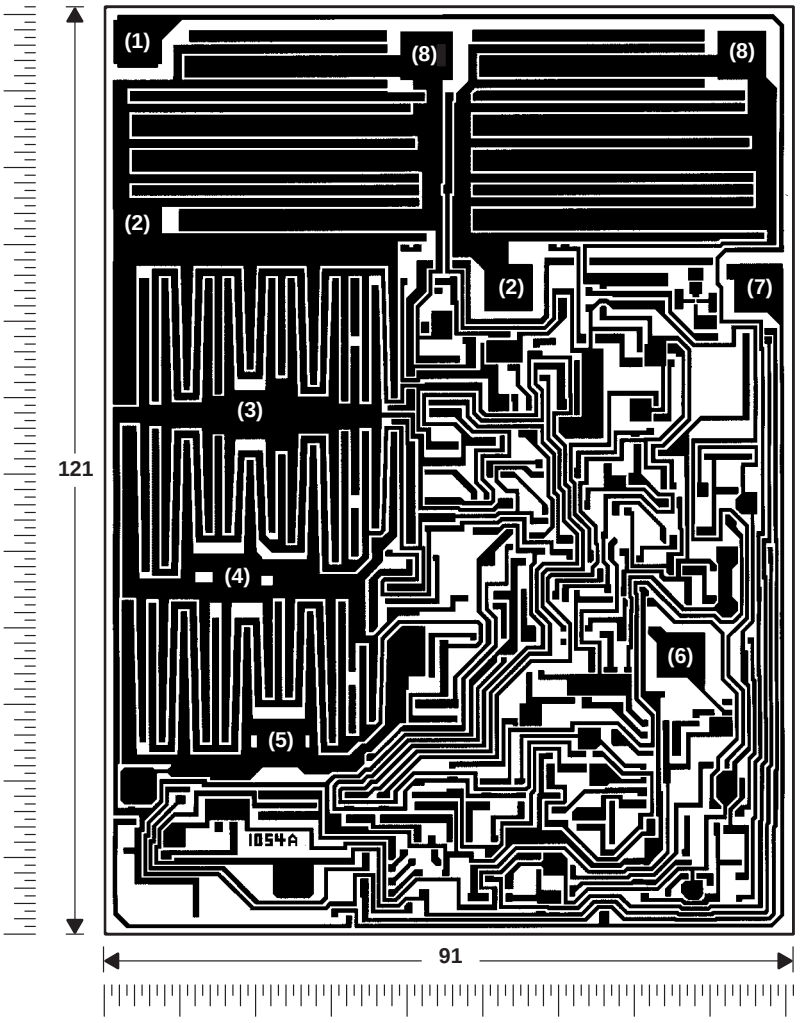


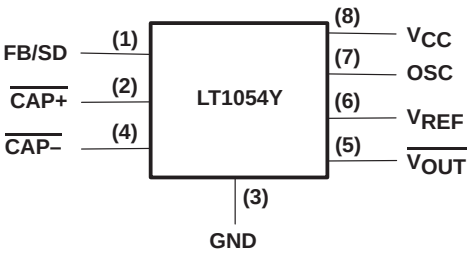
† External capacitors
Pin numbers shown are for the P package only.

LT1054Y chip information

This chip, when properly assembled, displays characteristics similar to the LT1054. Thermal compression or ultrasonic bonding can be used on the doped-aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





Chip Thickness:
15 Mils Typical

Bonding Pads:
4 × 4 Mils Minimum

T_J(max) = 150°C

Tolerances Are ±10%.

All Dimensions Are in Mils.

Pin Numbers Shown Are For the P Package Only

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 16 V
Input voltage range, V_I (FB/SD terminal) . . . . . 0 V to V_{CC}
Input voltage range, V_I (OSC terminal) . . . . . 0 V to V_{ref}
Junction temperature (see Note 2) T_J: LT1054C . . . . . 125°C
LT1054I . . . . . 135°C
Operating free-air temperature range, T_A: LT1054C . . . . . 0°C to 70°C
LT1054I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The absolute maximum supply voltage rating of 16 V is for unregulated circuits. For regulation mode circuits with $V_{OUT} \le 15$ V, this rating may be increased to 20 V.
2. The devices are functional up to the absolute maximum junction temperature.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.5	15	V
Operating free-air temperature range, T_A	LT1054C	0	70	°C
	LT1054I	–40	85	

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A‡	LT1054C, LT1054I			UNIT
						MIN	TYP§	MAX	
V_O	Regulated output voltage	V_{CC} = 7 V, T_J = 25°C, R_L = 500 Ω, See Note 3			25°C	–4.7	–5	–5.2	V
	Input regulation	V_{CC} = 7 V to 12 V, R_L = 500 Ω, See Note 3			Full range		5	25	mV
	Output regulation	V_{CC} = 7 V, See Note 3	R_L = 100 Ω to 500 Ω,		Full range		10	50	mV
	Voltage loss, $V_{CC} - \lvert V_O \rvert$ (see Note 4)	$C_I = C_O$ = 100 µF tantalum		I_O = 10 mA	Full range		0.35	0.55	V
				I_O = 100 mA	Full range		1.1	1.6	
	Output resistance	ΔI_O = 10 mA to 100 mA, See Note 5			Full range		10	15	Ω
	Oscillator frequency	V_{CC} = 3.5 V to 15 V			Full range	15	25	35	kHz
V_{ref}	Reference voltage	$I_{(REF)}$ = 60 µA			25°C	2.35	2.5	2.65	V
					Full range	2.25		2.75	
	Maximum switch current				25°C		300		mA
I_{CC}	Supply current	I_O = 0	V_{CC} = 3.5 V		Full range		2.5	4	mA
			V_{CC} = 15 V		Full range		3	5	
	Supply current in shutdown	$V_{(FB/SD)}$ = 0 V			Full range		100	200	µA

‡ Full range is 0°C to 70°C for the LT1054C and –40°C to 85°C for the LT1054I.
§ All typical values are at T_A = 25°C.

NOTES: 3. All regulation specifications are for a device connected as a positive-to-negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, external capacitor C_{IN} = 10 µF (tantalum), external capacitor C_{OUT} = 100 µF (tantalum) and C1 = 0.002 µF (see Figure 15).
4. For voltage-loss tests, the device is connected as a voltage inverter, with terminals 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations. C_{IN} and C_{OUT} are external capacitors.
5. Output resistance is defined as the slope of the curve (ΔV_O versus ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve is higher at currents less than 10 mA due to the characteristics of the switch transistors.

electrical characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		LT1054Y MIN	LT1054Y TYP	LT1054Y MAX	UNIT
V_O	Regulated output voltage	V_{CC} = 7 V, T_J = 25°C, R_L = 500 Ω, See Note 3			–5		V
	Input regulation	V_{CC} = 7 V to 12 V, R_L = 500 Ω, See Note 3			5		mV
	Output regulation	V_{CC} = 7 V, See Note 3	R_L = 100 Ω to 500 Ω,		10		mV
	Voltage loss, $V_{CC} - \lvert V_O \rvert$ (see Note 4)	$C_I = C_O$ = 100 µF tantalum	I_O = 10 mA		0.35		V
			I_O = 100 mA		1.1		
	Output resistance	ΔI_O = 10 mA to 100 mA, See Note 5			10		Ω
	Oscillator frequency	V_{CC} = 3.5 V to 15 V			25		kHz
V_{ref}	Reference voltage	$I_{(REF)}$ = 60 µA			2.5		V
	Maximum switch current				300		mA
I_{CC}	Supply current	I_O = 0	V_{CC} = 3.5 V		2.5		mA
			V_{CC} = 15 V		3		
	Supply current in shutdown	$V_{(FB/SD)}$ = 0 V			100		µA

NOTES: 3. All regulation specifications are for a device connected as a positive-to-negative converter/regulator with R1 = 20 kΩ, R2 = 102.5 kΩ, external capacitor C_{IN} = 10 µF (tantalum), external capacitor C_{OUT} = 100 µF (tantalum) and C1 = 0.002 µF (see Figure 15).

4. For voltage-loss tests, the device is connected as a voltage inverter, with terminals 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations. C_{IN} and C_{OUT} are external capacitors.

5. Output resistance is defined as the slope of the curve (ΔV_O versus ΔI_O) for output currents of 10 mA to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve is higher at currents less than 10 mA due to the characteristics of the switch transistors.

TYPICAL CHARACTERISTICS

Table of Graphs

Table of Figures

TYPICAL CHARACTERISTICS†

SHUTDOWN THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

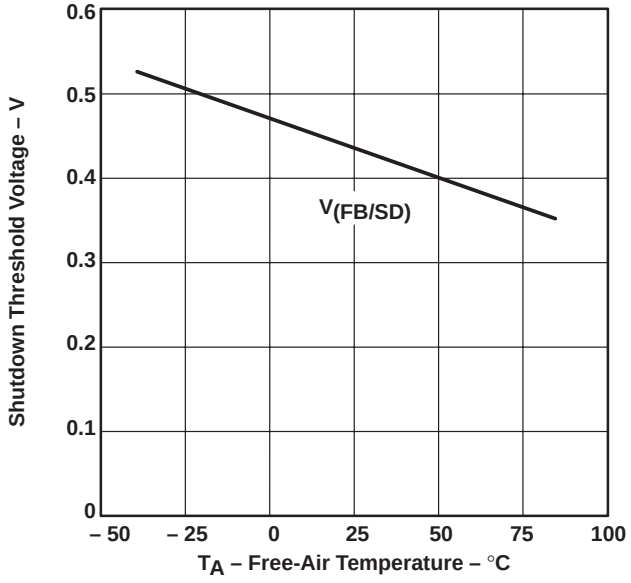


Figure 1

SUPPLY CURRENT vs INPUT VOLTAGE

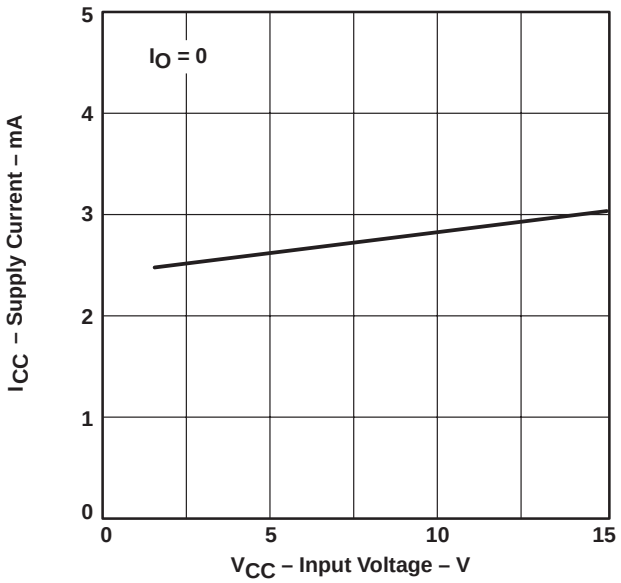


Figure 2

OSCILLATOR FREQUENCY vs FREE-AIR TEMPERATURE

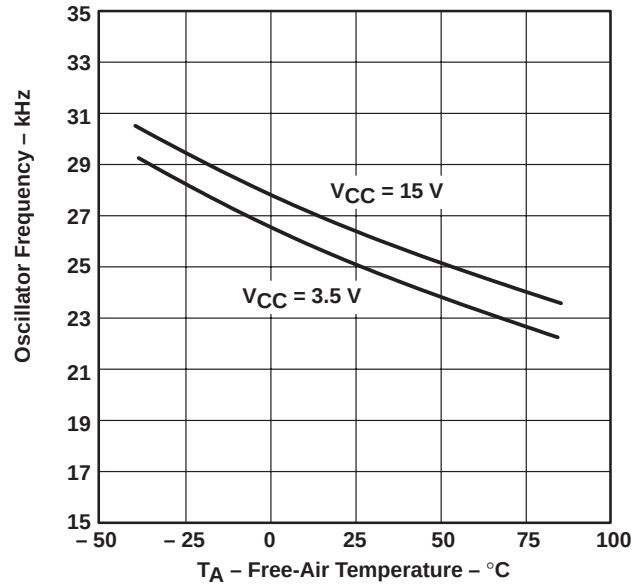


Figure 3

SUPPLY CURRENT IN SHUTDOWN vs INPUT VOLTAGE

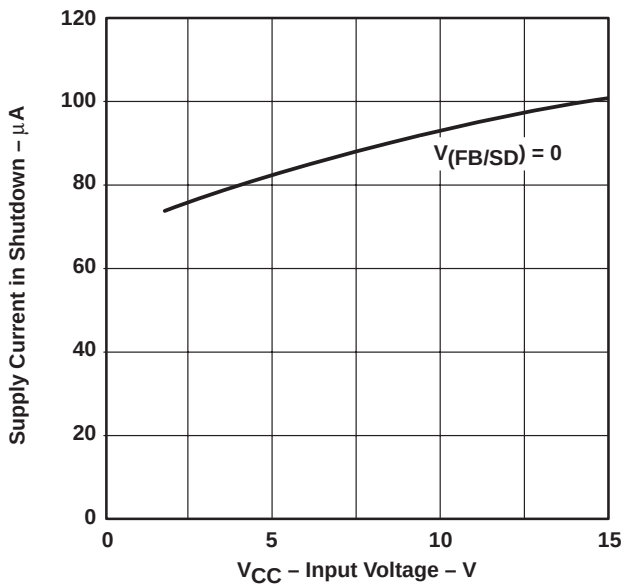


Figure 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT vs OUTPUT CURRENT

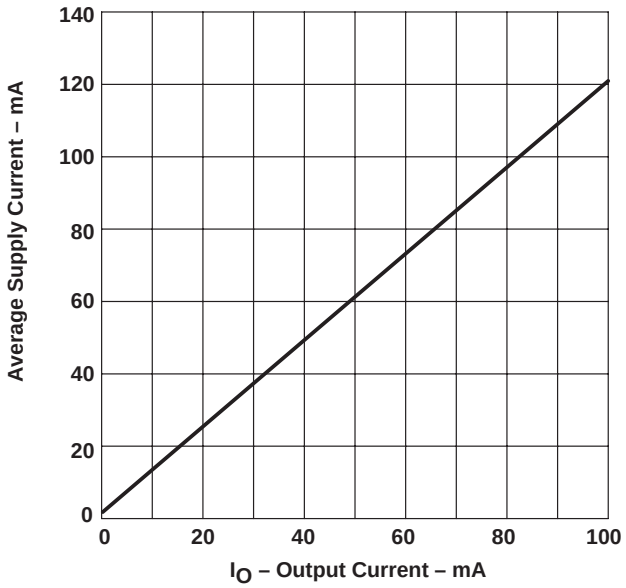


Figure 5

OUTPUT VOLTAGE LOSS vs INPUT CAPACITANCE

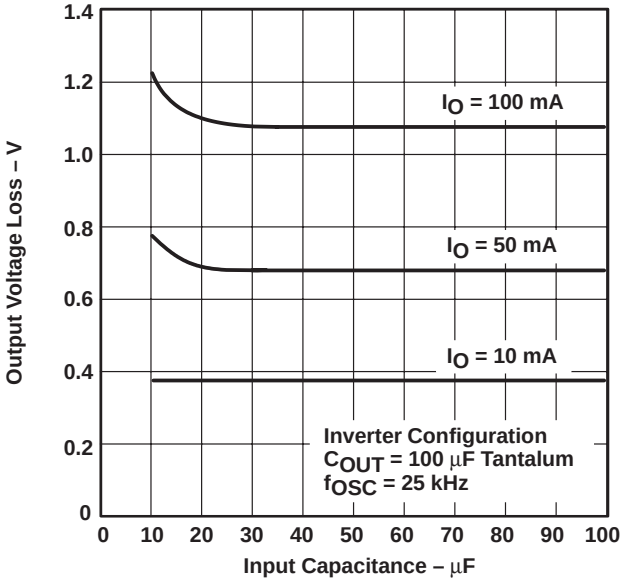


Figure 6

OUTPUT VOLTAGE LOSS vs OSCILLATOR FREQUENCY

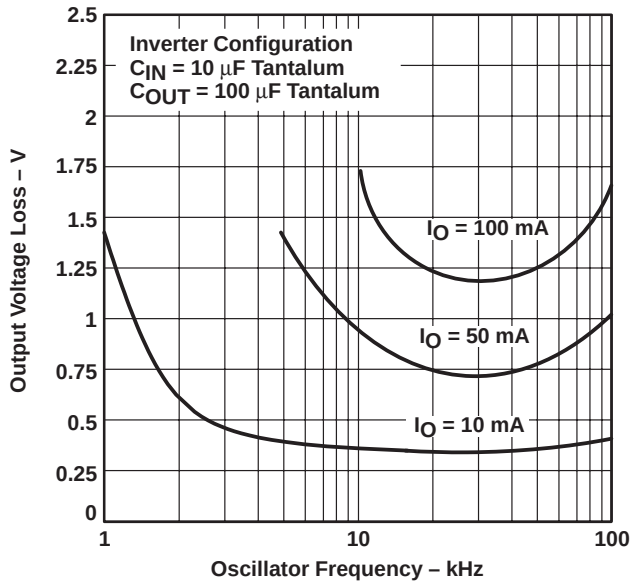


Figure 7

OUTPUT VOLTAGE LOSS vs OSCILLATOR FREQUENCY

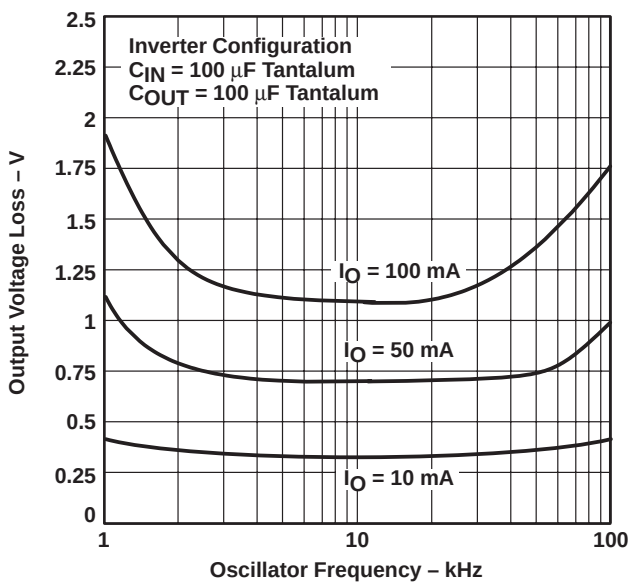


Figure 8

TYPICAL CHARACTERISTICS†

REGULATED OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

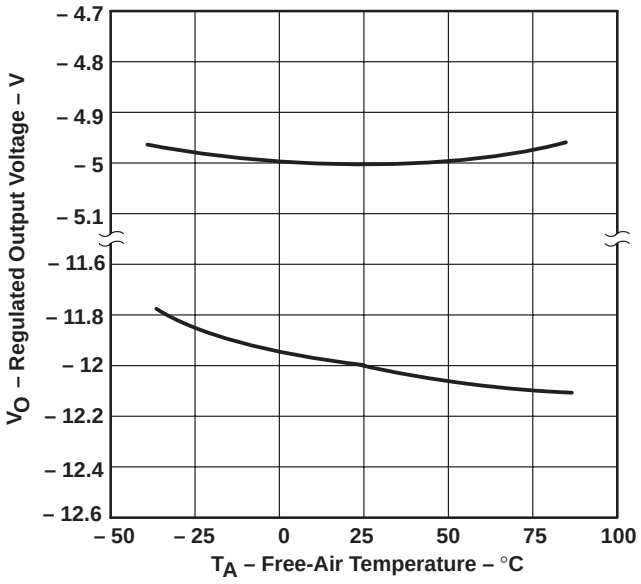


Figure 9

REFERENCE VOLTAGE CHANGE vs FREE-AIR TEMPERATURE

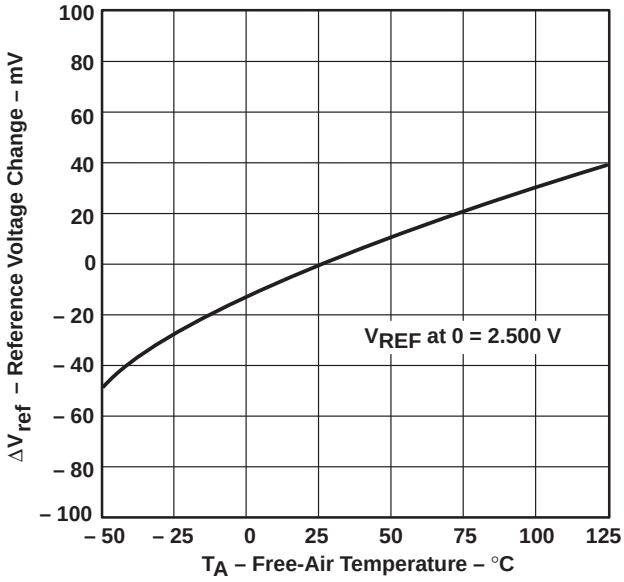


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

PRINCIPLES OF OPERATION

A review of a basic switched-capacitor building block is helpful in understanding the operation of the LT1054. When the switch shown in Figure 11 is in the left position, capacitor C1 charges to the voltage at V1. The total charge on C1 is q1 = C1V1. When the switch is moved to the right, C1 is discharged to the voltage at V2. After this discharge time, the charge on C1 is q2 = C1V2. The charge has been transferred from the source V1 to the output V2. The amount of charge transferred is shown in equation 1.

$$\Delta q = q1 - q2 = C1(V1 - V2) \quad (1)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is as shown in equation 2.

$$I = f \times \Delta q = f \times C1(V1 - V2) \quad (2)$$

To obtain an equivalent resistance for a switched-capacitor network, this equation can be rewritten in terms of voltage and impedance equivalence as shown in equation 3.

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}} \quad (3)$$

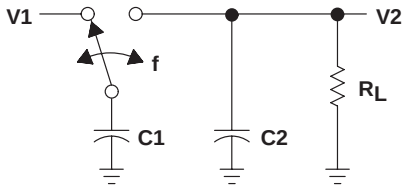


Figure 11. Switched-Capacitor Building Block

PRINCIPLES OF OPERATION

A new variable, R_{EQUIV}, is defined as $R_{EQUIV} = 1 \div fC1$. The equivalent circuit for the switched-capacitor network is shown in Figure 12. The LT1054 has the same switching action as the basic switched-capacitor building block. Even though this simplification does not include finite switch-on resistance and output-voltage ripple, it provides an insight into how the device operates.

These simplified circuits explain voltage loss as a function of oscillator frequency (see Figure 7). As oscillator frequency is decreased, the output impedance is eventually dominated by the 1/fC1 term and voltage losses rise.

Voltage losses also rise as oscillator frequency increases. This is caused by internal switching losses that occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency, this loss becomes significant and voltage losses again rise.

The oscillator of the LT1054 is designed to run in the frequency band where voltage losses are at a minimum.

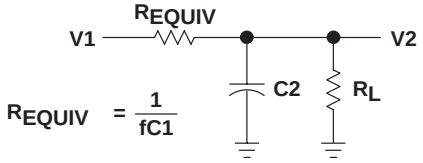


Figure 12. Switched-Capacitor Equivalent Circuit

terminal functions (see functional block diagram)

Supply voltage V_{CC} alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current is approximately 2.2 times the output current. During the time that C_{IN} is delivering a charge to C_{OUT}, the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor supplies part of the peak input current drawn by the LT1054, and averages out the current drawn from the supply. A minimum input supply bypass capacitor of 2 μF, preferably tantalum or some other low equivalent-series-resistance (ESR) type, is recommended. A larger capacitor is desirable in some cases. An example of this would be when the actual input supply is connected to the LT1054 through long leads or when the pulse currents drawn by the LT1054 might affect other circuits through supply coupling.

In addition to being the output terminal, V_{OUT} is tied to the substrate of the device. Special care must be taken in LT1054 circuits to avoid making V_{OUT} positive with respect to any of the other terminals. For circuits with the output load connected from V_{CC} to V_{OUT} or from some external positive supply voltage to V_{OUT}, an external transistor must be added (see Figure 13). This transistor prevents V_{OUT} from being pulled above GND during start up. Any small general-purpose transistor such as a 2N2222 or a 2N2219 device can be used. Resistor R1 should be chosen to provide enough base drive to the external transistor so that it is saturated under nominal output voltage and maximum output current conditions.

$$R1 \leq \frac{\left(|V_{OUT}| \right) \beta}{I_{OUT}} \quad (4)$$

APPLICATION INFORMATION

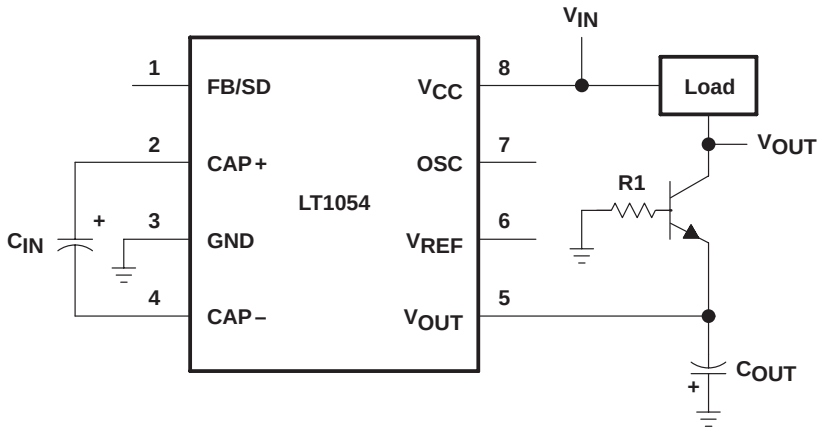


Figure 13. Circuit With Load Connected from V_{CC} to V_{OUT}

The voltage reference (V_{ref}) output provides a 2.5-V reference point for use in LT1054-based regulator circuits. The temperature coefficient (TC) of the reference voltage has been adjusted so that the TC of the regulated output voltage is near zero. As seen in the typical performance curves, this requires the reference output to have a positive TC. This non-zero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback terminal. The overall result of these drift terms is a regulated output that has a slight positive TC at output voltages below 5 V and a slight negative TC at output voltages above 5 V. For regulator feedback networks, reference output current should be limited to approximately 60 μA. V_{ref} draws approximately 100 μA when shorted to ground and does not affect the internal reference/regulator. This terminal also can be used as a pullup for LT1054 circuits that require synchronization.

CAP+ is the positive side of input capacitor C_{IN} and is alternately driven between V_{CC} and ground. When driven to V_{CC}, CAP+ sources current from V_{CC}. When driven to ground, CAP+ sinks current to ground. CAP– is the negative side of the input capacitor and is driven alternately between ground and V_{OUT}. When driven to ground, CAP– sinks current to ground. When driven to V_{OUT}, CAP– sources current from C_{OUT}. In all cases, current flow in the switches is unidirectional, as should be expected when using bipolar switches.

The OSC can be used to raise or lower the oscillator frequency or to synchronize the device to an external clock. Internally, OSC is connected to the oscillator timing capacitor ($C_t \approx 150$ pF), which is alternately charged and discharged by current sources of ±7 μA, so that the duty cycle is approximately 50%. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However, the frequency can be raised, lowered, or synchronized to an external system clock if necessary.

The frequency can be increased by adding an external capacitor (C2 in Figure 14) in the range of 5 pF – 20 pF from CAP+ to OSC. This capacitor couples a charge into C_t at the switch transitions. This shortens the charge and discharge time and raises the oscillator frequency. Synchronization can be accomplished by adding an external pullup resistor from OSC to V_{ref}. A 20-kΩ pullup resistor is recommended. An open-collector gate or an NPN transistor can then be used to drive OSC at the external clock frequency as shown in Figure 14.

The frequency can be lowered by adding an external capacitor (C_1 in Figure 14) from OSC to ground. This increases the charge and discharge times, which lowers the oscillator frequency.

APPLICATION INFORMATION

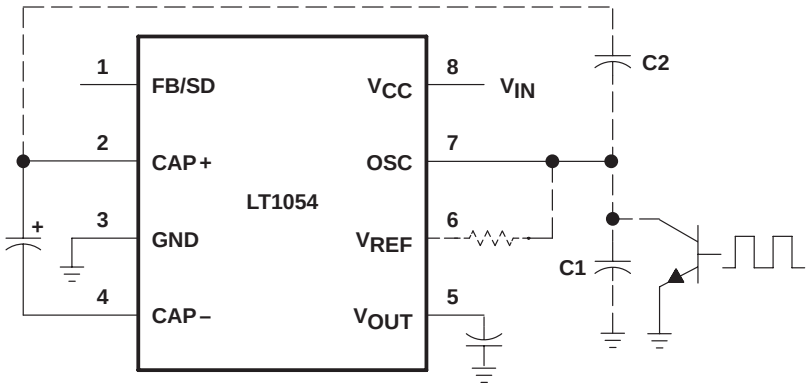
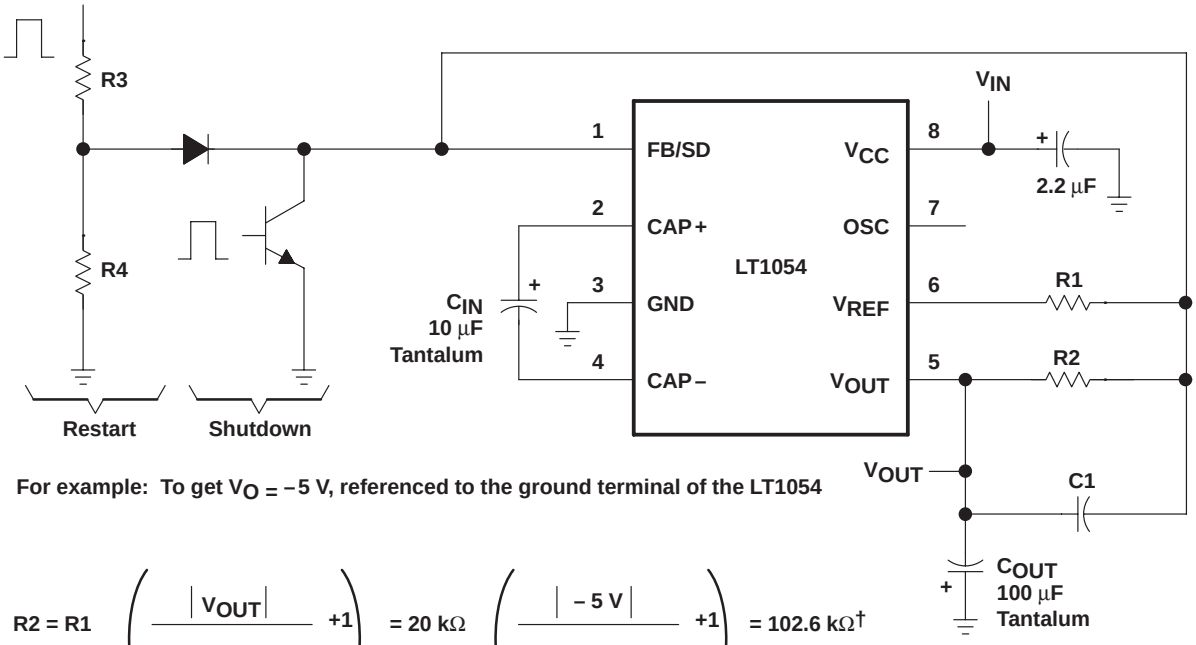


Figure 14. External Clock System

The feedback/shutdown (FB/SD) terminal has two functions. Pulling FB/SD below the shutdown threshold (≈ 0.45 V) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately 100 μA. Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation, the device will restart when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pulldown to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications where the LT1054 is run intermittently, this does not present a problem because the discharge time of the output capacitor is short compared to the off time of the device. In applications where the device has to start up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to FB/SD of the LT1054. Using the circuit shown in Figure 15, the restart signal can be either a pulse (t_p > 100 μs) or a logic high. Diode coupling the restart signal into FB/SD allows the output voltage to rise and regulate without overshoot. The resistor divider R3/R4 shown in Figure 15 should be chosen to provide a signal level at FB/SD of 0.7 V – 1.1 V.

FB/SD is also the inverting input of the LT1054 error amplifier and, as such, can be used to obtain a regulated output voltage.

APPLICATION INFORMATION



For example: To get $V_O = -5$ V, referenced to the ground terminal of the LT1054

$$R2 = R1 \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1 \right) = 20\text{ k}\Omega \left(\frac{|-5\text{ V}|}{\frac{2.5\text{ V}}{2} - 40\text{ mV}} + 1 \right) = 102.6\text{ k}\Omega\dagger$$

Where: R1 = 20 kΩ
V_{REF} = 2.5 V Nominal

† Choose the closest 1% value

Figure 15. Basic Regulation Configuration

regulation

The error amplifier of the LT1054 drives the pnp switch to control the voltage across the input capacitor (C_{IN}), which determines the output voltage. When the reference and error amplifier of the LT1054 are used, an external resistive divider is all that is needed to set the regulated output voltage. Figure 15 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R1 should be 20 kΩ or greater because the reference current is limited to ±100 μA. R2 should be in the range of 100 kΩ to 300 kΩ. Frequency compensation is accomplished by adjusting the ratio of C_{IN} to C_{OUT}.

For best results, this ratio should be approximately 1 to 10. Capacitor C1, required for good load regulation, should be 0.002 μF for all output voltages.

The functional block diagram shows that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referenced to the ground terminal of the LT1054, must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves. Other configurations, such as the negative doubler, can provide higher voltages at reduced output currents.

APPLICATION INFORMATION

capacitor selection

While the exact values of C_{IN} and C_{OUT} are non-critical, good-quality low-ESR capacitors, such as solid tantalum are necessary to minimize voltage losses at high currents. For C_{IN}, the effect of the ESR of the capacitor is multiplied by four, since switch currents are approximately two times higher than output current. Losses occur on both the charge and discharge cycle, which means that a capacitor with 1 Ω of ESR for C_{IN} has the same effect as increasing the output impedance of the LT1054 by 4 Ω. This represents a significant increase in the voltage losses. C_{OUT} is alternately charged and discharged at a current approximately equal to the output current. The ESR of the capacitor causes a step function to occur in the output ripple at the switch transitions. This step function degrades the output regulation for changes in output load current and should be avoided. A technique used to gain both low ESR and reasonable cost is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor.

output ripple

The peak-to-peak output ripple is determined by the output capacitor and the output current values. Peak-to-peak output ripple is approximated as shown:

$$\Delta V = \frac{I_{OUT}}{2\ fC_{OUT}} \tag{5}$$

where:

ΔV = p-p ripple
f_{OSC} = oscillator frequency

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is approximately equal to:

$$(2I_{OUT})\ (\text{ESR of } C_{OUT}) \tag{6}$$

power dissipation

The power dissipation of any LT1054 circuit must be limited so that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation is calculated from two components, the power loss due to voltage drops in the switches, and the power loss due to drive current losses. The total power dissipated by the LT1054 is calculated as shown.

$$P \approx (V_{CC} - |V_{OUT}|)\ I_{OUT} + (V_{CC})\ (I_{OUT})\ (0.2) \tag{7}$$

where both V_{CC} and V_{OUT} are referenced to ground. The power dissipation is equivalent to that of a linear regulator. Limited power-handling capability of the LT1054 packages causes limited output-current requirements or steps can be taken to dissipate power external to the LT1054 for large input or output differentials. This is accomplished by placing a resistor in series with C_{IN} as shown in Figure 16. A portion of the input voltage is dropped across this resistor without affecting the output regulation. Since switch current is approximately 2.2 times the output current and the resistor causes a voltage drop when C_{IN} is both charging and discharging, the resistor chosen is as shown:

$$R_X = V_X/(4.4\ I_{OUT})$$

where:

$$V_X \approx V_{CC} - \left[(\text{LT1054 voltage loss})\ (1.3) + |V_{OUT}|\right] \tag{8}$$

and I_{OUT} = maximum required output current. The factor of 1.3 allows some operating margin for the LT1054.

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When using a 12-V to –5-V converter at 100-mA output current, calculate the power dissipation without an external resistor.

$$P = (12\ V - |-5\ V|)\ (100\ mA) + (12\ V)\ (100\ mA)\ (0.2)$$

$$P = 700\ mW + 240\ mW = 940\ mW$$

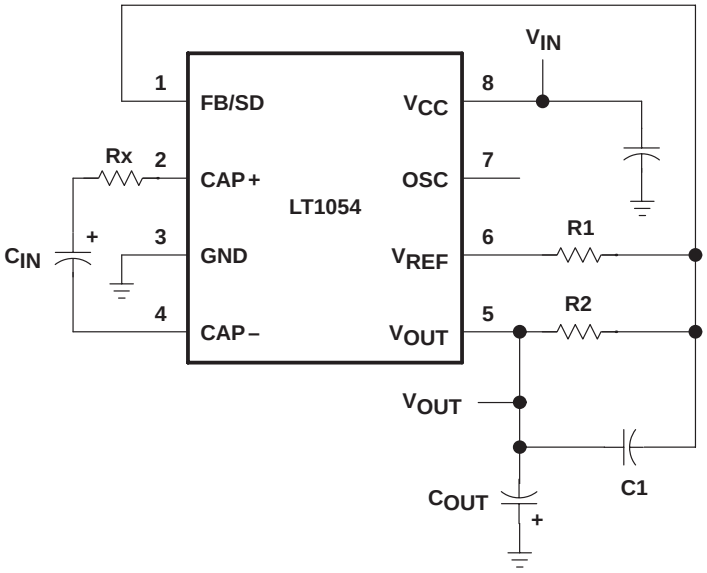


Figure 16. Power-Dissipation-Limiting Resistor in Series with C_{IN}

At $R_{\theta JA}$ of 130°C/W for a commercial plastic device, a junction temperature rise of 122°C is seen. The device exceeds the maximum junction temperature at an ambient temperature of 25°C. To calculate the power dissipation with an external resistor (R_X), determine how much voltage can be dropped across R_X. The maximum voltage loss of the LT1054 in the standard regulator configuration at 100 mA output current is 1.6 V.

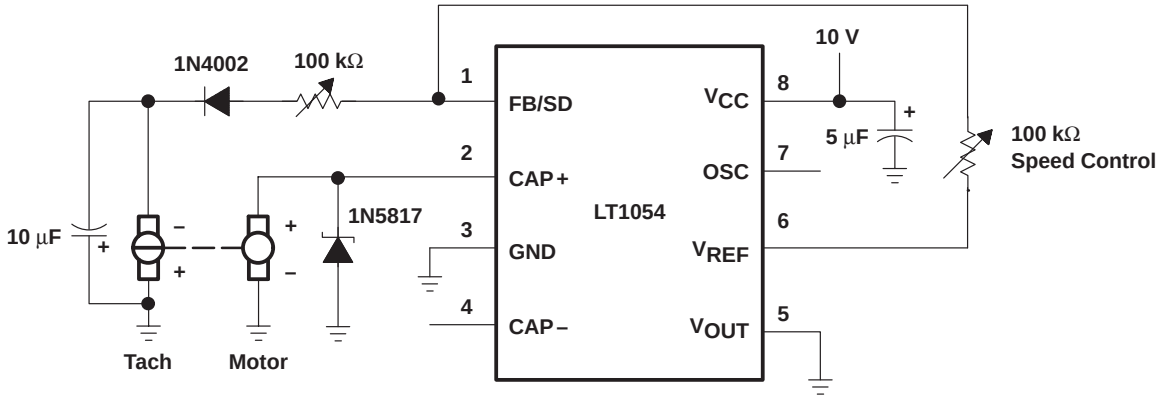
and

$$V_X = 12\ V - \left[(1.6\ V)\ (1.3) + |-5\ V|\right] = 4.9\ V$$

$$R_X = 4.9\ V/(4.4)\ (100\ mA) = 11\ \Omega$$

APPLICATION INFORMATION

The resistor reduces the power dissipated by the LT1054 by (4.9 V) (100 mA) = 490 mW. The total power dissipated by the LT1054 is equal to (940 mW – 490 mW) = 450 mW. The junction temperature rise is 58°C. Although commercial devices are functional up to a junction temperature of 125°C, the specifications are tested to a junction temperature of 100°C. In this example, this means limiting the ambient temperature to 42°C. To allow higher ambient temperatures, the thermal resistance numbers for the LT1054 packages represent worst-case numbers with no heat sinking and still air. Small clip-on heat sinks can be used to lower the thermal resistance of the LT1054 package. Airflow in some systems helps to lower the thermal resistance. Wide PC board traces from the LT1054 leads help to remove heat from the device. This is especially true for plastic packages.



NOTE: Motor-Tach Canon CKT26-T5-3SAE

Figure 17. Motor Speed Servo

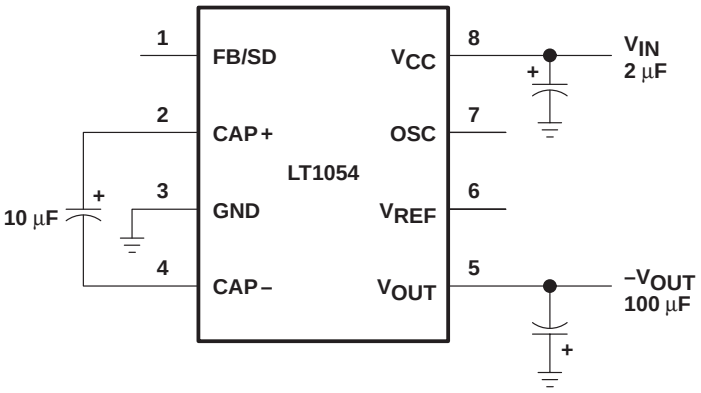
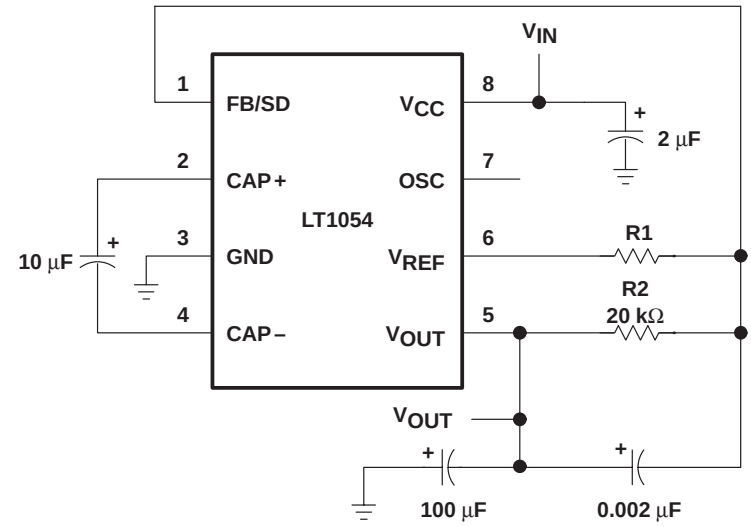


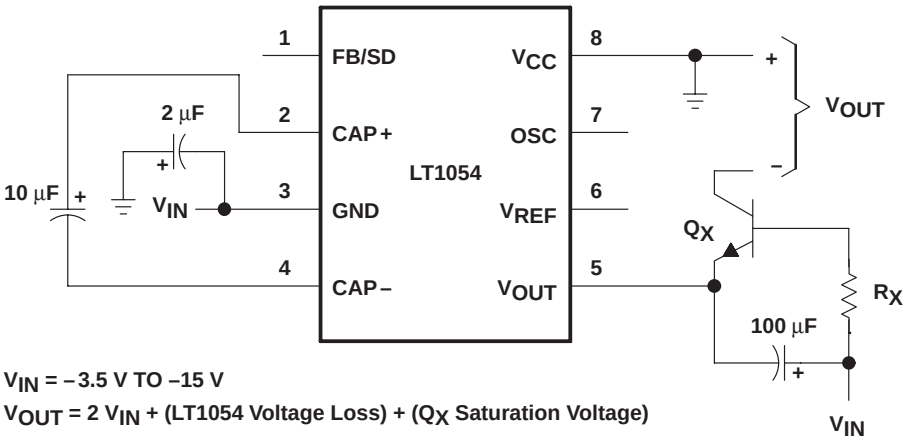
Figure 18. Basic Voltage Inverter

APPLICATION INFORMATION



$$R2 = R1 \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1 \right) = 20\ k\Omega \left(\frac{|V_{OUT}|}{1.21\ V} + 1 \right)$$

Figure 19. Basic Voltage Inverter/Regulator



V_{IN} = –3.5 V TO –15 V

$V_{OUT} = 2\ V_{IN}$ + (LT1054 Voltage Loss) + (Q_X Saturation Voltage)

Figure 20. Negative Voltage Doubler

APPLICATION INFORMATION

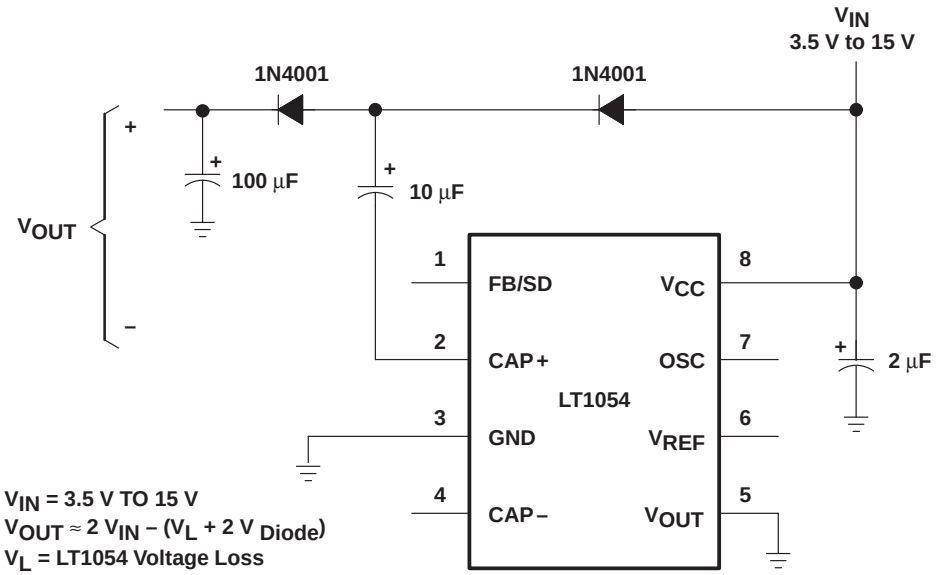
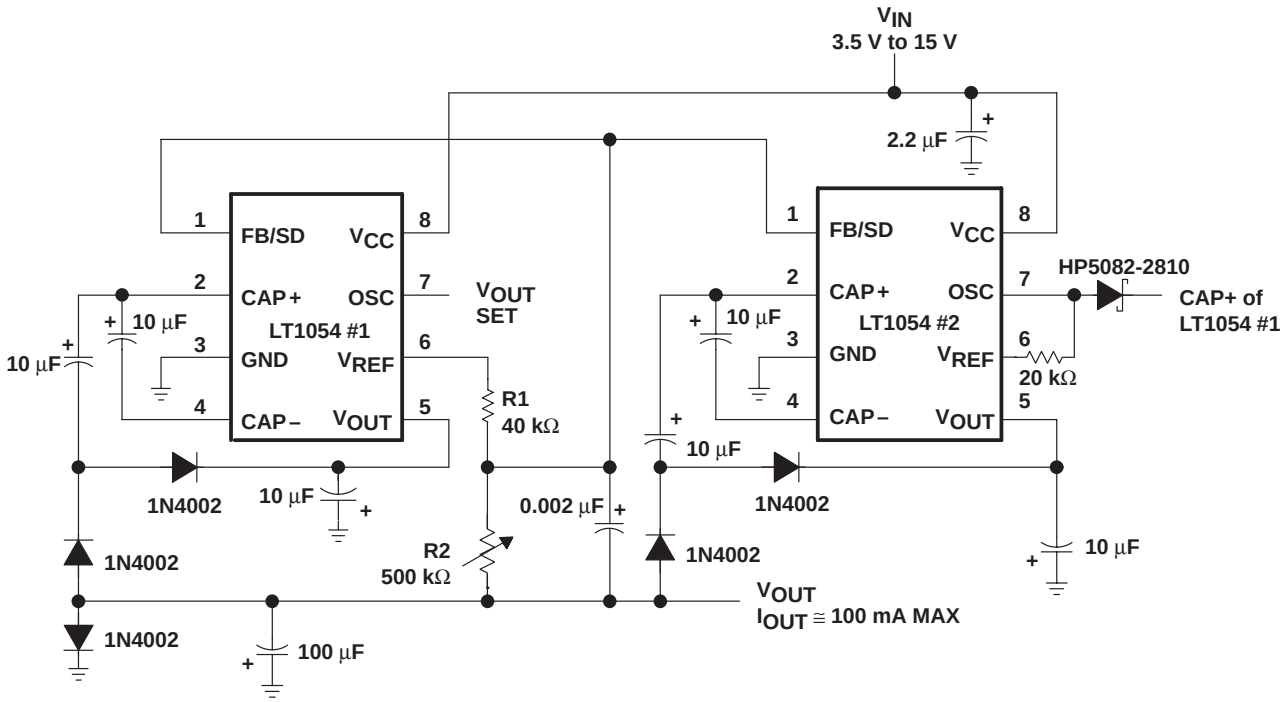


Figure 21. Positive Doubler

APPLICATION INFORMATION



V_{IN} = 3.5 to 15 V
V_{OUT} MAX ≈ –2 V_{IN} + [LT1054 Voltage Loss +2 (V_{Diode})]

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\text{ V}} + 1\right)$$

Figure 22. 100-mA Regulating Negative Doubler

APPLICATION INFORMATION

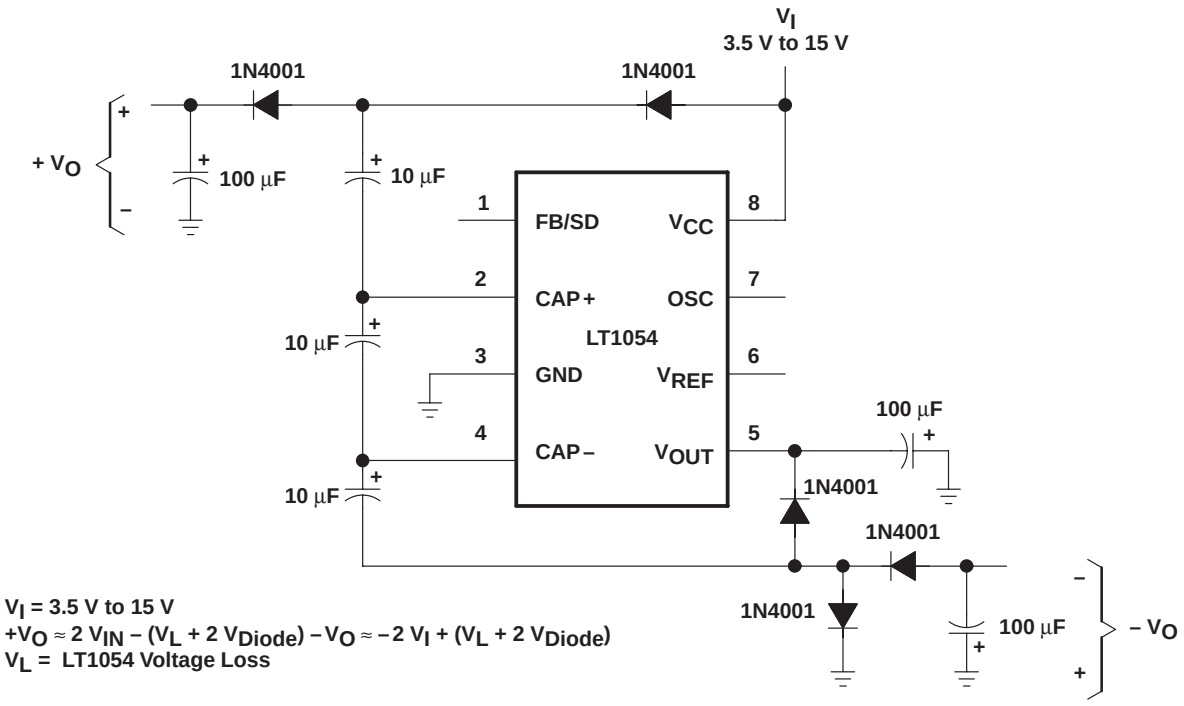


Figure 23. Dual-Output Voltage Doubler

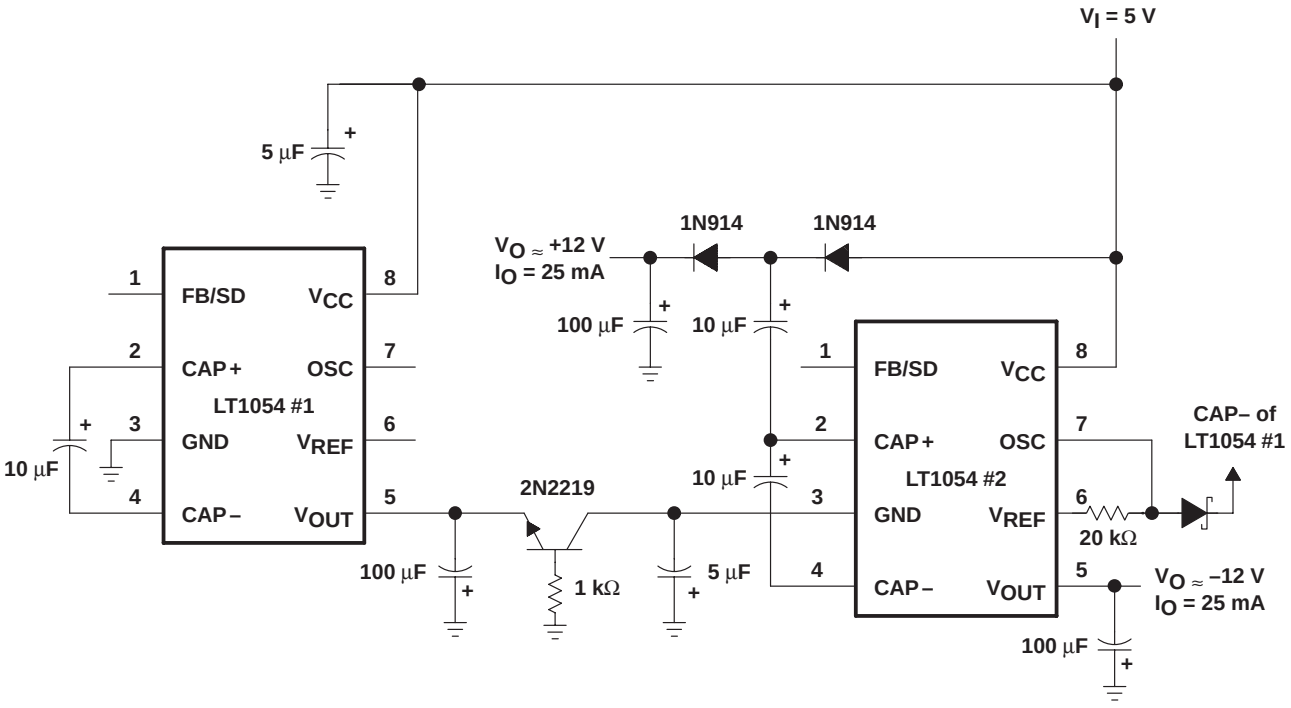


Figure 24. 5-V to ±12-V Converter

APPLICATION INFORMATION

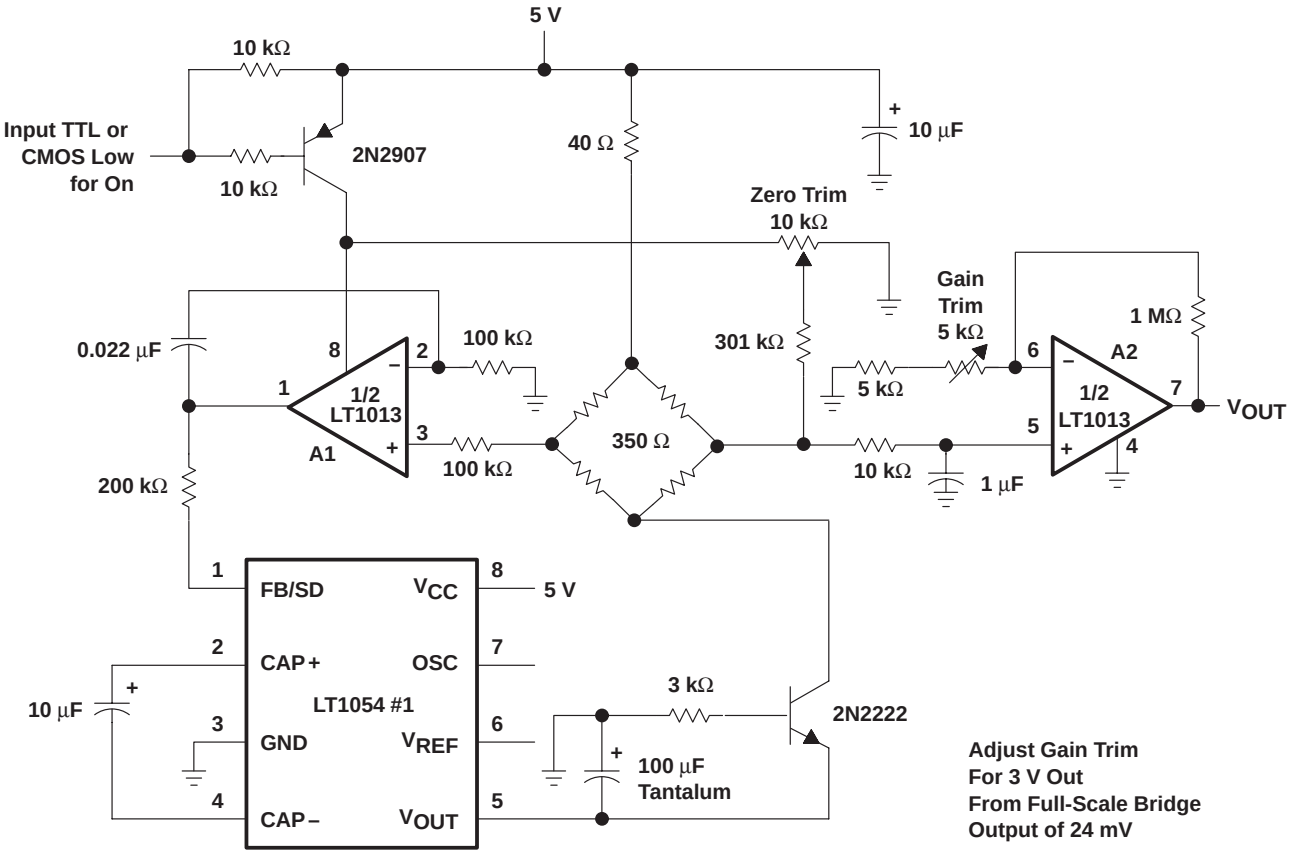
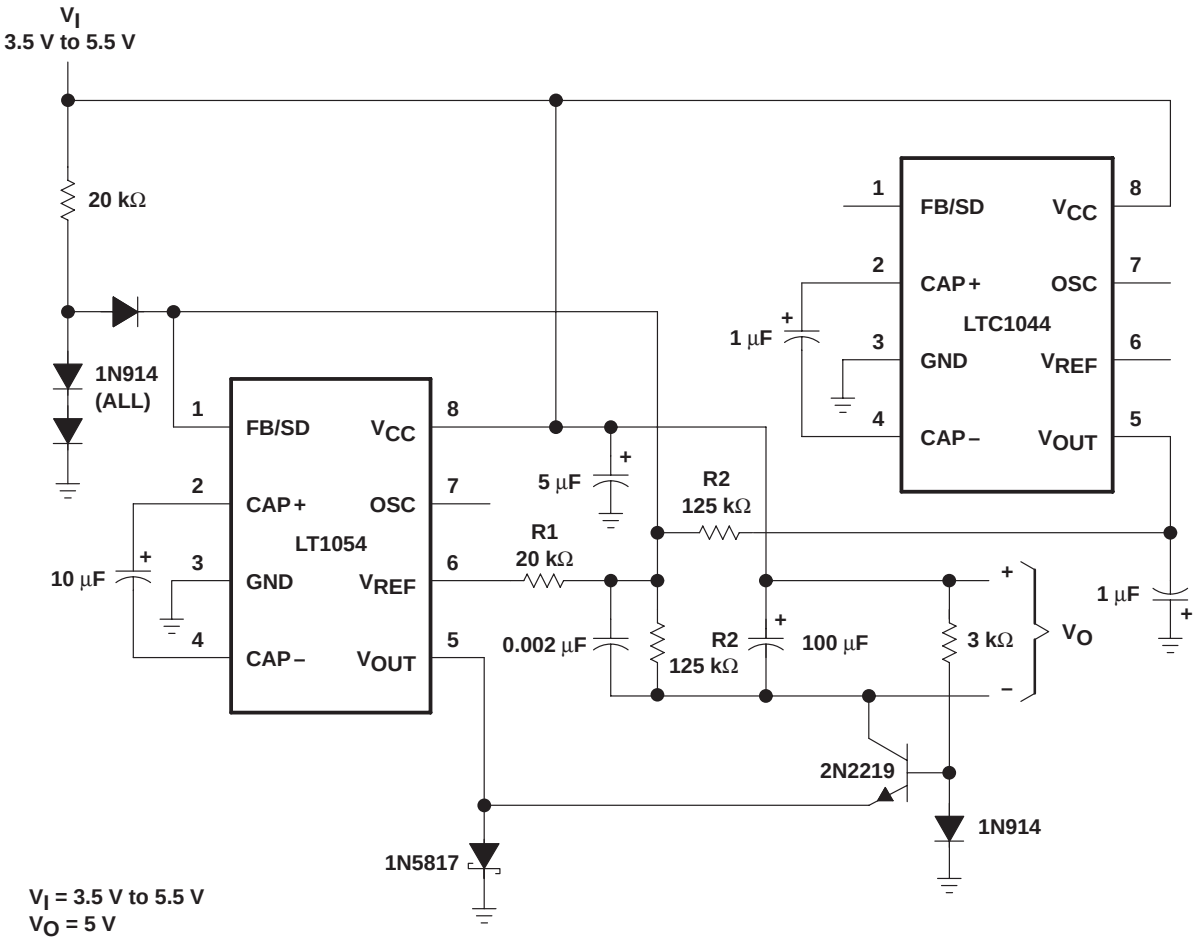


Figure 25. Strain-Gage Bridge Signal Conditioner

APPLICATION INFORMATION

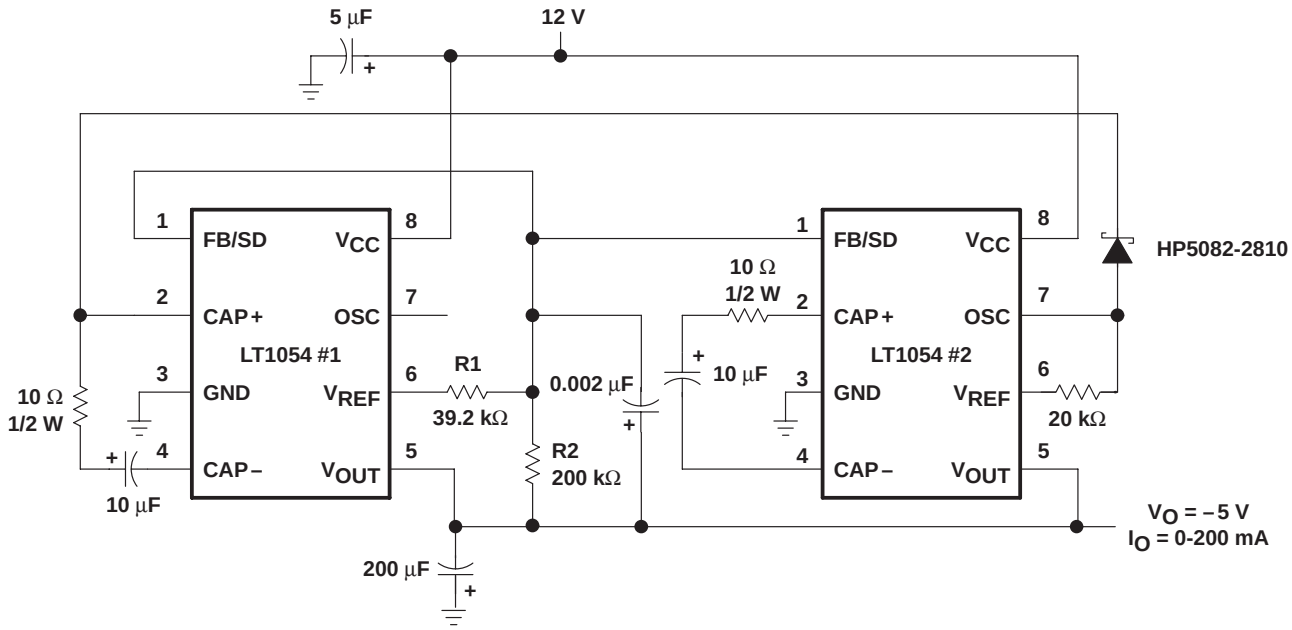


V_I = 3.5 V to 5.5 V
V_O = 5 V
I_O MAX = 50 mA

$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\text{ mV}} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\text{ V}} + 1\right)$$

Figure 26. 3.5-V to 5-V Regulator

APPLICATION INFORMATION



$$R2 = R1\left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1\right) = R1\left(\frac{|V_{OUT}|}{1.21\ V} + 1\right)$$

Figure 27. Regulating 200-mA + 12-V to –5-V Converter

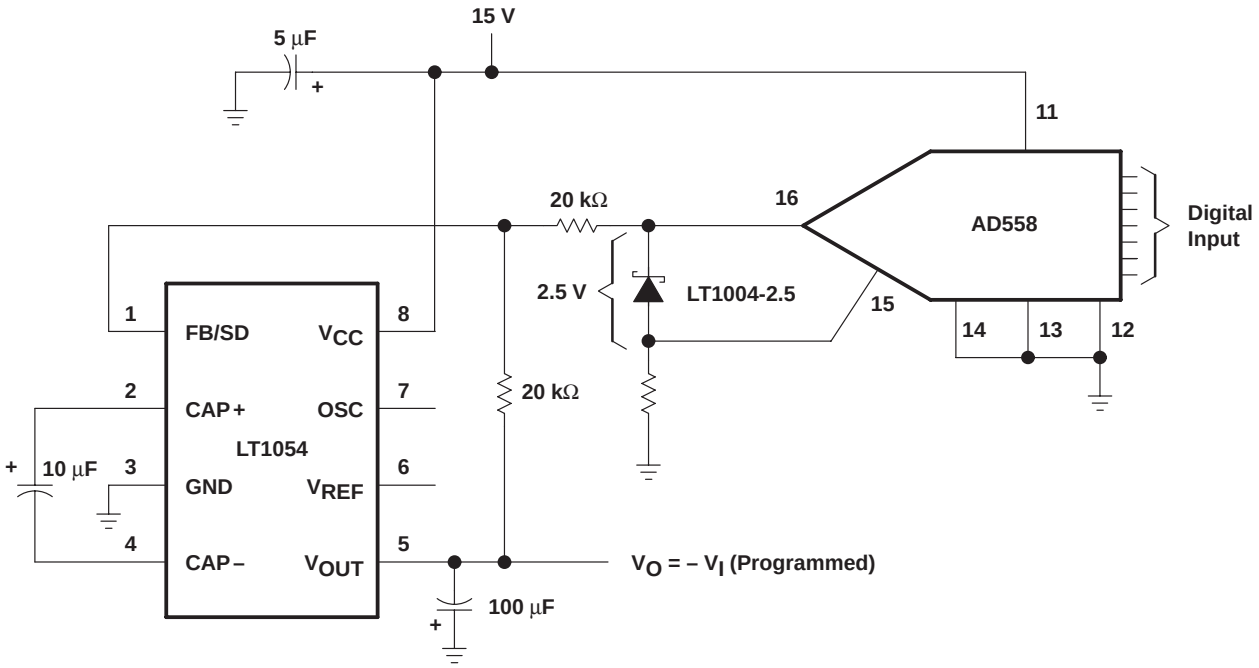


Figure 28. Digitally Programmable Negative Supply

APPLICATION INFORMATION

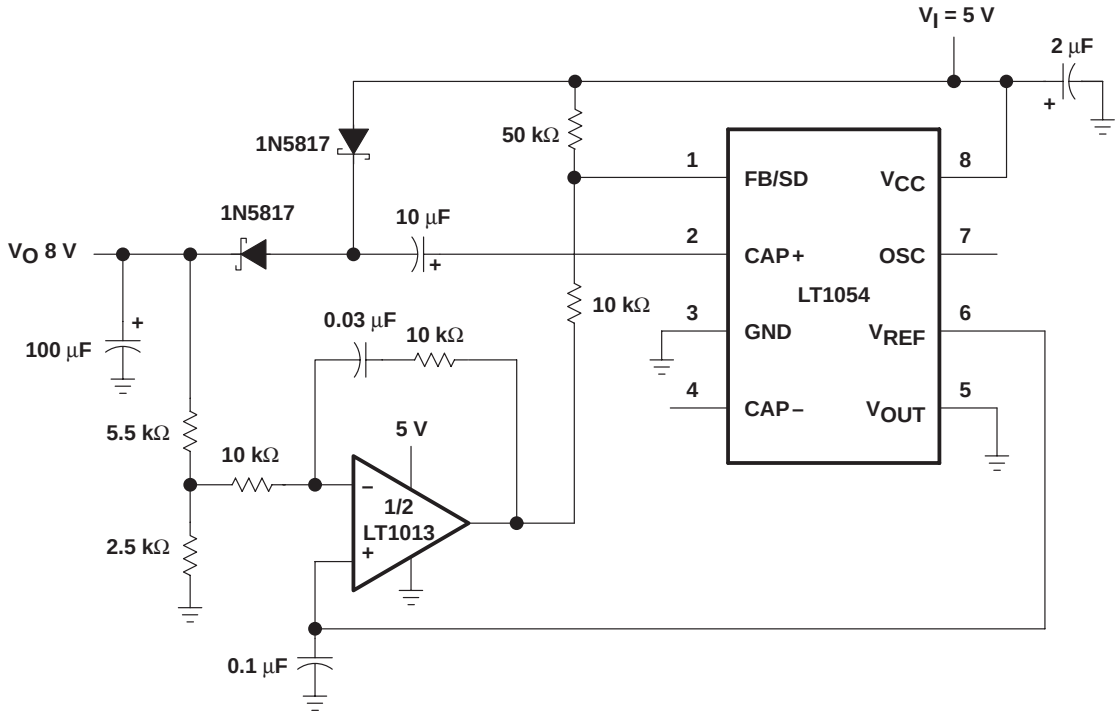
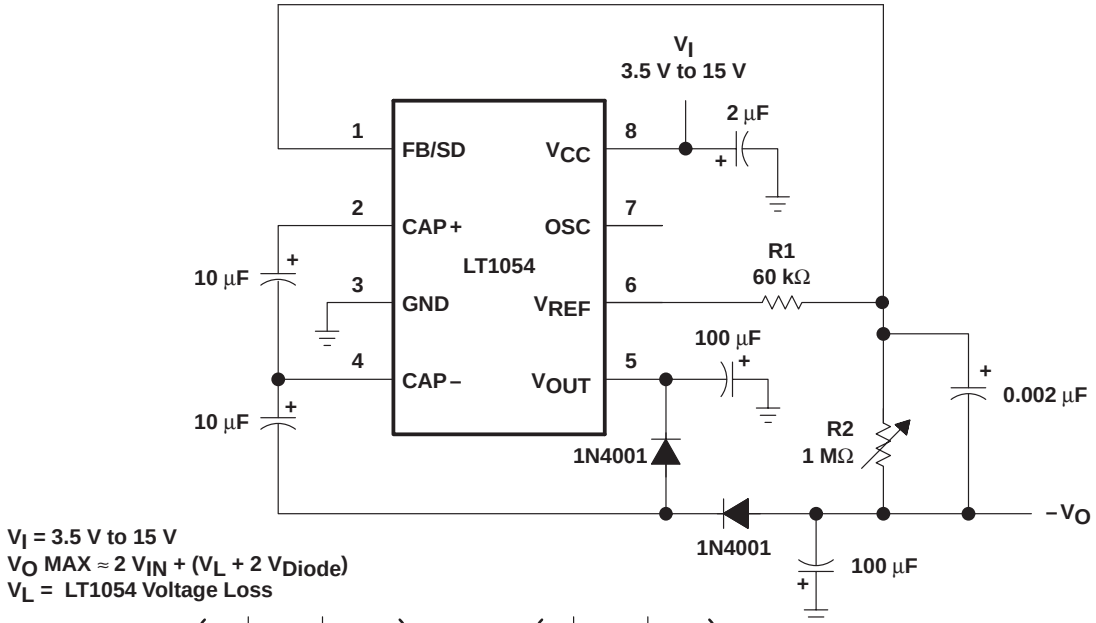


Figure 29. Positive Doubler With Regulation (5-V to 8-V Converter)



V_I = 3.5 V to 15 V
V_O MAX ≈ 2 V_{IN} + (V_L + 2 V_{Diode})
V_L = LT1054 Voltage Loss

$$R2 = R1 \left(\frac{|V_{OUT}|}{\frac{V_{REF}}{2} - 40\ mV} + 1 \right) = R1 \left(\frac{|V_{OUT}|}{1.21\ V} + 1 \right)$$

Figure 30. Negative Doubler With Regulator

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