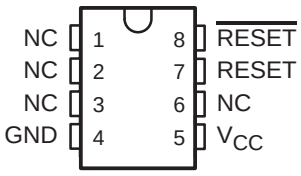
- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Input Threshold Voltage . . . 4.55 V ±120 mV**
- **Low Standby Current . . . 20 μA**
- **Reset Outputs Defined When V_{CC} Exceeds 1 V**
- **True and Complementary Reset Outputs**
- **Wide Supply Voltage Range . . . 1 V to 7 V**

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL7759C is a monolithic supply-voltage supervisor designed for use as a reset controller in microcomputer and microprocessor systems. The supervisor monitors the supply voltage for undervoltage conditions. During power up, when the supply voltage, V_{CC}, attains a value approaching 1 V, the RESET and $\overline{\text{RESET}}$ outputs become active (high and low, respectively) to prevent undefined operation. If at any time the supply voltage drops below the input threshold voltage level (V_{IT-}), the reset outputs go to the reset active state until the supply voltage has returned to its nominal value (see timing diagram).

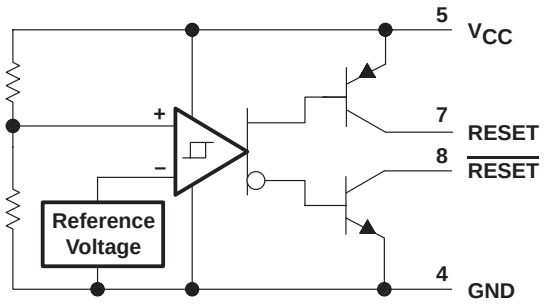
The TL7759C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	2.5 mV	TL7759CD	TLC7759CP	TL7759Y

The D packages are available taped and reeled. Add R suffix to device type (e.g., TL7759CDR). Chips are tested at 25°C.

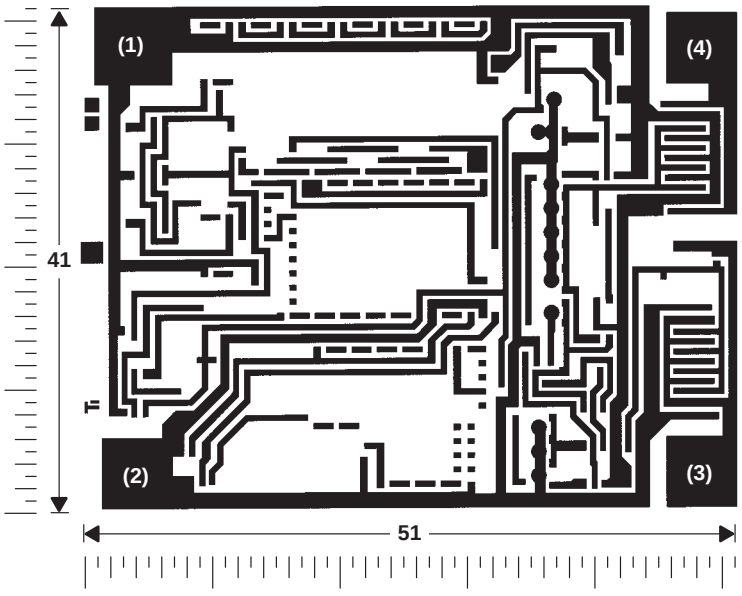
functional block diagram

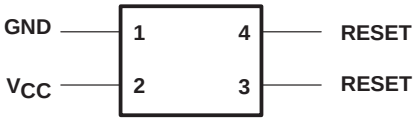


TL7759Y chip information

This chip, when properly assembled, displays characteristics similar to the TL7759C. Thermal compression or ultrasonic bonding can be used on the doped-aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TERMINALS 1, 2, 3, AND 6 ARE NOT CONNECTED.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 20 V
Off-state output voltage range: $\overline{\text{RESET}}$ voltage . . . . . –0.3 V to 20 V
RESET voltage . . . . . –0.3 V to 20 V
Low-level output current, I_{OL} ($\overline{\text{RESET}}$) . . . . . 30 mA
High-level output current, I_{OH} (RESET) . . . . . –10 mA
Package thermal impedance, θJ_A (see Note 2): D package . . . . . 197°C
P package . . . . . 104°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		1	7	V
Output voltage, V_O (see Note 3)	Transistor off $\overline{\text{RESET}}$ voltage		15	V
	Transistor off RESET voltage	0		
Low-level output current, I_{OL}	$\overline{\text{RESET}}$		24	mA
High-level output current, I_{OH}	RESET		–8	
Operating free-air temperature, T_A		0	70	°C

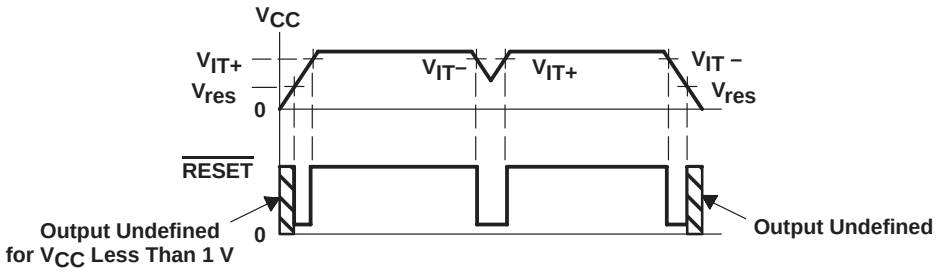
NOTE 3: RESET output must not be pulled down below GND potential.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TL7759C MIN	TL7759C TYP‡	TL7759C MAX	UNIT
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	V_{CC} = 4.3 V	I_{OL} = 24 mA		0.4	0.8	V
V_{OH}	High-level output voltage	RESET		I_{OH} = –8 mA	V_{CC}–1			V
$V_{IT–}$	Input threshold voltage (negative-going V_{CC})		T_A = 25°C		4.43	4.55	4.67	V
			T_A = 0°C to 70°C		4.4		4.7	
V_{res}§	Power-up reset voltage		R_L = 2.2 kΩ	T_A = 25°C		0.8	1	V
				T_A = 0°C to 70°C			1.2	
V_{hys}¶	Hysteresis at V_{CC} input		T_A = 25°C		40	50	60	mV
			T_A = 0°C to 70°C		30		70	mV
I_{OH}	High-level output current	$\overline{\text{RESET}}$	V_{CC} = 7 V, See Figure 1	V_{OH} = 15 V			1	µA
I_{OL}	Low-level output current	RESET		V_{OL} = 0 V			–1	µA
I_{CC}	Supply current		No load	V_{CC} = 4.3 V		1400	2000	µA
				V_{CC} = 5.5 V			40	

‡ Typical values are at T_A = 25°C.
§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active, V_{CC} slew rate ≤ 5 V/µs.
¶ This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, $V_{IT–}$.

timing diagram



switching characteristics at T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7759C MIN	TL7759C MAX	UNIT
t_{PLH}	Propagation delay time, low-to high-level output	V_{CC}	RESET	See Figures 2 and 3†		5	µs
t_{PHL}	Propagation delay time, high-to low-level output	V_{CC}	$\overline{\text{RESET}}$	See Figures 2 and 4		5	µs
t_r	Rise time		$\overline{\text{RESET}}$	See Figures 2 and 4†		1	µs
t_f	Fall time		$\overline{\text{RESET}}$	See Figures 2 and 4		1	µs
$t_{w(min)}$	Minimum pulse duration	V_{CC}	$\overline{\text{RESET}}$	See Figures 2 and 4	5		µs

† V_{CC} slew rate ≤ 5 V/µs

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TL7759Y MIN	TL7759Y TYP	TL7759Y MAX	UNIT
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	V_{CC} = 4.3 V, I_{OL} = 24 mA		0.4		V
V_{IT-}	Input threshold voltage (negative-going V_{CC})				4.55		V
V_{res}‡	Power-up reset voltage		R_L = 2.2 kΩ		0.8		V
V_{hys}§	Hysteresis at V_{CC} input				50		mV
I_{CC}	Supply current		V_{CC} = 4.3 V, No load		1400		µA

‡ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active, V_{CC} slew rate ≤ 5 V/µs.
§ This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.

PARAMETER MEASUREMENT INFORMATION

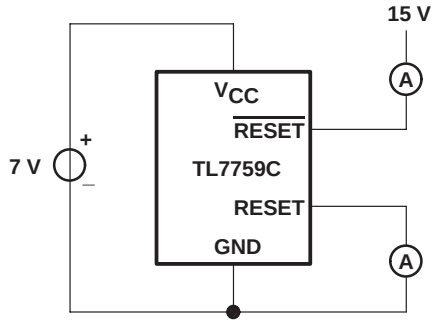
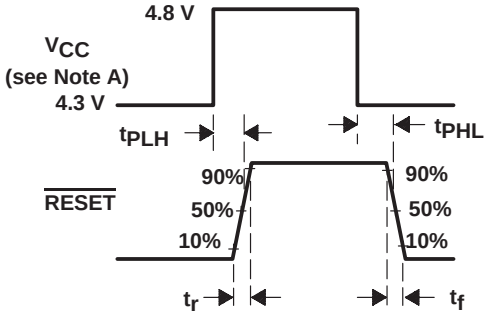
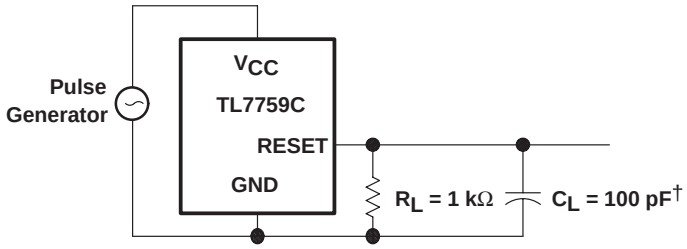


Figure 1. Test Circuit for Output Leakage Current



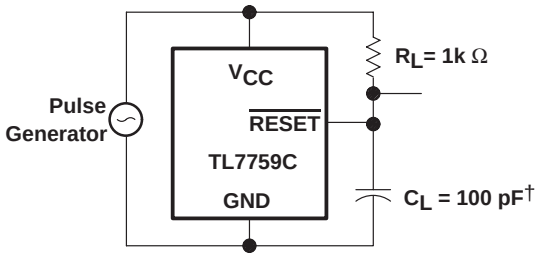
NOTE A: V_{CC} slew rate ≤ 5 V/μs.

Figure 2. Switching Diagram



† C_L Includes jig and probe capacitance.

Figure 3. Test Circuit for RESET Output Switching Characteristics



† C_L Includes jig and probe capacitance.

Figure 4. Test Circuit for $\overline{\text{RESET}}$ Output Switching Characteristics

APPLICATION INFORMATION

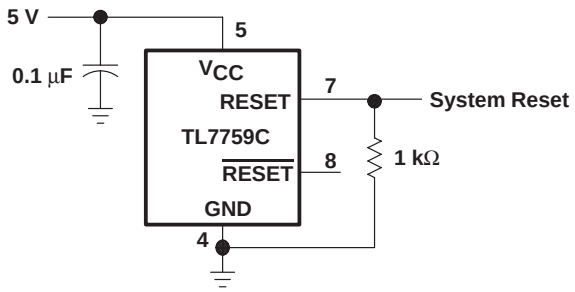


Figure 5. Power-Supply System Reset Generation