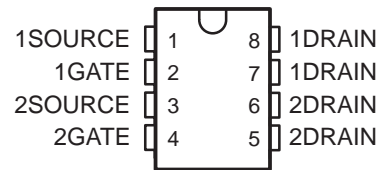


TPS1120, TPS1120Y DUAL P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS080A – MARCH 1994 – REVISED AUGUST 1995

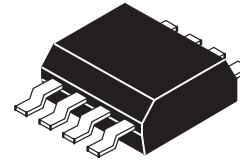
- Low $r_{DS(on)}$. . . 0.18 Ω at $V_{GS} = -10$ V
- 3-V Compatible
- Requires No External V_{CC}
- TTL and CMOS Compatible Inputs
- $V_{GS(th)} = -1.5$ V Max
- ESD Protection Up to 2 kV per MIL-STD-883C, Method 3015

**D PACKAGE
(TOP VIEW)**



description

The TPS1120 incorporates two independent p-channel enhancement-mode MOSFETs that have been optimized, by means of the Texas Instruments LinBiCMOS™ process, for 3-V or 5-V power distribution in battery-powered systems. With a maximum $V_{GS(th)}$ of -1.5 V and an I_{DSS} of only $0.5 \mu A$, the TPS1120 is the ideal high-side switch for low-voltage portable battery-management systems, where maximizing battery life is a primary concern. Because portable equipment is potentially subject to electrostatic discharge (ESD), the MOSFETs have built-in circuitry for 2-kV ESD protection. End equipment for the TPS1120 includes notebook computers, personal digital assistants (PDAs), cellular telephones, bar-code scanners, and PCMCIA cards. For existing designs, the TPS1120D has a pinout common with other p-channel MOSFETs in small-outline integrated circuit SOIC packages.



The TPS1120 is characterized for an operating junction temperature range, T_J , from $-40^\circ C$ to $150^\circ C$.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES†	CHIP FORM (Y)
	SMALL OUTLINE (D)	
$-40^\circ C$ to $150^\circ C$	TPS1120D	TPS1120Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1120DR). The chip form is tested at $25^\circ C$.



Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

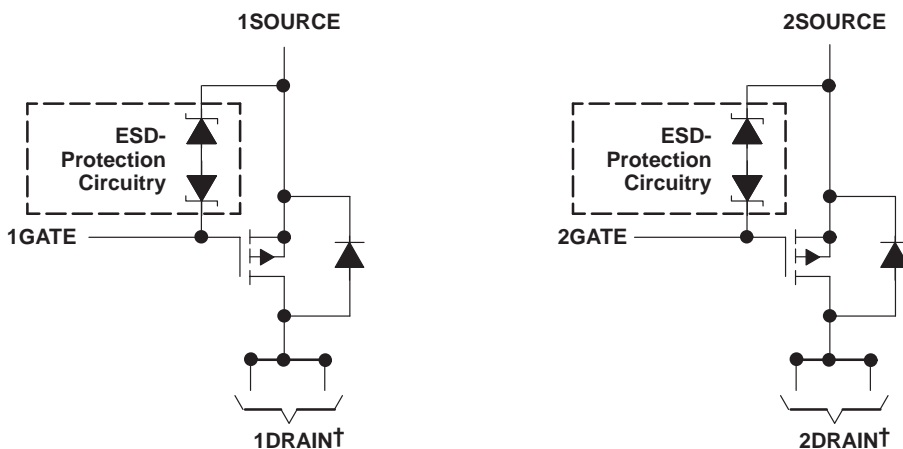
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated

TPS1120, TPS1120Y DUAL P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS080A – MARCH 1994 – REVISED AUGUST 1995

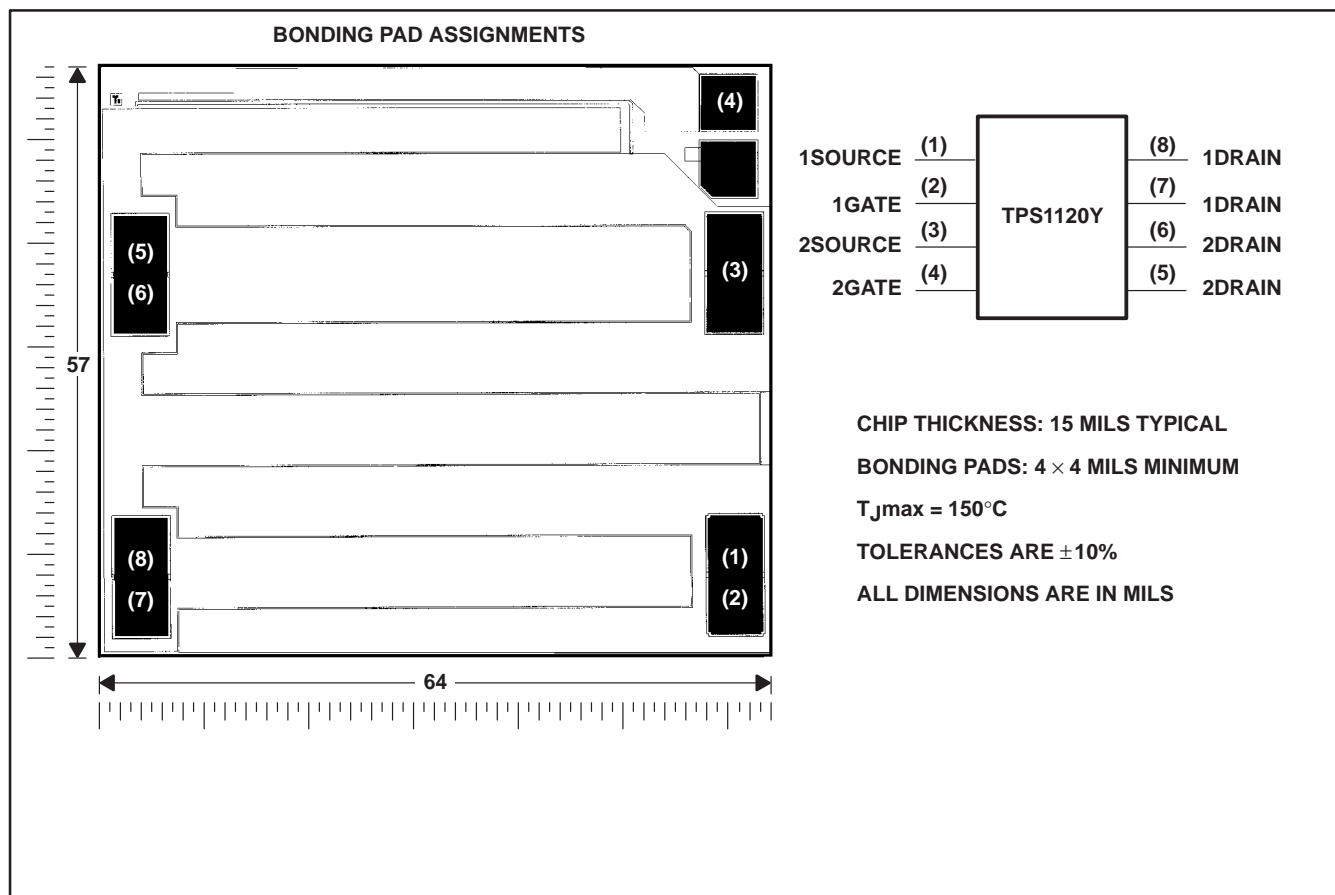
schematic



† For all applications, both drain pins for each device should be connected.

TPS1120Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1120C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.



TPS1120, TPS1120Y

DUAL P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS080A – MARCH 1994 – REVISED AUGUST 1995

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

			UNIT
Drain-to-source voltage, V_{DS}		-15	V
Gate-to-source voltage, V_{GS}		2 or -15	V
Continuous drain current, each device ($T_J = 150^\circ\text{C}$), I_D	$V_{GS} = -2.7\text{ V}$	$T_A = 25^\circ\text{C}$	± 0.39
		$T_A = 125^\circ\text{C}$	± 0.21
	$V_{GS} = -3\text{ V}$	$T_A = 25^\circ\text{C}$	± 0.5
		$T_A = 125^\circ\text{C}$	± 0.25
	$V_{GS} = -4.5\text{ V}$	$T_A = 25^\circ\text{C}$	± 0.74
		$T_A = 125^\circ\text{C}$	± 0.34
$V_{GS} = -10\text{ V}$	$T_A = 25^\circ\text{C}$	± 1.17	
	$T_A = 125^\circ\text{C}$	± 0.53	
Pulse drain current, I_D		$T_A = 25^\circ\text{C}$	± 7
Continuous source current (diode conduction), I_S		$T_A = 25^\circ\text{C}$	-1
Continuous total power dissipation		See Dissipation Rating Table	
Storage temperature range, T_{stg}		-55 to 150	$^\circ\text{C}$
Operating junction temperature range, T_J		-40 to 150	$^\circ\text{C}$
Operating free-air temperature range, T_A		-40 to 125	$^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	$^\circ\text{C}$

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR [‡] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	840 mW	6.71 mW/ $^\circ\text{C}$	538 mW	437 mW	169 mW

[‡] Maximum values are calculated using a derating factor based on $R_{\theta JA} = 149^\circ\text{C}/\text{W}$ for the package. These devices are mounted on an FR4 board with no special thermal considerations.

TPS1120, TPS1120Y

DUAL P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS080A – MARCH 1994 – REVISED AUGUST 1995

electrical characteristics at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

static

PARAMETER	TEST CONDITIONS	TPS1120			UNIT
		MIN	TYP	MAX	
$V_{GS(th)}$ Gate-to-source threshold voltage	$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$	-1	-1.25	-1.50	V
V_{SD} Source-to-drain voltage (diode forward voltage) [†]	$I_S = -1 \text{ A}$, $V_{GS} = 0 \text{ V}$	-0.9			V
I_{GSS} Reverse gate current, drain short circuited to source	$V_{DS} = 0 \text{ V}$, $V_{GS} = -12 \text{ V}$	±100			nA
I_{DSS} Zero-gate-voltage drain current	$V_{DS} = -12 \text{ V}$, $V_{GS} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$	-0.5		μA
		$T_J = 125^\circ\text{C}$	-10		
$r_{DS(on)}$ Static drain-to-source on-state resistance [†]	$V_{GS} = -10 \text{ V}$	$I_D = -1.5 \text{ A}$	180		m Ω
	$V_{GS} = -4.5 \text{ V}$	$I_D = -0.5 \text{ A}$	291 400		
	$V_{GS} = -3 \text{ V}$	$I_D = -0.2 \text{ A}$	476 700		
	$V_{GS} = -2.7 \text{ V}$		606 850		
g_{fs} Forward transconductance [†]	$V_{DS} = -10 \text{ V}$, $I_D = -2 \text{ A}$	2.5			S

[†] Pulse test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$

static

PARAMETER	TEST CONDITIONS	TPS1120Y			UNIT
		MIN	TYP	MAX	
$V_{GS(th)}$ Gate-to-source threshold voltage	$V_{DS} = V_{GS}$, $I_D = -250 \mu\text{A}$	-1.25			V
V_{SD} Source-to-drain voltage (diode forward voltage) [†]	$I_S = -1 \text{ A}$, $V_{GS} = 0 \text{ V}$	-0.9			V
$r_{DS(on)}$ Static drain-to-source on-state resistance [†]	$V_{GS} = -10 \text{ V}$	$I_D = -1.5 \text{ A}$	180		m Ω
	$V_{GS} = -4.5 \text{ V}$	$I_D = -0.5 \text{ A}$	291		
	$V_{GS} = -3 \text{ V}$	$I_D = -0.2 \text{ A}$	476		
	$V_{GS} = -2.7 \text{ V}$		606		
g_{fs} Forward transconductance [†]	$V_{DS} = -10 \text{ V}$, $I_D = -2 \text{ A}$	2.5			S

[†] Pulse test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$

dynamic

PARAMETER	TEST CONDITIONS	TPS1120, TPS1120Y			UNIT
		MIN	TYP	MAX	
Q_g Total gate charge	$V_{DS} = -10 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -1 \text{ A}$	5.45			nC
Q_{gs} Gate-to-source charge		0.87			
Q_{gd} Gate-to-drain charge		1.4			
$t_{d(on)}$ Turn-on delay time	$V_{DD} = -10 \text{ V}$, $R_L = 10 \Omega$, $R_G = 6 \Omega$, See Figures 1 and 2, $I_D = -1 \text{ A}$,	4.5			ns
$t_{d(off)}$ Turn-off delay time		13			ns
t_r Rise time		10			ns
t_f Fall time		2			
$t_{rr(SD)}$ Source-to-drain reverse recovery time		$I_F = 5.3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	16		

PARAMETER MEASUREMENT INFORMATION

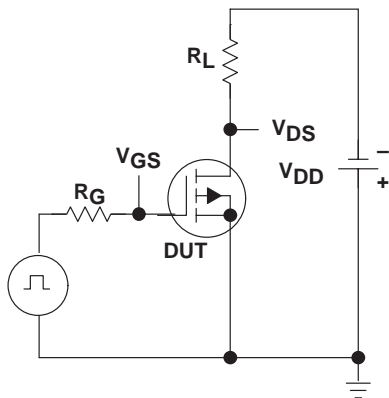


Figure 1. Switching-Time Test Circuit

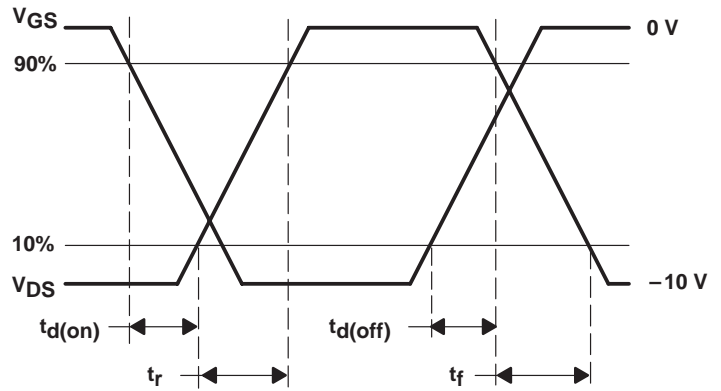


Figure 2. Switching-Time Waveforms

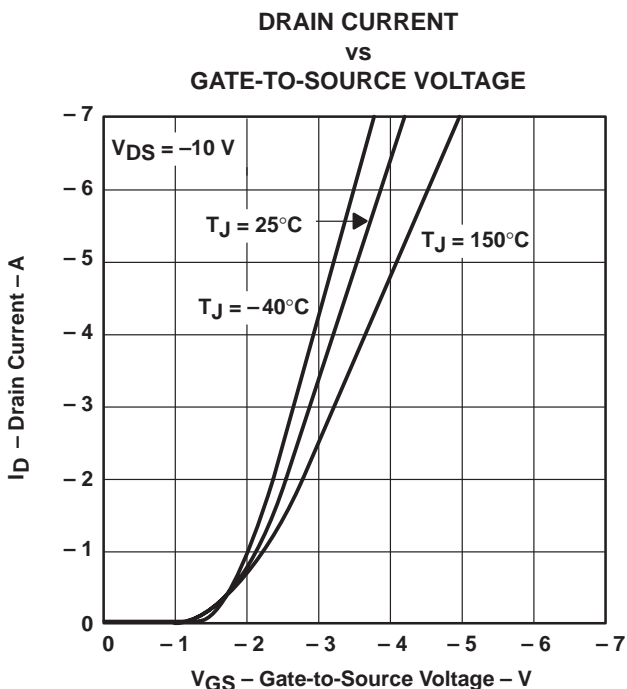
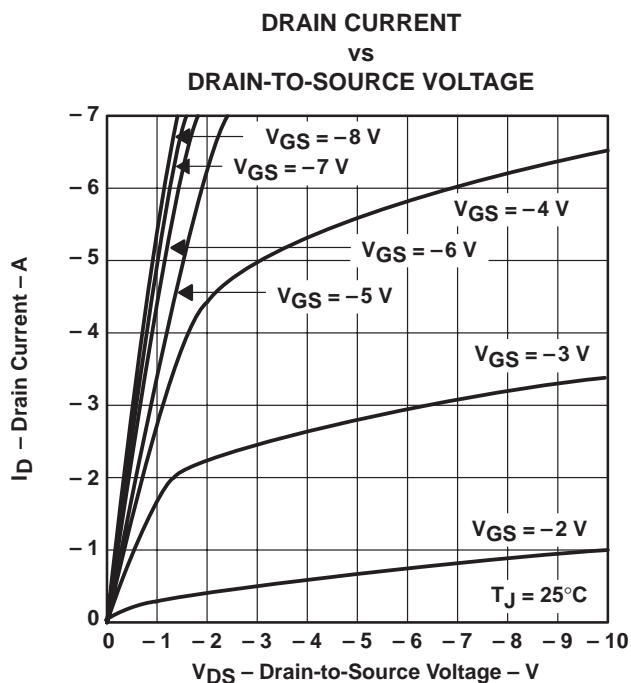
TPS1120, TPS1120Y DUAL P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS080A – MARCH 1994 – REVISED AUGUST 1995

TYPICAL CHARACTERISTICS†

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11



† All characteristics data applies for each independent MOSFET incorporated on the TPS1120.

TYPICAL CHARACTERISTICS

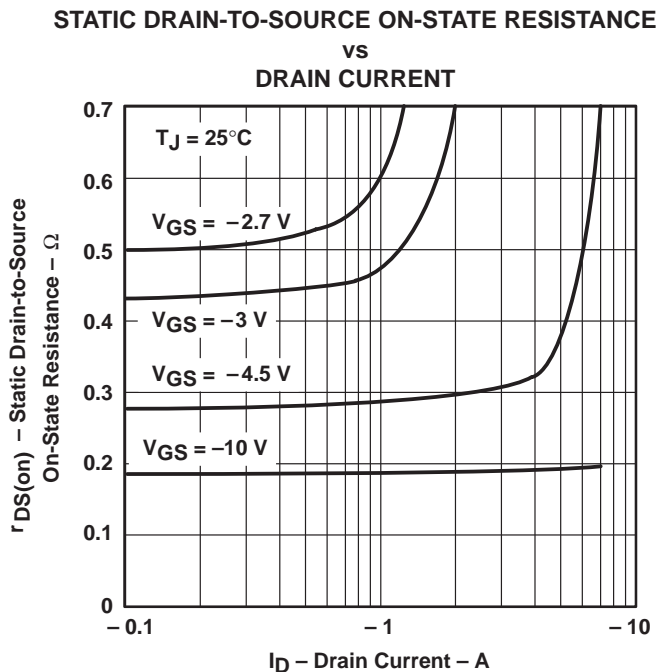
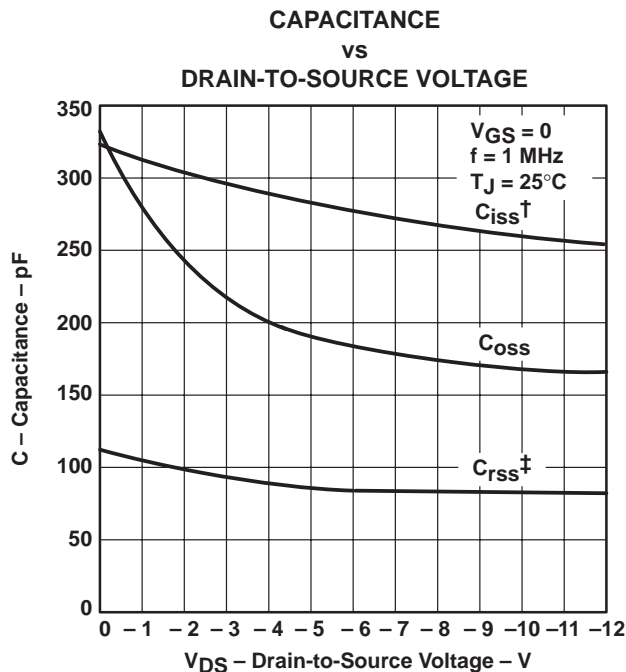


Figure 5



$$^\dagger C_{iss} = C_{gs} + C_{gd}, C_{ds(\text{shorted})}$$

$$^\ddagger C_{rss} = C_{gd}, C_{oss} = C_{ds} + \frac{C_{gs} C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$$

Figure 6

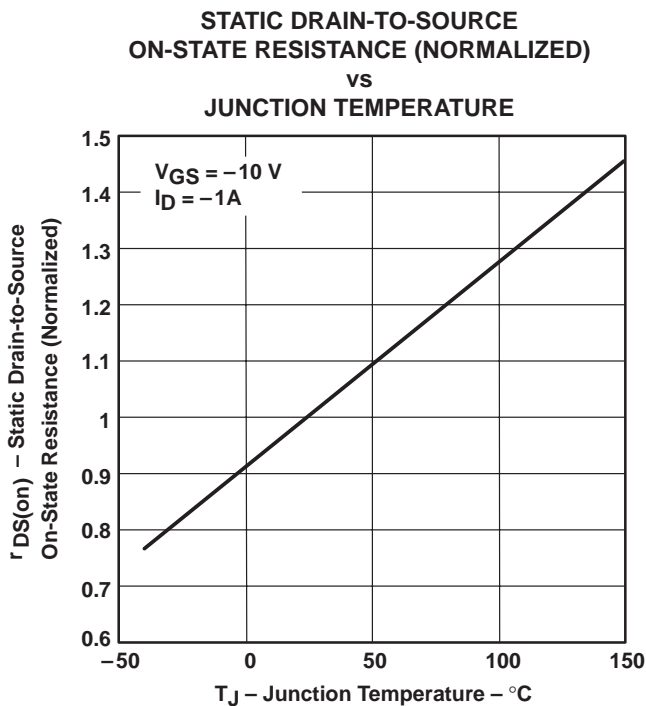


Figure 7

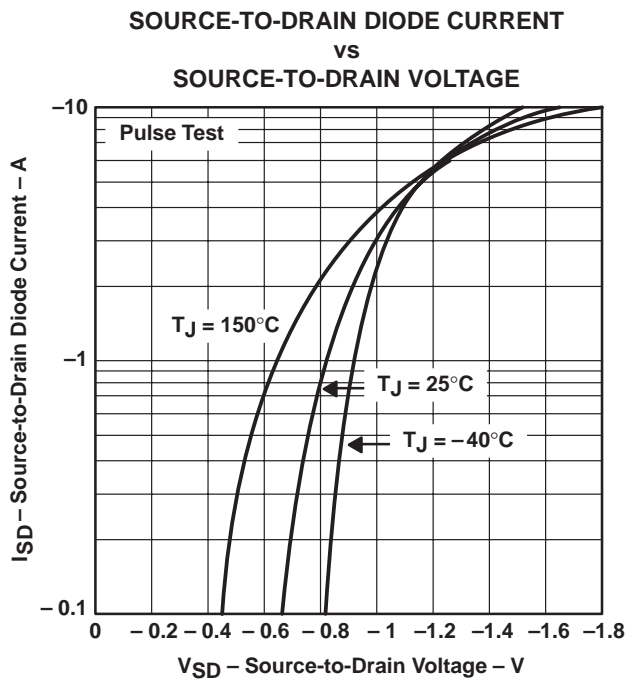


Figure 8

TPS1120, TPS1120Y DUAL P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS080A – MARCH 1994 – REVISED AUGUST 1995

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
GATE-TO-SOURCE VOLTAGE

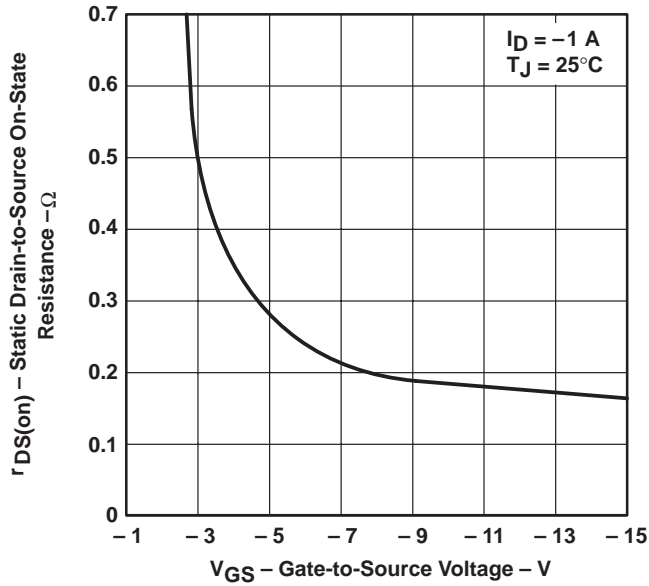


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

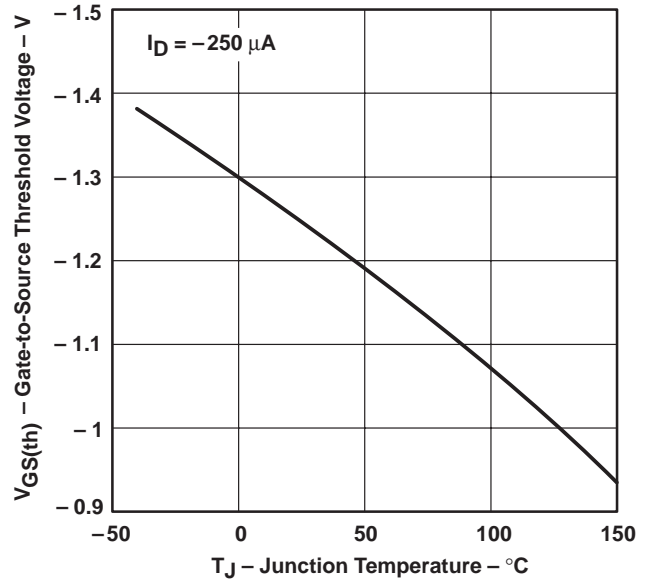


Figure 10

GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

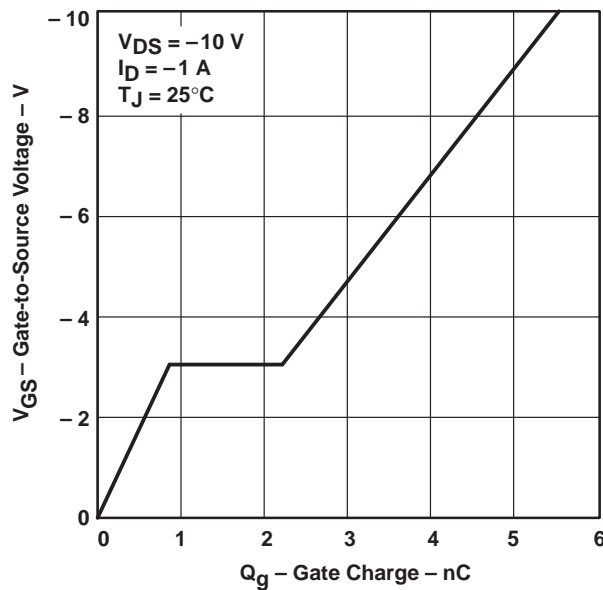
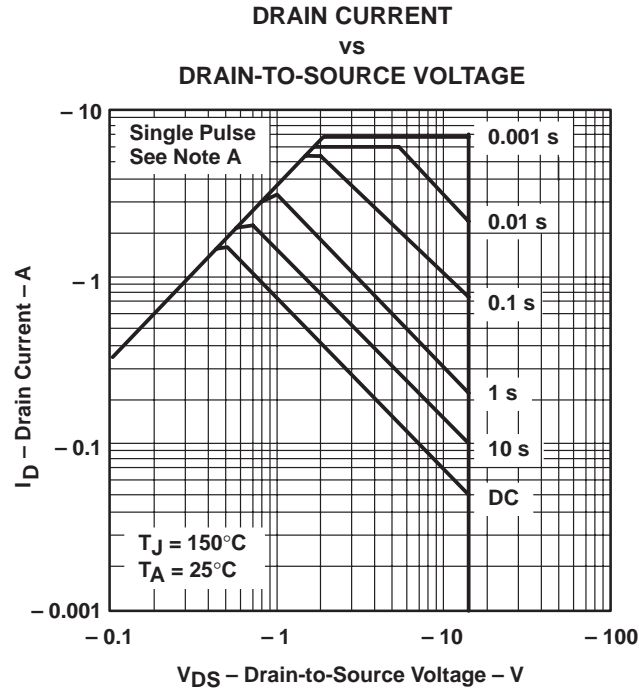


Figure 11



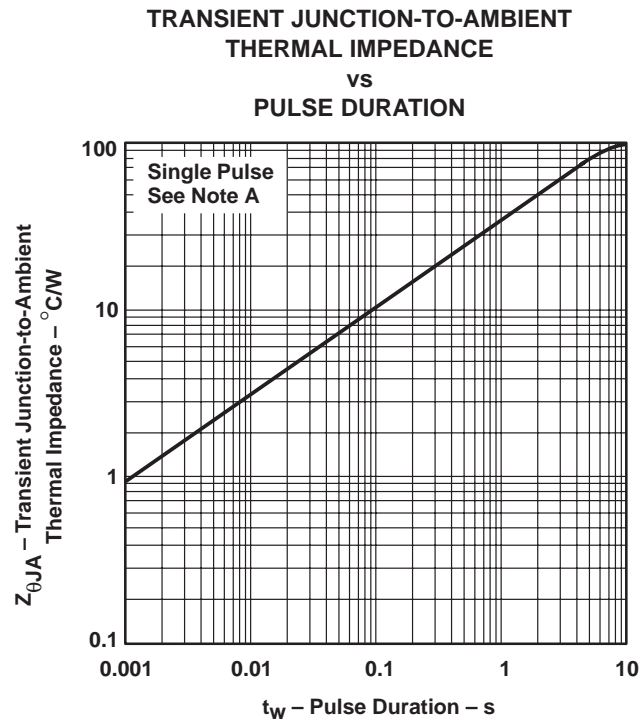
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

THERMAL INFORMATION



NOTE A: FR4-board-mounted only

Figure 12



NOTE A: FR4-board-mounted only

Figure 13

TPS1120, TPS1120Y DUAL P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS080A – MARCH 1994 – REVISED AUGUST 1995

THERMAL INFORMATION

The profile of the heat sinks used for thermal measurements is shown in Figure 14. Board type is FR4 with 1-oz copper and 1-oz tin/lead (63/37) plate. Use of vias or through-holes to enhance thermal conduction was avoided.

Figure 15 shows a family of $R_{\theta JA}$ curves. The $R_{\theta JA}$ was obtained for various areas of heat sinks while subject to air flow. Power remained fixed at 0.25 W per device or 0.50 W per package. This testing was done at 25°C.

As Figure 14 illustrates, there are two separated heat sinks for each package. Each heat sink is coupled to the lead that is internally tied to a single MOSFET source and is half the total area, as shown in Figure 15. For example, if the total area shown in Figure 15 is 4 cm², each heat sink is 2 cm².

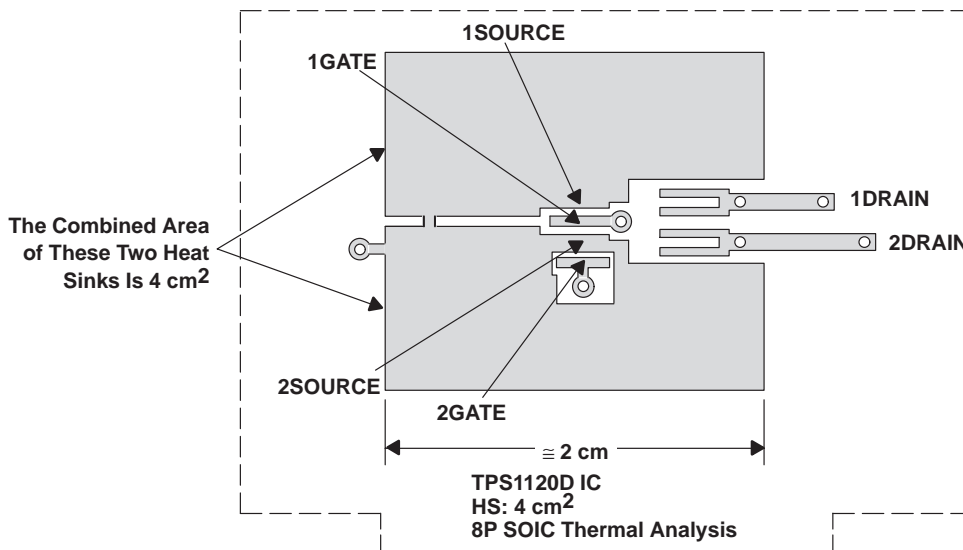


Figure 14. Profile of Heat Sinks

THERMAL RESISTANCE, JUNCTION-TO-AMBIENT vs AIRFLOW, 25°C

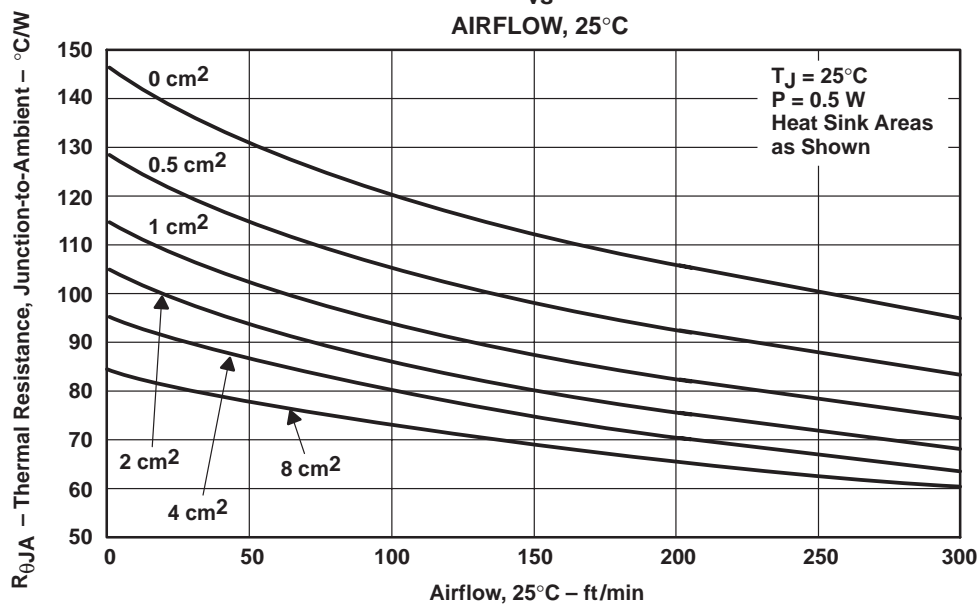


Figure 15

THERMAL INFORMATION

Figure 16 illustrates the thermally enhanced (SO) lead frame. Attaching the two MOSFET dies directly to the source terminals allows maximum heat transfer into a power plane.

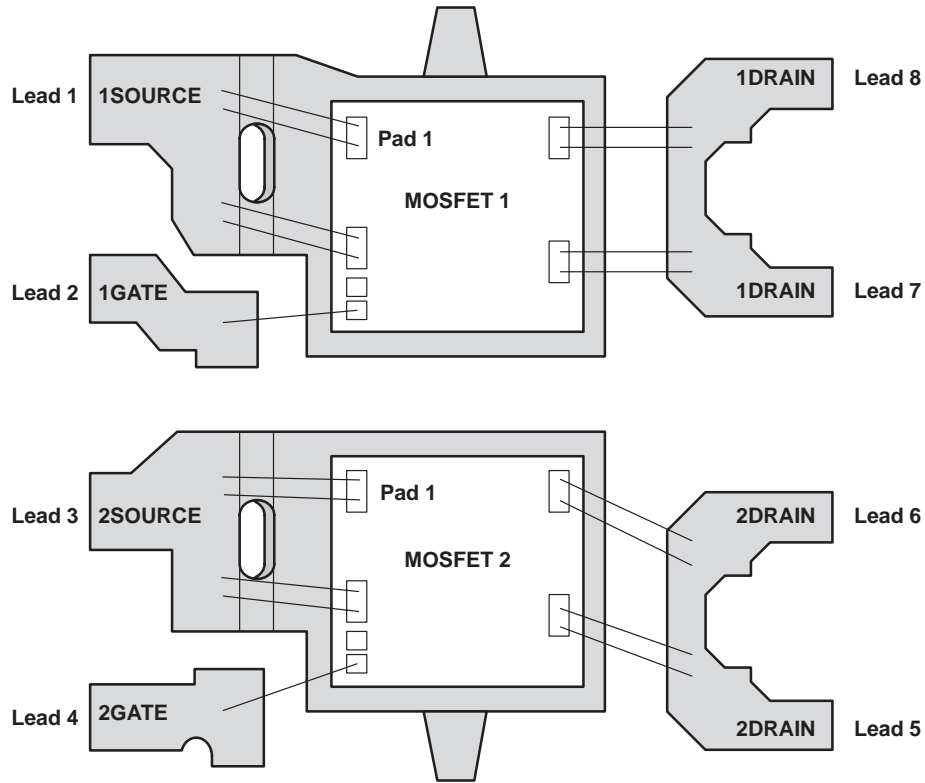


Figure 16. TPS1120 Dual MOSFET SO-8 Lead Frame

APPLICATION INFORMATION

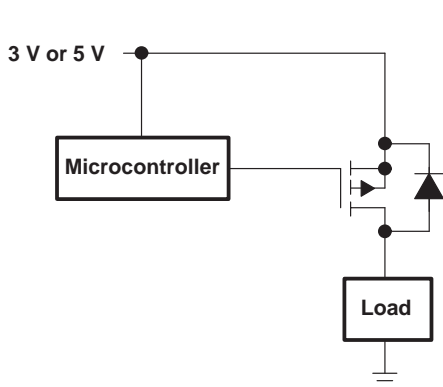


Figure 17. Notebook Load Management

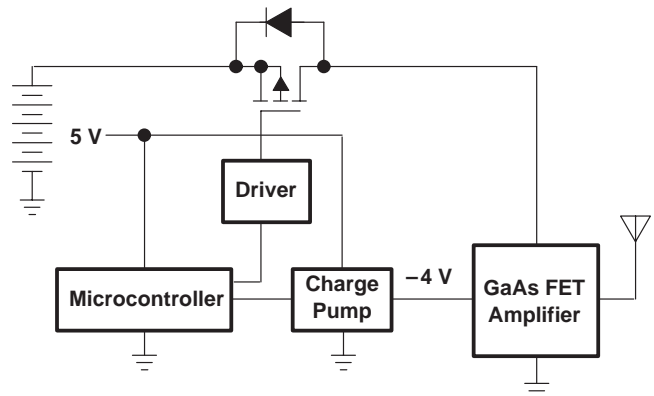


Figure 18. Cellular Phone Output Drive

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.