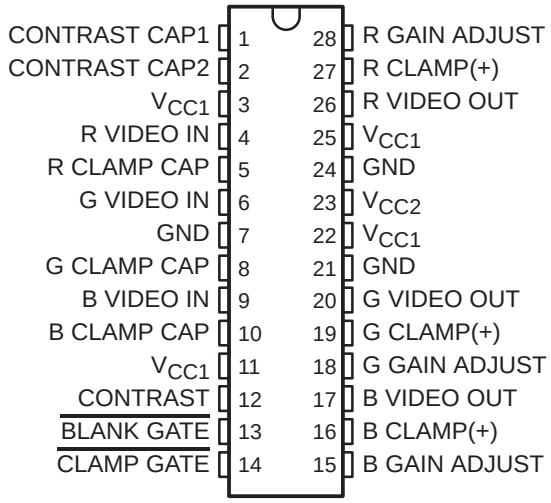
- **Wide Bandwidth . . . Typ 100 MHz at –3 dB**
- **0-V to 4-V Digital Level-Contrast Control Voltage Range**
- **0-V to 4-V Digital Level-Gain Adjust Control Voltage Range**
- **Individual Gain Adjust for Video Amplifiers**
- **Output-Stage Blanking**
- **Fewer Peripheral Components Required Than for Competitive Systems**

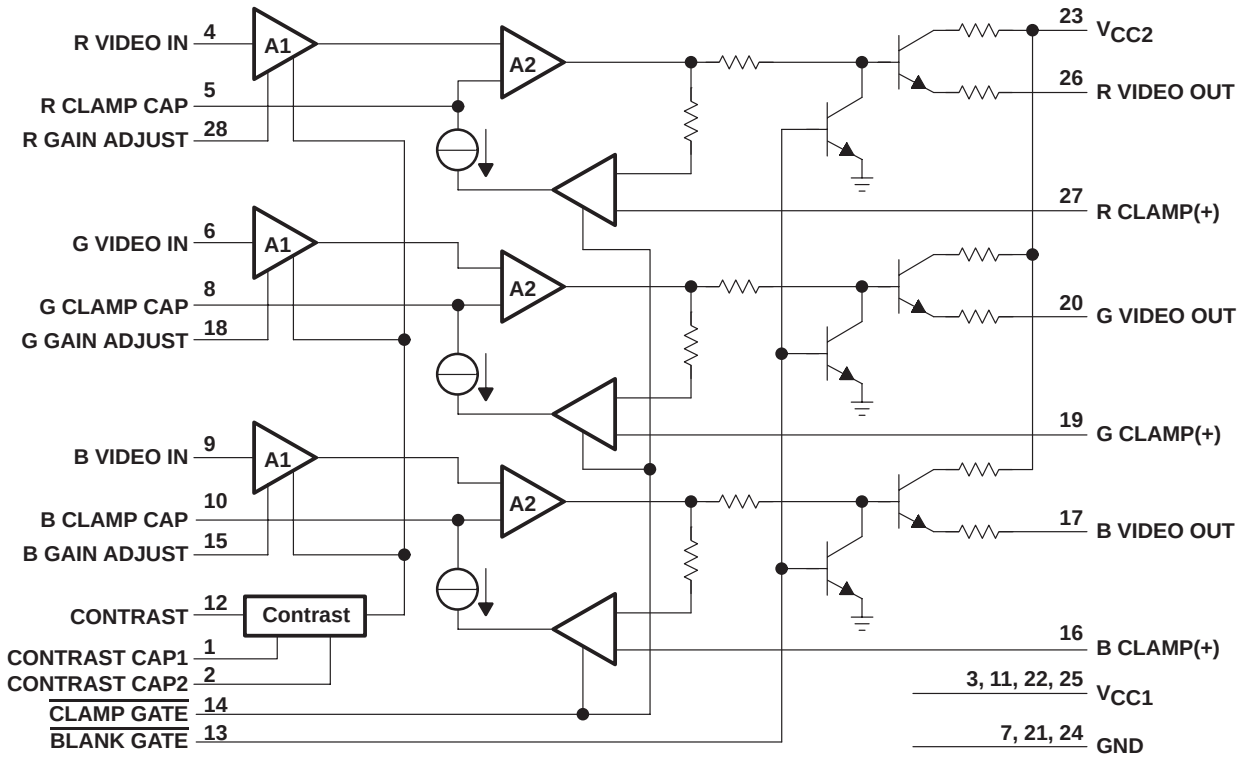
N PACKAGE
(TOP VIEW)



description

The TLS1215 is a wide-band video preamplifier system intended for high-resolution RGB (red-green-blue) color monitors with blanking control features. Each video amplifier (R, G, and B) contains a gain set for adjusting maximum system gain. The TLS1215 provides digital level-operated contrast, brightness, and gain adjustment. All the control inputs offer high input impedance and an operation range from 0 V to 4 V for easy interface to the serial digital buses. The TLS1215 also contains a blanking circuit, which clamps the video output voltage during blanking period to as low as 0.2 V above ground. The device operates from a 12-V supply. The TLS1215 is characterized for operation from 0°C to 70°C.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 13.5 V
Input voltage range, V_I (see Note 1) . . . . . 0 V to V_{CC}
Video output current (per channel) . . . . . 28 mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 2.1 W
Operating virtual junction temperature, T_J . . . . . 150°C
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All V_{CC} pins must be externally wired together to prevent internal damage during V_{CC} power-on/off cycles.
2. For operation above 25°C free-air temperature, derate linearly to 1.5 W at the rate of 13 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1} and V_{CC2}		10.8	12	13.2	V
High-level input voltage, $\overline{\text{CLAMP GATE}}$, V_{IH}	Clamp comparators off	2.4		5	V
Low-level input voltage, $\overline{\text{CLAMP GATE}}$, V_{IL}	Clamp comparators on	0		0.8	V
High-level input voltage, $\overline{\text{BLANK GATE}}$, V_{IH}	Blanking circuit inactive	2.4		5	V
Low-level input voltage, $\overline{\text{BLANK GATE}}$, V_{IL}	Blanking circuit active	0		0.8	V
Operating free-air temperature, T_A		0		70	°C

electrical characteristics at 25°C operating free-air temperature range, $\overline{\text{CLAMP GATE}}$ = 0 V, $\overline{\text{BLANK GATE}}$ = 4 V, CLAMP(+) = 2 V, CONTRAST = R, G, B GAIN ADJUST = 4 V, $V_{CC1} = V_{CC2}$ = 12 V (see Figure 2) (unless otherwise noted)

PARAMETER		ALT SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current		$V_{CC1} + V_{CC2}$	78	90	100	mA
V_{ref}	Video input reference voltage		Measure R, G, B VIDEO IN	2.1	2.3	2.6	V
I_I	Contrast, R, G, B gain adjust input current	I_I	Measure CONTRAST and B, G, R GAIN ADJUST		–1	–2.5	µA
I_{IL}	Clamp gate low input current		$\overline{\text{CLAMP GATE}}$ = 0 V		–1	–2.5	µA
I_{IH}	Clamp gate high input current		$\overline{\text{CLAMP GATE}}$ = 5 V		0.03	1	µA
	Clamp capacitor charge current	$I_{K(chg)}$	R, G, B CLAMP CAP = 0 V		–850		µA
	Clamp capacitor discharge current	$I_{K(dschg)}$	R, G, B CLAMP CAP = 5 V		+850		µA
V_{OL}	Low-level output voltage		R, G, B CLAMP CAP = 0 V		0.3		V
V_{OH}	High-level output voltage		R, G, B CLAMP CAP = 5 V		7.8		V
$V_{O(blanked)}$	Blanked output voltage		Blanking circuit active		0.2		V
$V_{O(diff)}$	Output voltage difference	V_{Odiff}	Between any two channels		±0.5	±50	mV

operating characteristics at 25°C free-air temperature range, $\overline{\text{CLAMP GATE}}$ = 0 V, $\overline{\text{BLANK GATE}}$ = 4 V, CLAMP(+) = 4 V, CONTRAST = R, G, B GAIN ADJUST = 4 V, f_I = 10 kHz (unless otherwise noted)

PARAMETER		ALT SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$A_{V(max)}$	Maximum voltage amplification	A_{VMAX}	CONTRAST = 4 V, $V_{I(PP)}$ = 700 mV		7.8		V/V
$A_{V(mid)}$	Mid-range voltage amplification	A_{VMID}	CONTRAST = 2 V, $V_{I(PP)}$ = 700 mV		2		V/V
	Contrast voltage for minimum amplification	$V_{CONTRASTLOW}$	$V_{I(PP)}$ = 1 V, See Note 3		1		V
	Amplification match at $A_{V(max)}$	$A_{VMAX(DIFF)}$	CONTRAST = 4 V, See Note 4		±0.2		dB
	Amplification match at $A_{V(mid)}$	$A_{VMID(DIFF)}$	CONTRAST = 2 V, See Note 3		±0.2		dB
	Amplification match at $A_{V(low)}$	$A_{VLOW(DIFF)}$	CONTRAST = $V_{CONTRASTLOW}$, See Notes 3 and 4		±0.2		dB
THD	Total harmonic distortion	THD	CONTRAST = 1 V, $V_{I(PP)}$ = 1 V		1.0%		
BW	Amplifier bandwidth	BW(–3 dB)	CONTRAST = 4 V, See Notes 5 and 7		100		MHz
	Crosstalk attenuation	a_X	CONTRAST = 4 V, f = 10 kHz, See Note 6		80		dB
			CONTRAST = 4 V, f = 10 MHz, See Notes 6 or 7		40		dB
	Pulse test	Tr, video Tf, video	$V_{O(PP)}$ = 4 V, CONTRAST = 4 V, Clamp(+) = 2 V, See Notes 5 and 7		4		ns
		Tr, blank Tf, blank	CONTRAST = 4 V , Clamp(+) = 2 V, See Notes 5 and 7		7		

NOTES: 3. Determine $V_{CONTRASTLOW}$ for –40 dB attenuation of output. Reference to A_V maximum.
4. Measure gain difference between any two amplifiers, $V_{I(PP)}$ = 1 V.
5. Adjust input frequency from 10 kHz (A_V maximum ref level) to the –3 dB corner frequency (f–3 dB). $V_{I(PP)}$ = 700 mV.
6. $V_{I(PP)}$ = 700 mV at f = 10 kHz to any amplifier. Measure output levels of the other two undriven amplifiers relative to driven amplifier.
7. A special text fixture without a socket and a double-sided full-ground-plane PC board are required.

APPLICATION INFORMATION

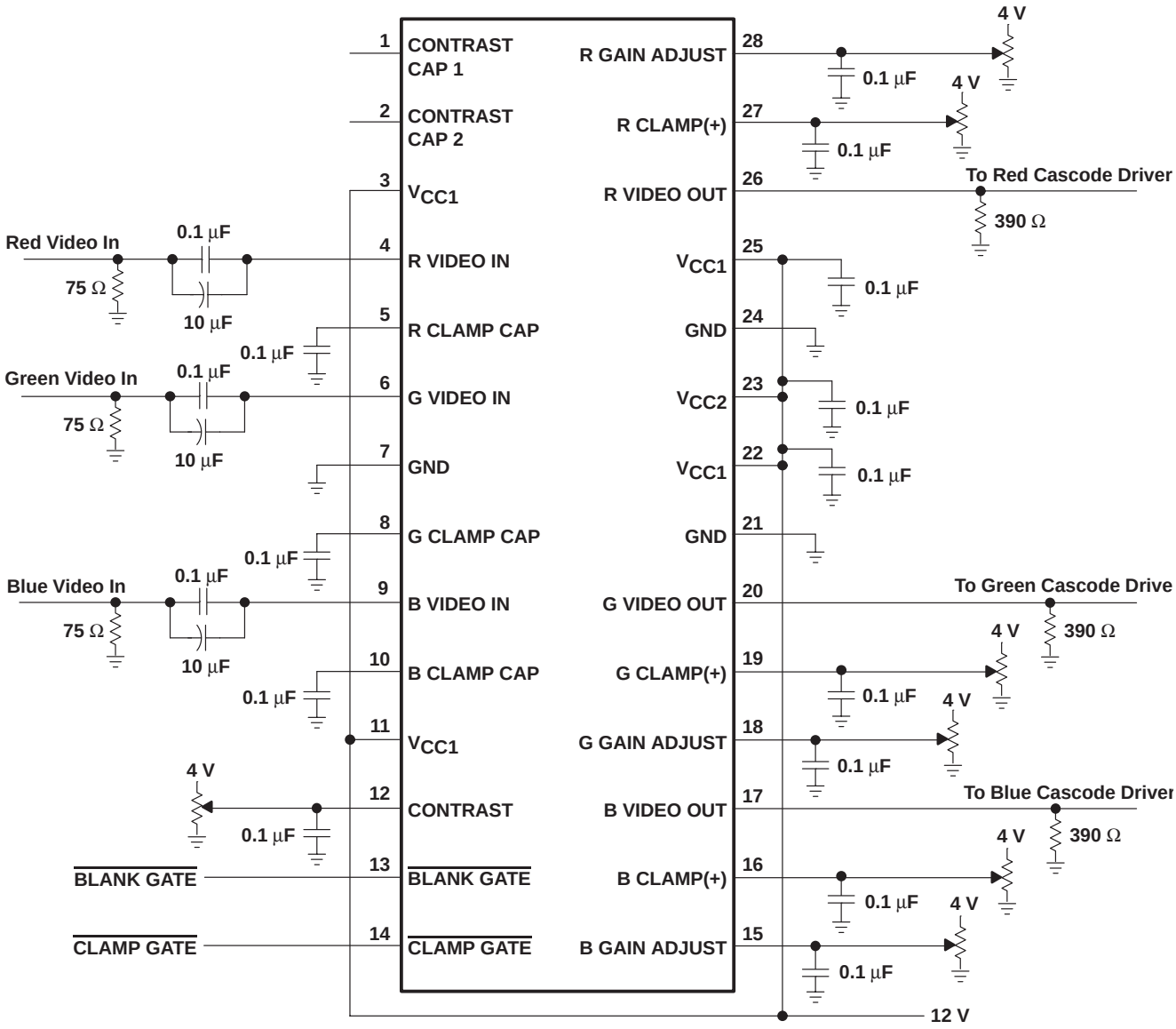
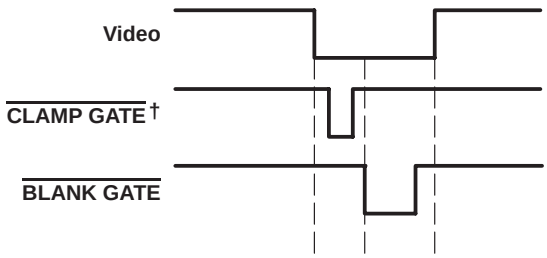


Figure 1. Test/Application Circuit



† Minimum $\overline{\text{CLAMP GATE}}$ pulse: 300 ns

Figure 2. Test/Application Circuit Timing Diagram

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