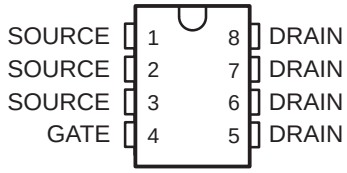
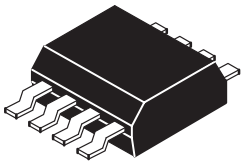
- **Low $r_{DS(on)}$ . . . 65 mΩ Typ at V_{GS} = –4.5 V**
- **High Current Capability**
  6 A at V_{GS} = –4.5 V
- **Logic-Level Gate Drive (3 V Compatible)**
  $V_{GS(th)}$ = –0.9 V Max
- **Low Drain-Source Leakage Current**
  <100 nA From 25°C to 75°C
  at V_{DS} = –6 V
- **Fast Switching . . . 5.8 ns Typ $t_{d(on)}$**
- **Small-Outline Surface-Mount Power Package**

D PACKAGE
(TOP VIEW)





description

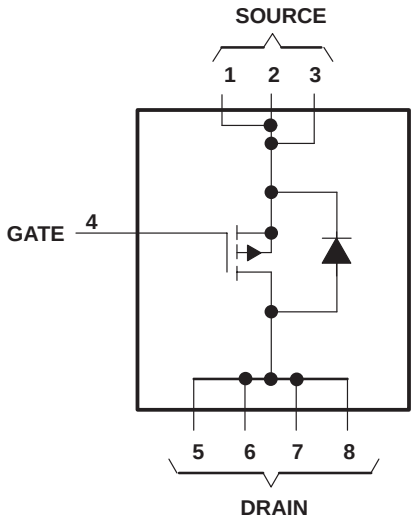
The TPS1110 is a single, low-$r_{DS(on)}$, P-channel enhancement-mode power MOS transistor. The device features extremely low-$r_{DS(on)}$ values coupled with logic-level gate-drive capability and very low drain-source leakage current. With a maximum $V_{GS(th)}$ of –0.9 V and an I_{DSS} of only –100 nA, the TPS1110 is the ideal high-side switch for low-voltage, portable battery-management power-distribution systems where maximizing battery life is an important concern. The thermal performance of the 8-pin small-outline (D) package has been greatly enhanced over the standard 8-pin SOIC, further making the TPS1110 ideally suited for many power applications. For compatibility with existing designs, the TPS1110 has a pinout common with other P-channel MOSFETs in small-outline integrated circuit (SOIC) packages. The TPS1110 is characterized for an operating junction temperature range, T_J, from –40°C to 150°C. The D package is available packaged in standard sleeves or in taped and reeled formats. When ordering the tape-and-reel format, add an R suffix to the device type number (e.g., TPS1110DR).

AVAILABLE OPTIONS

T_J	PACKAGED DEVICE†	CHIP FORM (Y)
	SMALL OUTLINE (D)	
–40°C to 150°C	TPS1110D	TPS1110Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1110DR). The chip form is tested at 25°C.

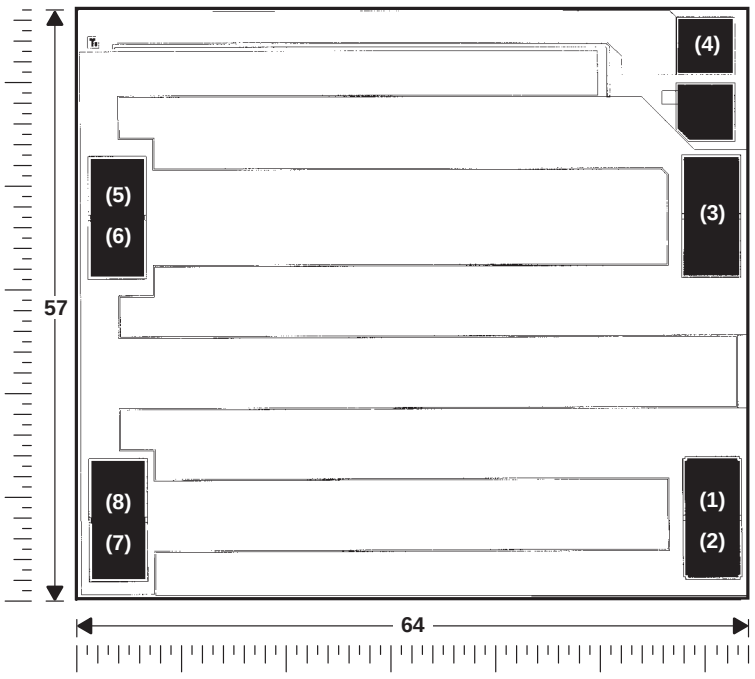
schematic

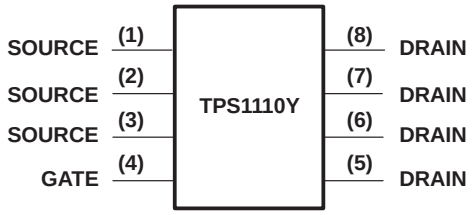


TPS1110Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1110C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

				UNIT
Drain-to-source voltage, V_{DS}			–7	V
Gate-to-source voltage, V_{GS}			±7	V
Continuous drain current, I_D	V_{GS} = –2.7 V	T_P = 25°C‡	–5	A
		T_P = 125°C‡	–2.3	
	V_{GS} = –4.5 V	T_P = 25°C‡	–6	
		T_P = 125°C‡	–2.7	
Pulse drain current, I_D		T_A = 25°C	–24	A
Continuous source current (diode conduction), I_S		T_A = 25°C	–6	A
Continuous total power dissipation		T_P = 25°C‡	4	W
Junction-to-pin thermal resistance (θ_{JP})			31	°C/W
Continuous total power dissipation		T_A = 25°C	1.25	W
Junction-to-ambient thermal resistance (θ_{JA})			100	°C/W
Storage temperature range, T_{stg}			–65 to 150	°C
Operating junction temperature range, T_J			–40 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ T_P – Temperature of drain pins measured close to the package

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS		TPS1110 MIN	TPS1110 TYP	TPS1110 MAX	TPS1110Y MIN	TPS1110Y TYP	TPS1110Y MAX	UNIT
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, See Figure 9	I_D = –250 µA,	–0.5	–0.75	–0.9		–0.75		V
V_{SD}	Source-to-drain voltage (diode forward voltage)§	I_{SD} = –3 A, See Figure 8	V_{GS} = 0 V,		–0.8			–0.8		V
I_{GSS}	Reverse gate current, drain short circuited to source	V_{DS} = 0 V,	V_{GS} = –6 V			±100				nA
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = –7 V, V_{GS} = 0 V	T_J = 25°C			–100				nA
		V_{DS} = –6 V, V_{GS} = 0 V	T_J = 75°C			–100				nA
			T_J = 125°C			–10				µA
$r_{DS(on)}$	Static drain-to-source on-state resistance§	V_{GS} = –4.5 V, See Figure 5	I_D = –6 A,		65	75		65		mΩ
		V_{GS} = –2.7 V, See Figure 5	I_D = –2 A,		100	110		100		
g_{fs}	Forward transconductance§	V_{DS} = –5 V,	I_D = –6 A		5			5		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = –6 V, f = 1 MHz	V_{GS} = 0 V, See Figure 6		275			275		pF
C_{oss}	Short-circuit output capacitance, common source				415			415		
C_{rss}	Short-circuit reverse transfer capacitance, common source				73			73		

§ Pulse test: pulse duration ≤ 300 µs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS	TPS1110			TPS1110Y			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Q_g	Total gate charge	V_{DS} = –6 V, V_{GS} = –6 V, I_D = –3 A, See Figures 1 and 10		4.3	5.4		4.3		nC
Q_{gs}	Gate-to-source charge			0.66	0.83		0.66		
Q_{gd}	Gate-to-drain charge			0.52	0.68		0.52		
$t_{d(on)}$	Turn-on delay time	V_{DD} = –6 V, R_L = 6 Ω, I_D = –1 A, R_G = 6 Ω, See Figure 2		5.8	8		5.8		ns
$t_{d(off)}$	Turn-off delay time			22	29		22		ns
t_r	Rise time			22	29		22		ns
t_f	Fall time			4.5	7		4.5		
$t_{rr(SD)}$	Source-to-drain reverse-recovery time	V_{DS} = –6 V, di/dt = 100 A/μs, I_D = –3 A		65	98		65		
Q_{rr}	Total diode charge			71			71		nC

PARAMETER MEASUREMENT INFORMATION

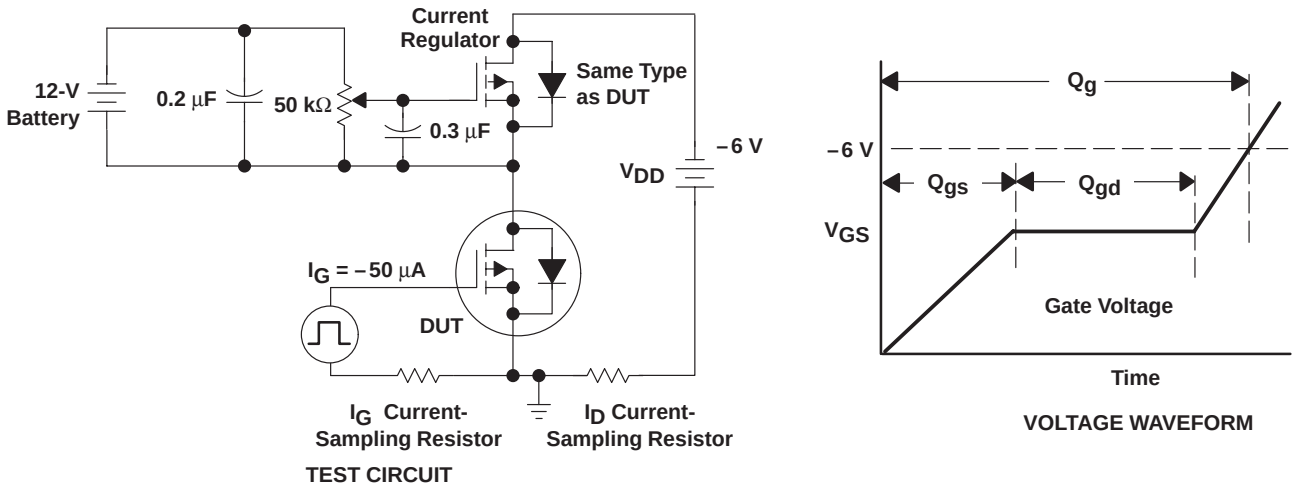


Figure 1. Gate-Charge Test Circuit and Waveform

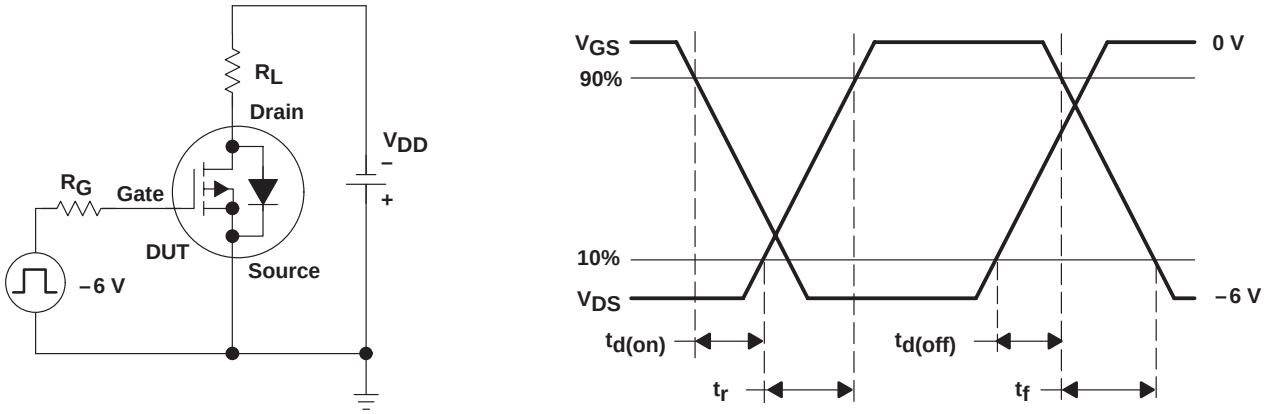


Figure 2. Resistive Switching

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Gate-to-source threshold voltage	vs Junction temperature	9
Gate-to-source voltage	vs Gate charge	10

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

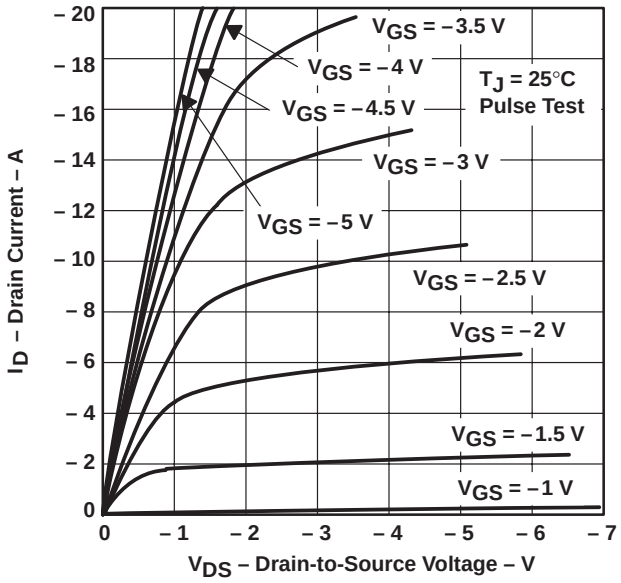


Figure 3

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

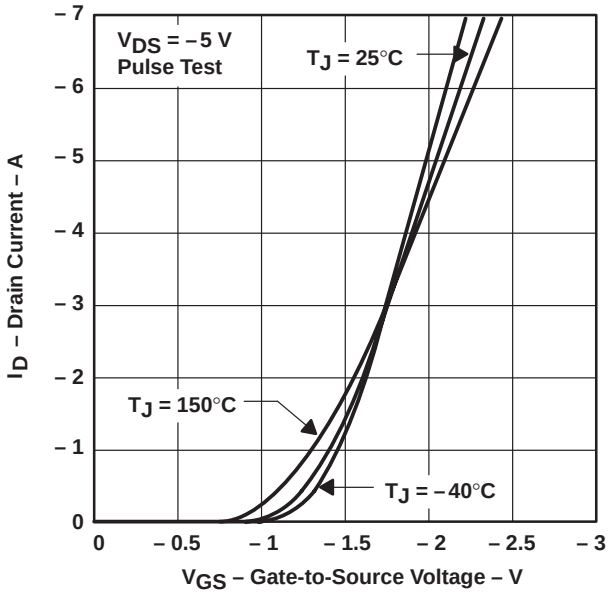


Figure 4

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

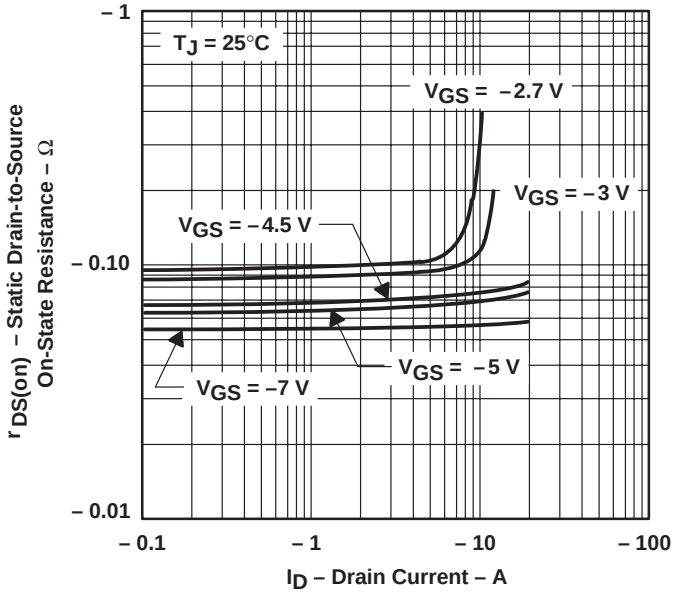
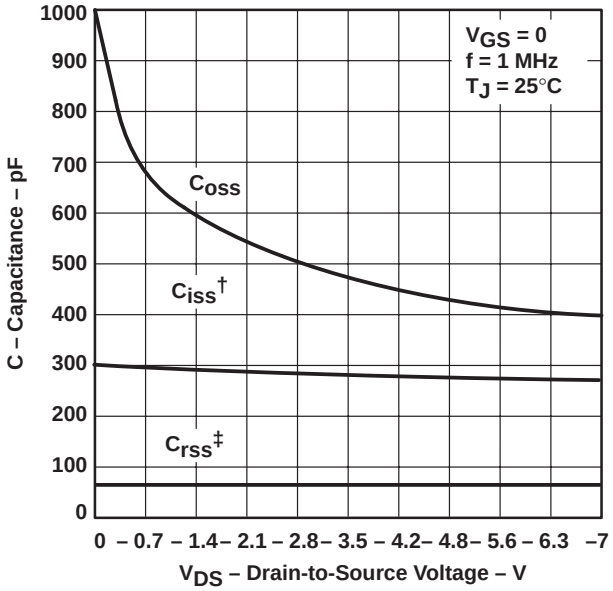


Figure 5

CAPACITANCE† vs DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}$, $C_{ds(shorted)}$
‡ $C_{rss} = C_{gd}$, $C_{oss} = C_{ds} + C_{gd}$

Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE (NORMALIZED) vs JUNCTION TEMPERATURE

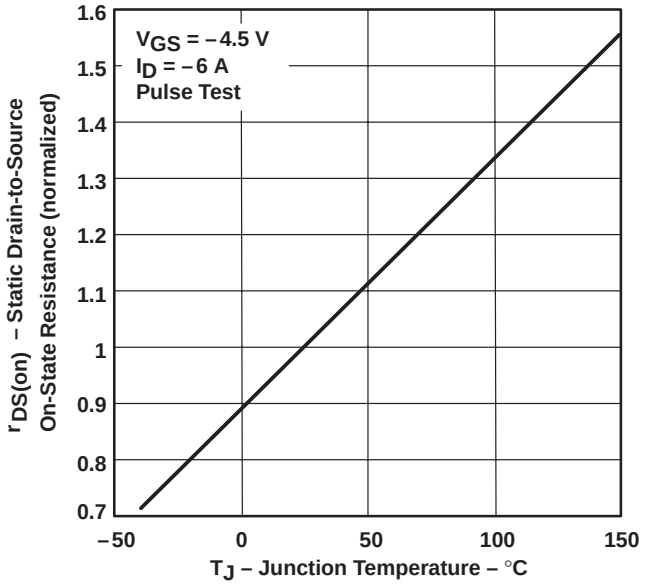


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

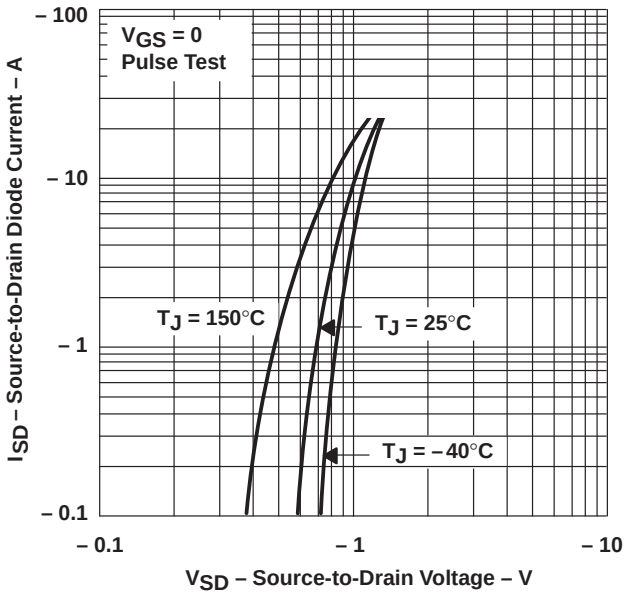


Figure 8

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

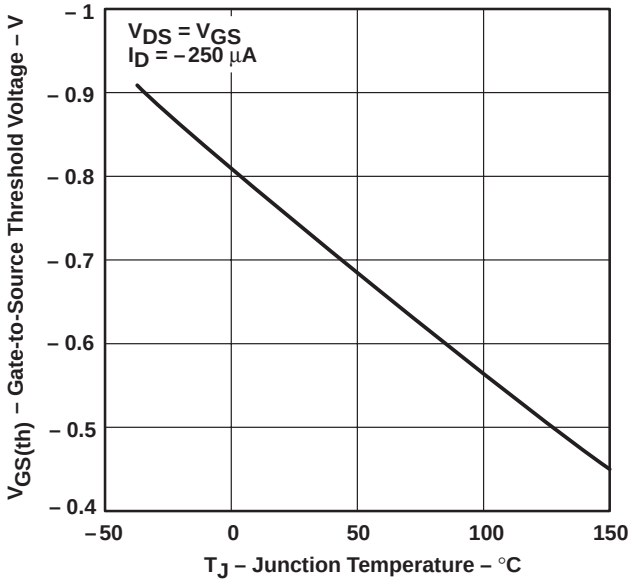


Figure 9

GATE-TO-SOURCE VOLTAGE vs GATE CHARGE

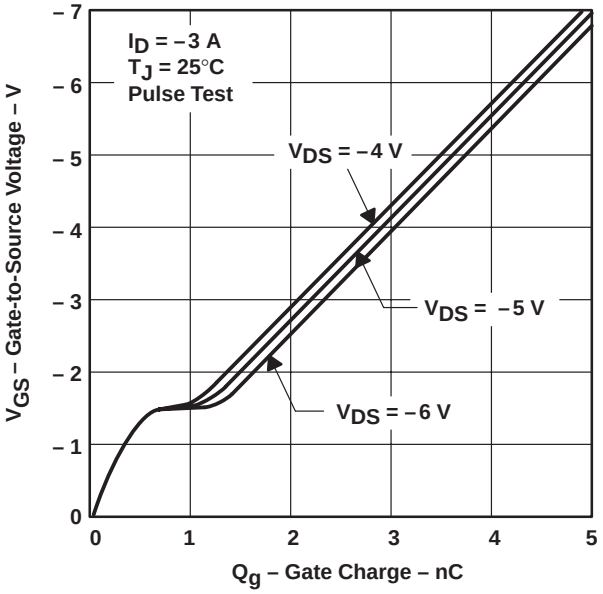


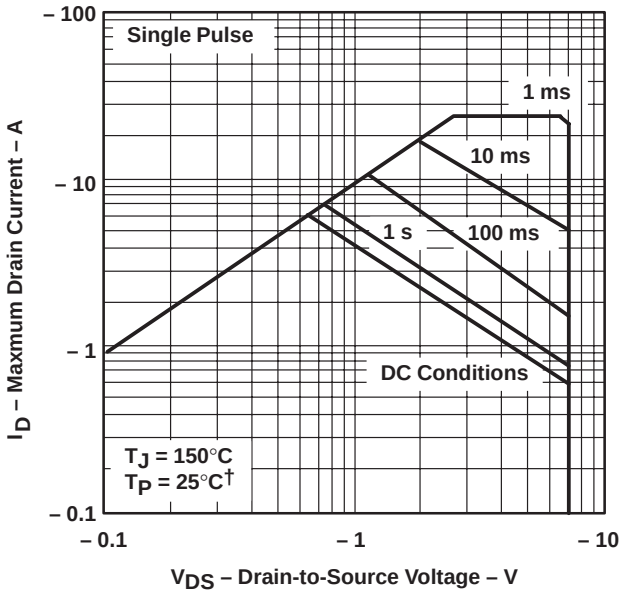
Figure 10

THERMAL INFORMATION

Table of Graphs

		FIGURE
Maximum drain current	vs Drain-to-source voltage	11
Junction-to-pin thermal resistance (normalized)	vs Pulse duration	12
Junction-to-ambient thermal resistance (normalized)	vs Pulse duration	13

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

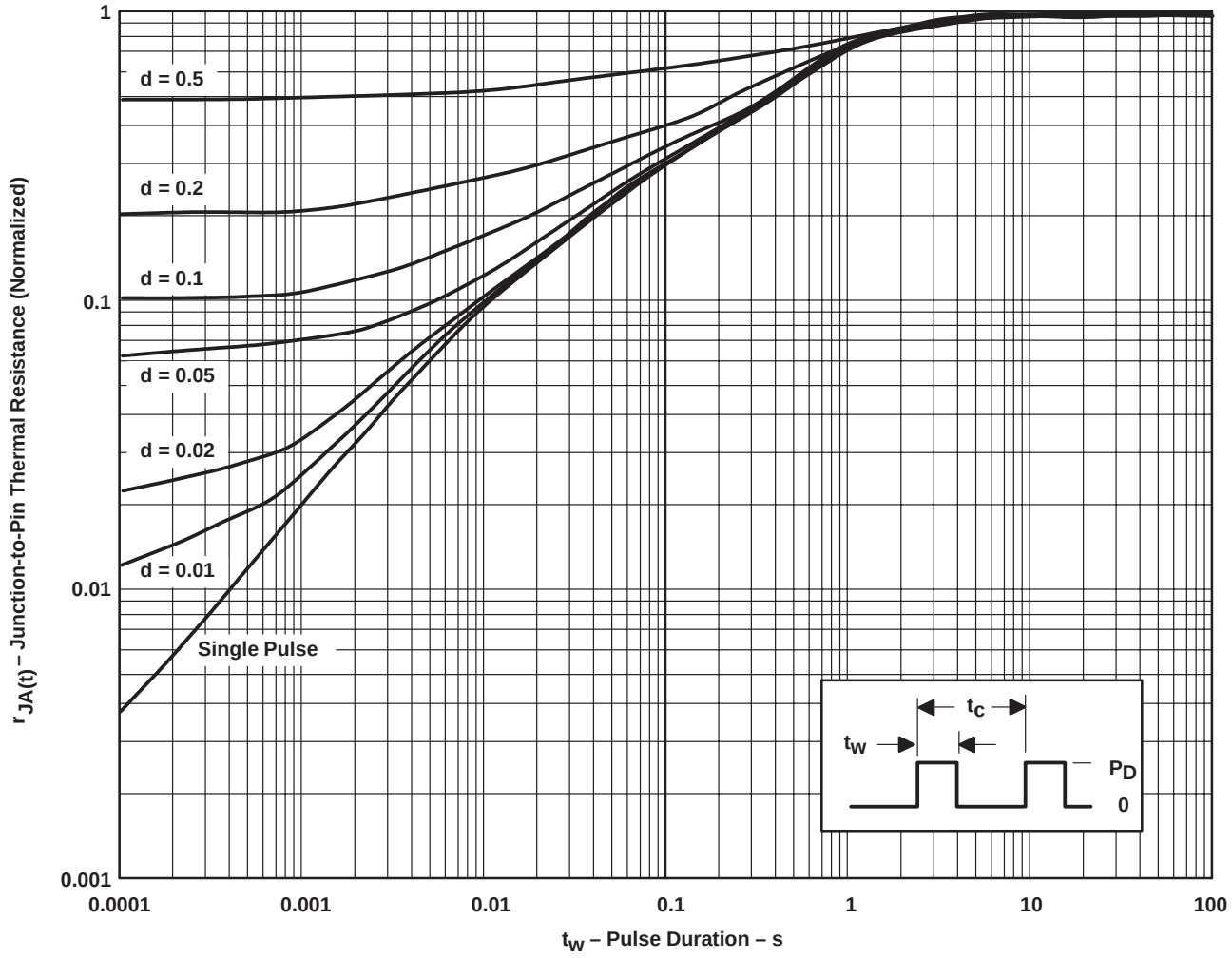


† T_P – Temperature of drain pins measured close to the package

Figure 11

THERMAL INFORMATION

**JUNCTION-TO-PIN THERMAL RESISTANCE (NORMALIZED)
vs
PULSE DURATION**

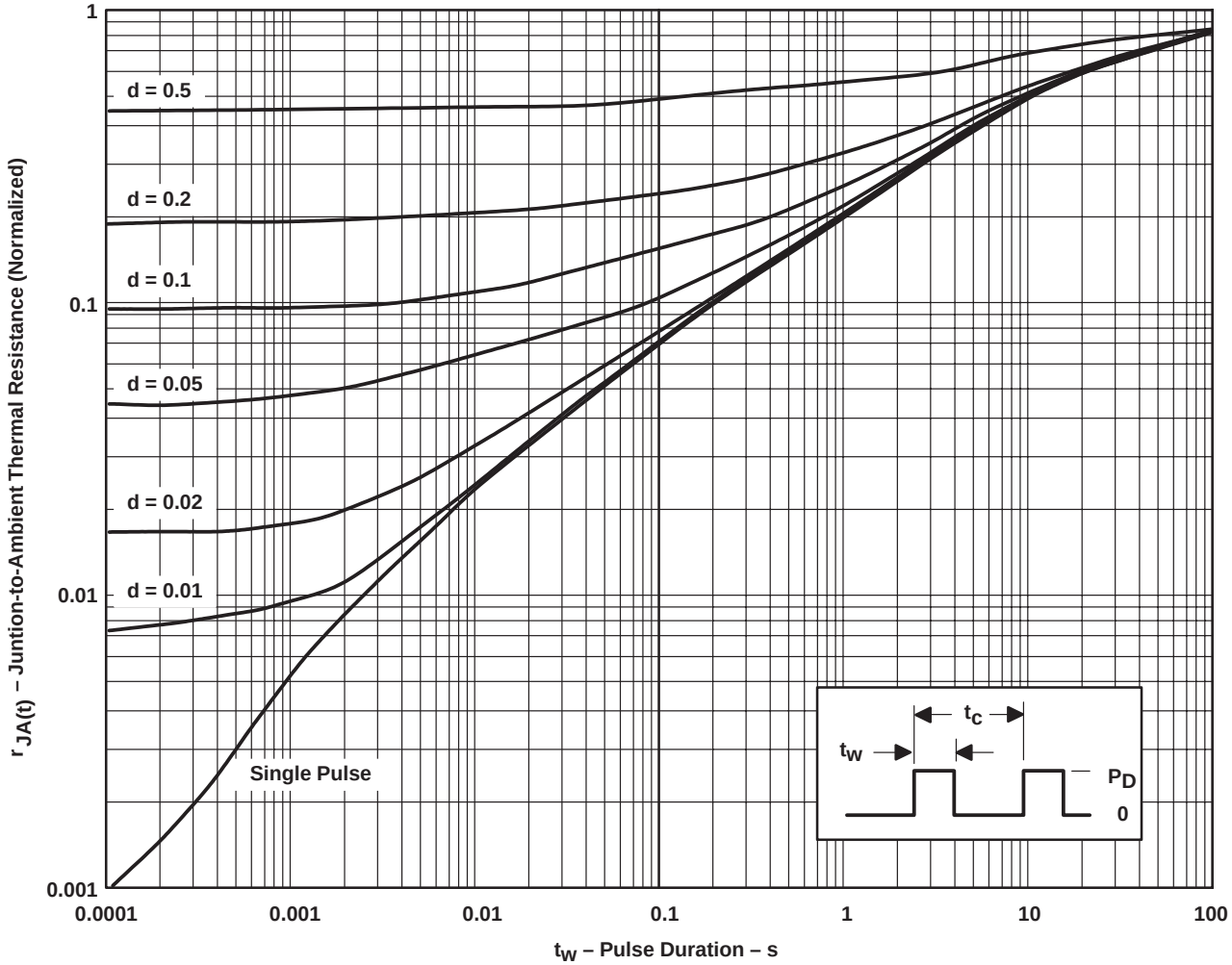


NOTE A: $Z_{\theta JP}(t) = r_{JP(t)} \cdot \theta_{JP}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C
peak $T_J = P_D \cdot Z_{\theta JP}(t) + T_P$

Figure 12

THERMAL INFORMATION

JUNCTION-TO-AMBIENT THERMAL RESISTANCE (NORMALIZED)†
vs
PULSE DURATION



† Device mounted on FR4 printed-circuit board with no special thermal considerations.

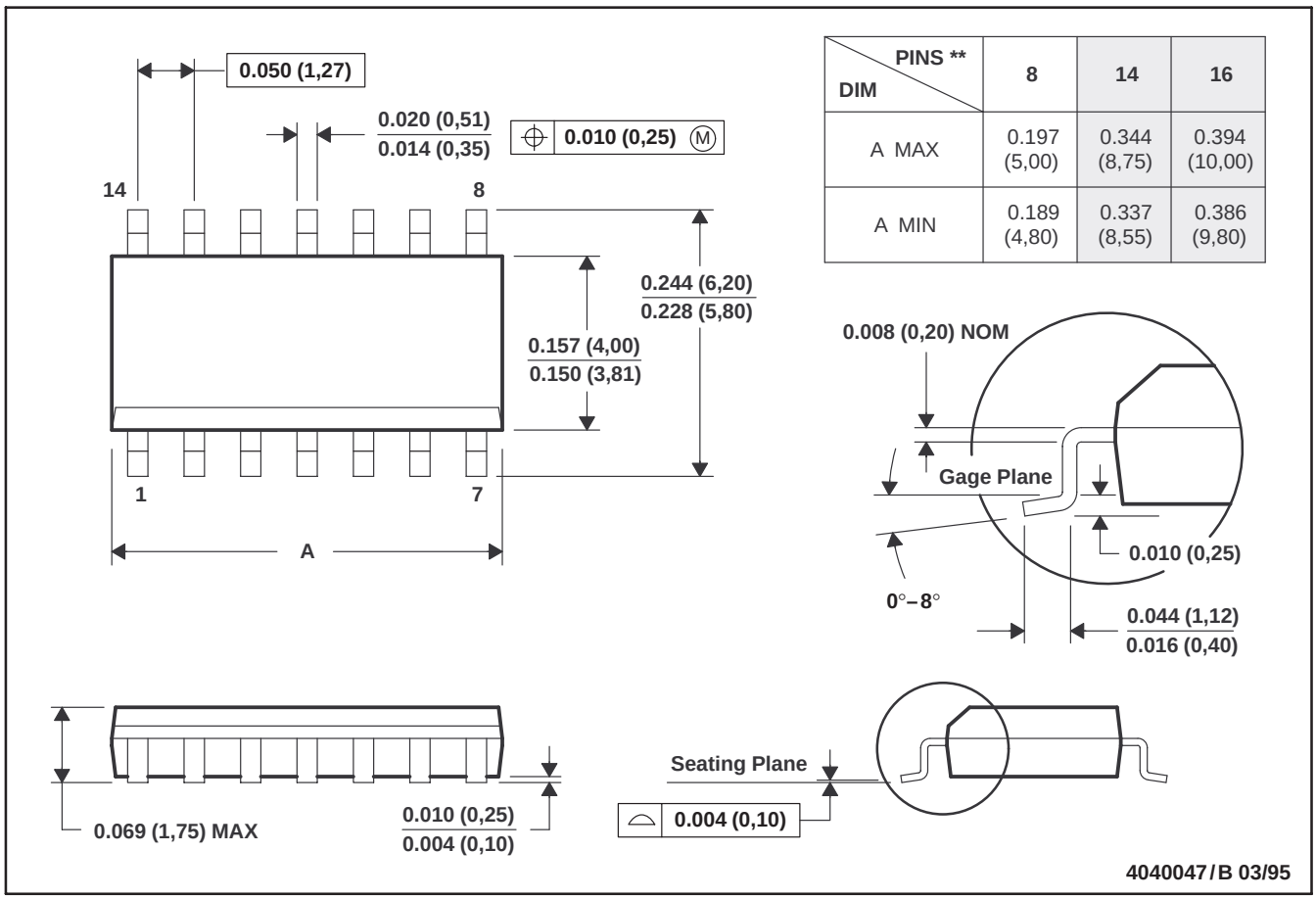
NOTE A: $Z_{\theta JA}(t) = r_{JA(t)} \cdot \theta_{JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C
peak $T_J = P_D \cdot Z_{\theta JA}(t) + T_A$

Figure 13

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

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