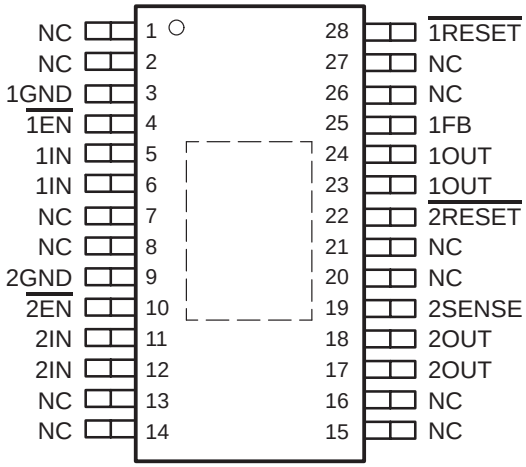
- **Dual Output Voltages for Split-Supply Applications**
- **3.3-V/Adjustable Output**
- **Dropout Voltage < 80 mV Max at I_O = 100 mA**
- **Low Quiescent Current, Independent of Load . . . 340 μA Typ Per Regulator**
- **Ultra-Low-Current Sleep State . . . 2 μA Max**
- **Output Regulated to ±2% Over Full Operating Range for Fixed-Output Regulator**
- **Dual Active-Low Reset Signals with 200-ms Pulse Width**
- **Output Current Range of 0 mA to 750 mA Per Regulator or 1-A Total Device Output Current**
- **28-Pin PowerPAD™ TSSOP Package**

PWP PACKAGE
(TOP VIEW)



NC – No internal connection

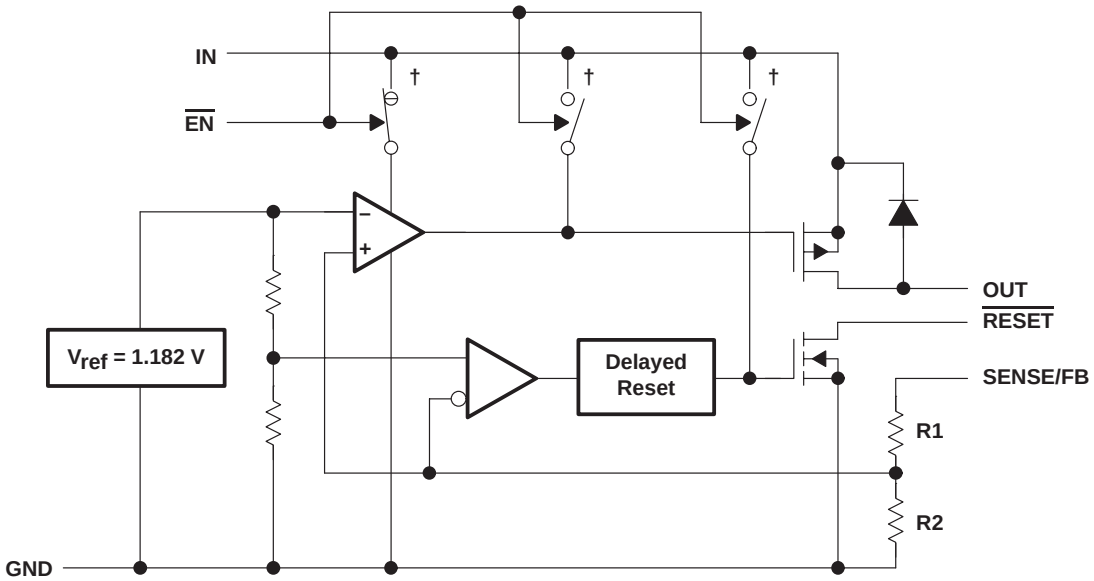
description

The TPS73HD301 voltage regulator offers very low dropout voltages and dual outputs in a compact package. Designed primarily for DSP applications, this regulator can be used in any mixed-output voltage application. Total device output current can be as high as 1 A with each regulator supporting up to 750 mA. Output current can be allocated as desired between the two regulators and used to power many of todays DSPs. Low quiescent current and very low dropout voltage assure maximum power usage in battery-powered applications. Texas Instruments PowerPAD TSSOP package allows use of this device with any voltage/current combination within the range of the listed specifications without thermal problems, provided proper device mounting procedures are followed. Separate inputs allow the designer to configure the source power as desired. Dual active-low reset signals allow resetting of core-logic and I/O separately. Remote sense/feedback terminals provide regulation at the load. The TPS73HD301 is available in 28-pin PowerPAD TSSOP. It operates over a free-air temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

T_A	REGULATOR 1 V_O (V)	REGULATOR 2 V_O (V)	TSSOP (PWP)
–40°C to 125°C	Adj (1.2 – 9.75 V)	3.3 V	TPS73HD301PWPR

functional block diagram



OUTPUT VOLTAGE	R1	R2	UNIT
Adjustable	0	∞	Ω
3.3 V	420	233	kΩ

† Switch positions shown with $\overline{EN}$ low (active).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
NC	1, 2, 7, 8, 13–16, 20, 21, 26, 27		No connection
1GND	3		Regulator #1 ground
$\overline{1EN}$	4	I	Regulator #1 enable, low = enable
1IN	5, 6	I	Regulator #1 input supply voltage
2GND	9		Regulator #2 ground
$\overline{2EN}$	10	I	Regulator #2 enable, low = enable
2IN	11, 12	I	Regulator #2 input supply voltage
2OUT	17, 18	O	Regulator #2 output voltage
2SENSE	19	I	Regulator #2 output voltage sense (fixed output)
$\overline{2RESET}$	22	O	Regulator #2 reset signal, low = reset
1OUT	23, 24	O	Regulator #1 output voltage
1FB	25	I	Regulator #1 output voltage feedback (adjustable output)
$\overline{1RESET}$	28	O	Regulator #1 reset signal, low = reset

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range, V_I (xIN, $\overline{\text{xRESET}}$, xSENSE, $\overline{\text{xEN}}$) . . . . . –0.3 V to 11 V
Differential input voltage,V_{ID} (1GND to 2GND) . . . . . 2 V
Output current, I_O (1OUT, 2OUT) . . . . . 2 A
Continuous total power dissipation . . . . . See Dissipation Rating Tables
Operating free-air temperature range, T_A . . . . . –40°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES‡

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PWP§	700 mW	5.6 mW/°C	448 mW	364 mW

DISSIPATION RATING TABLE 2 – CASE TEPMPERATURE‡

PACKAGE	T_A < 62.5°C POWER RATING	DERATING FACTOR ABOVE T_A = 62.5°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PWP§	25 W	285.76 mW/°C	22.9 W	18.6 W

‡ Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. For guidelines on maintaining junction temperature within recommended operating range, see the Thermal Information section.

§ Refer to the Thermal Information section for detailed power dissipation considerations when using the TSSOP packages.

MAXIMUM CONTINUOUS DISSIPATION vs FREE-AIR TEMPERATURE

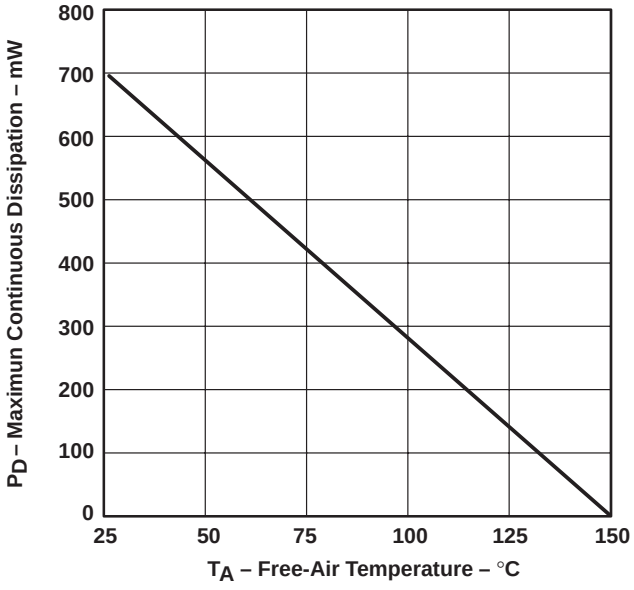


Figure 1

MAXIMUM CONTINUOUS DISSIPATION vs CASE TEMPERATURE

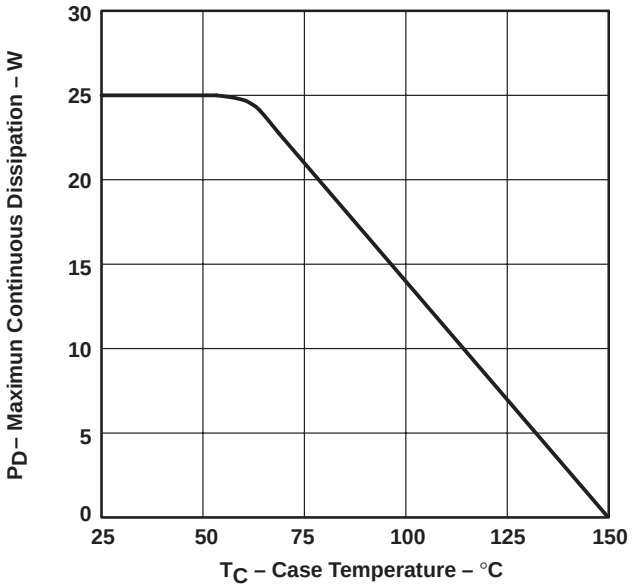


Figure 2

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I†	Adjustable output (regulator #1)	2.97	10	V
	3.3-V output (regulator #2)	3.97	10	
High-level input voltage at $\overline{EN}$, V_{IH}		2		V
Low-level input voltage at $\overline{EN}$, V_{IL}			0.5	V
Total output current range (per regulator), I_O		0	750	mA
Operating virtual junction temperature range, T_J		–40	125	°C

† Minimum input voltage defined in the recommended operating conditions is the maximum specified output voltage plus dropout voltage, V_{DO}, at the maximum specified load range (750 mA). Since dropout voltage is a function of output current, the usable range can be extended for lighter loads. To calculate the minimum input voltage for the maximum load current used in a given application, use the following equation:

$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$

Because regulator 2 of the TPS373HD301 is programmable, $r_{DS(on)}$ should be used to calculate V_{DO} before applying the above equation. The equation for calculating V_{DO} from $r_{DS(on)}$ is given in Note 2 in the TPS73HD301 electrical characteristics table. The minimum value of 2.97 V is the absolute lower limit for the recommended input voltage range for the TPS73HD301.

electrical characteristics, $V_{I(IN)}$ = 4.3 V, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR‡ = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	T_J	MIN	TYP	MAX	UNIT
	Quiescent current (active mode), each regulator	EN ≤ 0.5 V, $V_I = V_O$ + 1 V, 0 mA ≤ I_O ≤ 750 mA	25°C		340	415	μA
			–40°C to 125°C			550	
I_{CC}	Supply current (standby mode), each regulator	EN = V_I, 3 V ≤ V_I ≤ 10 V	25°C		0.01	0.5	μA
			–40°C to 125°C			2	
I_O	Output current limit, each regulator	V_O = 0, V_I = 10 V	25°C	0.8	1.2	2	A
			–40°C to 125°C			2	
I_{lkg}	Pass-element leakage current (standby mode)	EN = V_I, 3 V ≤ V_I ≤ 10 V	25°C		0.01	0.5	μA
			–40°C to 125°C			1	
	Output voltage temperature coefficient		–40°C to 125°C		61	75	ppm/°C
	Thermal shutdown junction temperature				165		°C
	Logic high (EN) (standby mode)	2.5 V ≤ V_I ≤ 6 V, 6 V ≤ V_I ≤ 10 V	–40°C to 125°C	2			V
				2.7			
	Logic low (EN) (active mode)	3 V ≤ V_I ≤ 10 V	25°C			0.5	V
			–40°C to 125°C			0.5	
V_{hys}	Hysteresis voltage ($\overline{EN}$)		25°C		50		mV
I_I	Input current (EN)	0 V ≤ V_I ≤ 10 V	25°C	–0.5	0.001	0.5	μA
			–40°C to 125°C	–0.5		0.5	
	Minimum input voltage, for active pass element		25°C		2.05	2.5	V
			–40°C to 125°C			2.5	
	Minimum input voltage, for valid RESET	$I_{O(RESET)}$ = –300 μA	25°C		1	1.5	V
			–40°C to 125°C			1.9	

‡ CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

§ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics, $V_{I(IN)}$ = 4.3 V, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR‡ = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted) (continued)

regulator #1 (adjustable)

PARAMETER		TEST CONDITIONS§		T_J	MIN	TYP	MAX	UNIT
	Reference voltage (1FB)	2.97 V ≤ V_I ≤ 10 V, 5 mA ≤ I_O ≤ 750 mA		25°C		1.182		V
				–40°C to 125°C	1.147		1.217	
	Reference voltage temperature coefficient			–40°C to 125°C		61	75	ppm/°C
	Pass-element series resistance (see Note 2)	2.97 V ≤ V_I ≤ 10 V, 50 μA ≤ I_O ≤ 750 mA		25°C		0.52	1	Ω
				–40°C to 125°C			1	
		V_I = 3.9 V, 50 μA ≤ I_O ≤ 750 mA		25°C		0.32		
		V_I = 5.9 V, 50 μA ≤ I_O ≤ 750 mA		25°C		0.23		
	Input regulation	V_I = 2.97 V, 50 μA ≤ I_O ≤ 750 mA		25°C		3	18	mV
				–40°C to 125°C			25	
	Output regulation	I_O = 5 mA to 750 mA, 3 V ≤ V_I ≤ 10 V		25°C		7	21	mV
				–40°C to 125°C			32	
		I_O = 50 μA to 750 mA, 3 V ≤ V_I ≤ 10 V		25°C		10	33	mV
				–40°C to 125°C			65	
	Ripple rejection	f = 120 Hz,	I_O = 50 μA	25°C		59		dB
		f = 120 Hz,	I_O = 500 mA	25°C		54		
	Output noise-spectral density	f = 120 Hz		25°C		2		mV/√Hz
	Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR = 1 Ω	C_L = 4.7 μF	25°C		95		μV/rms
			C_L = 10 μF	25°C		89		
			C_L = 100 μF	25°C		74		
$V_{(TO)}$	Trip-threshold voltage ($\overline{RESET}$)¶	$V_{O(FB)}$ decreasing		–40°C to 125°C	1.101		1.145	V
V_{hys}	Hysteresis voltage ($\overline{RESET}$)¶	Measured at $V_{O(ER)}$		25°C		12		mV
V_{OL}	Low-level output voltage ($\overline{RESET}$)¶	V_I = 2.13 V, $I_{O(RESET)}$ = 400 μA		25°C		0.1	0.4	V
				–40°C to 125°C			0.4	
I_I	Input current (1FB)			25°C	–10	0.1	10	nA
				–40°C to 125°C	–20		20	

‡ CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_L.

§ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

¶ Output voltage programmed to 2.5 V with closed-loop configuration (see application information)

NOTE 2: To calculate dropout voltage, use equation:

$$V_{DO} = I_O \times r_{DS(ON)}$$

$r_{DS(ON)}$ is a function of both output current and input voltage. This parametric table lists $r_{DS(ON)}$ for V_I = 2.97 V, 3.9 V, and 5.9 V, which corresponds to dropout conditions for programmed output voltages of 3 V, 4 V, and 6 V respectively. For other programmed values, refer to Figure 29.

electrical characteristics, $V_{I(IN)}$ = 4.3 V, I_O = 10 mA, $\overline{EN}$ = 0 V, C_O = 4.7 μF/CSR‡ = 1 Ω, SENSE/FB shorted to OUT (unless otherwise noted) (continued)

regulator #2 (3.3 V)

PARAMETER		TEST CONDITIONS§		T_J	MIN	TYP	MAX	UNIT
V_O	Output voltage	4.3 V ≤ V_I ≤ 10 V		25°C		3.3		V
				–40°C to 125°C	3.23		3.37	
	Dropout voltage	I_O = 10 mA,	V_I = 3.23 V	25°C		4.5	10	mV
		I_O = 100 mA,	V_I = 3.23 V	25°C		44	100	
		I_O = 750 mA,	V_I = 3.23 V	25°C		353	750	
				–40°C to 125°C			800	
	Pass-element series resistance	(3.23 V – V_O)/I_O, I_O = 750 mA	V_I = 3.23 V,	25°C		0.44	1	Ω
				–40°C to 125°C			1.07	
	Input regulation	V_I = 4.3 V to 10 V, 50 μA ≤ I_O ≤ 750 mA		25°C		6	28	mV
				–40°C to 125°C			29	
	Output regulation	I_O = 5 mA to 750 mA, 4.3 V ≤ V_I ≤ 10 V		25°C		32	57	mV
				–40°C to 125°C			113	
		I_O = 50 μA to 750 mA, 4.3 V ≤ V_I ≤ 10 V		25°C		47	90	mV
				–40°C to 125°C			180	
	Ripple rejection	f = 120 Hz,	I_O = 50 μA	25°C		51		dB
		f = 120 Hz,	I_O = 500 mA	25°C		49		
	Output noise-spectral density	f = 120 Hz		25°C		2		mV/√Hz
	Output noise voltage	10 Hz ≤ f ≤ 100 kHz, CSR = 1 Ω	C_L = 4.7 μF	25°C		274		μV/rms
			C_L = 10 μF	25°C		228		
			C_L = 100 μF	25°C		159		
$V_{(TO)}$	Trip-threshold voltage ($\overline{RESET}$)	V_O decreasing		–40°C to 125°C	2.868			V
V_{hys}	Hysteresis voltage ($\overline{RESET}$)			25°C		18		mV
V_{OL}	Low-level output voltage ($\overline{RESET}$)	V_I = 2.8 V,	$I_{O(RESET)}$ = –1 mA	25°C		0.17	0.4	V
				–40°C to 125°C			0.4	

‡ CSR (compensation series resistance) refers to the total series resistance, including the equivalent series resistance (ESR) of the capacitor, any series resistance added externally, and PWB trace resistance to C_L.

§ Pulse-testing techniques are used to maintain virtual junction temperature as close as possible to ambient temperature; thermal effects must be taken into account separately.

switching characteristics

PARAMETER	TEST CONDITIONS§	T_J	MIN	TYP	MAX	UNIT
Time-out delay (RESET)	See Figure 3	25°C	140	200	260	ms
		–40°C to 125°C	100		300	

PARAMETER MEASUREMENT INFORMATION

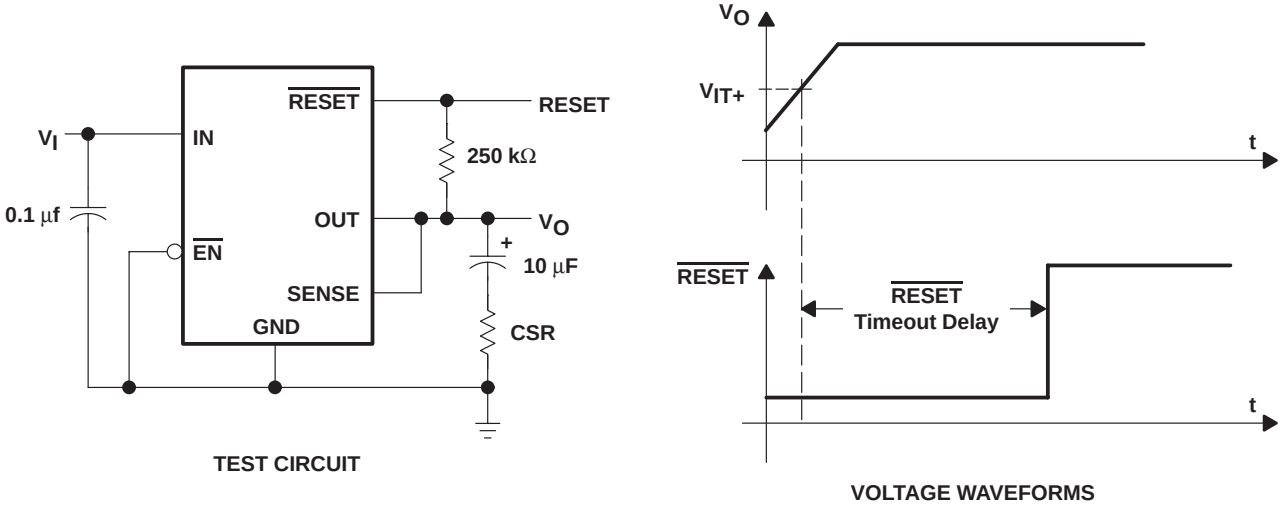


Figure 3. Test Circuit and Voltage Waveforms

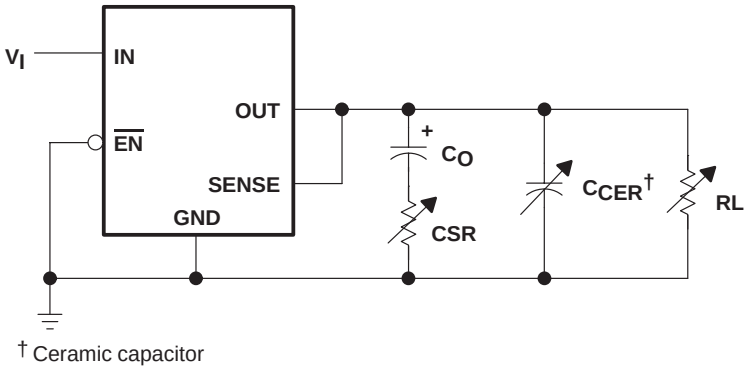


Figure 4. Test Circuit for Typical Regions of Stability (Refer to Figures 29 through 32)

TYPICAL CHARACTERISTICS

Table of Graphs

I_Q	Quiescent current		vs Load current	5
			vs Input voltage	6
V_{DO}	Dropout voltage	Adjustable regulator	vs Output current	7
V_{DO}	Dropout voltage	3.3-V regulator		8
ΔV_{DO}	Change in dropout voltage		vs Free-air temperature	9
V_{DO}	Dropout voltage		vs Output current	10
ΔV_O	Change in output voltage		vs Free-air temperature	11
V_O	Output voltage		vs Input voltage	12
	Line regulation			13
V_O	Output voltage		vs Output current	14
V_O	Output voltage		vs Output current	15
	Output voltage response from enable ($\overline{EN}$)			16
	Load transient response	Adjustable regulator		17
		3.3-V regulator		18
	Line transient response			19
	Line transient response			20
	Ripple rejection		vs Frequency	21
	Output spectral noise density		vs Frequency	22
	Compensation series resistance (CSR)	Adjustable regulator	vs Output current (C_O = 4.7 μF)	23
			vs Added ceramic capacitance (C_O = 4.7 μF)	24
			vs Output current (C_O = 10 μF)	25
		3.3-V regulator	vs Output current (C_O = 10 μF)	26
		Adjustable regulator	vs Added ceramic capacitance (C_O = 10 μF)	27
		3.3-V regulator	vs Added ceramic capacitance (C_O = 10 μF)	28
$r_{DS(on)}$	Pass-element resistance		vs Input voltage	29
V_I	Minimum input voltage for valid $\overline{RESET}$		vs Free-air temperature	30
V_{IT-}	Negative-going reset threshold		vs Free-air temperature	31
$I_{OL(RESET)}$	$\overline{RESET}$ output current		vs Input voltage	32
t_d	Reset time delay		vs Free-air temperature	33
t_d	Distribution for reset delay			34

TYPICAL CHARACTERISTICS

QUEISCENT CURRENT
vs
LOAD CURRENT

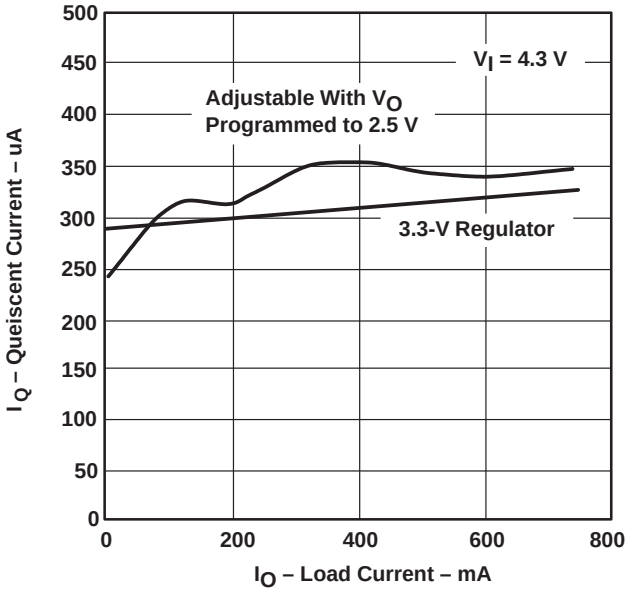


Figure 5

QUIESCENT CURRENT
vs
INPUT VOLTAGE

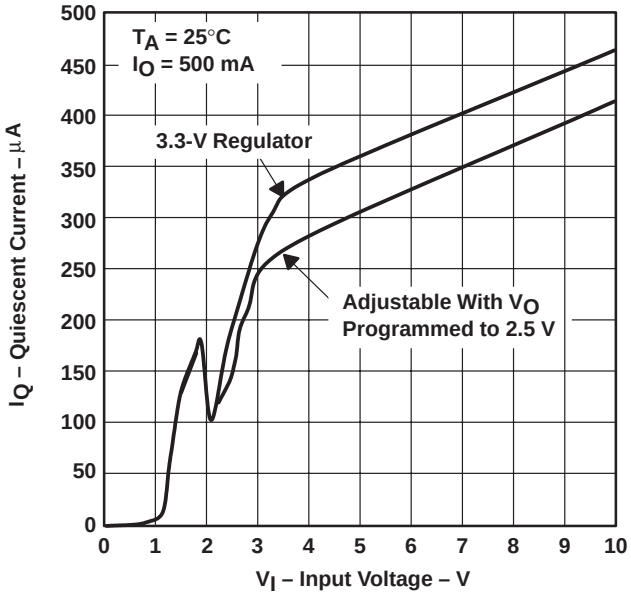


Figure 6

ADJUSTABLE REGULATOR DROPOUT VOLTAGE
vs
LOAD CURRENT

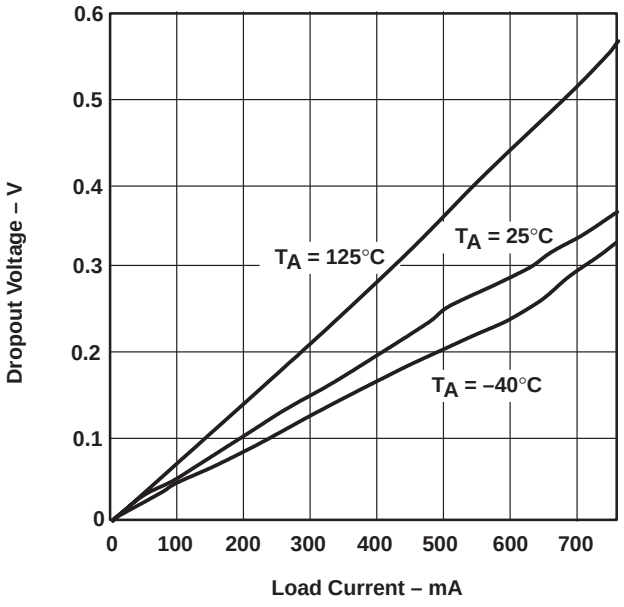


Figure 7

3.3–V REGULATOR DROPOUT VOLTAGE
vs
LOAD CURRENT

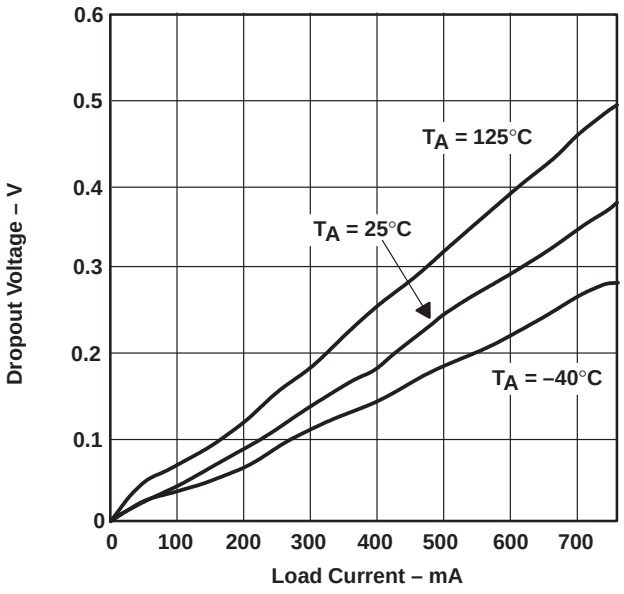


Figure 8

TYPICAL CHARACTERISTICS

CHANGE IN DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

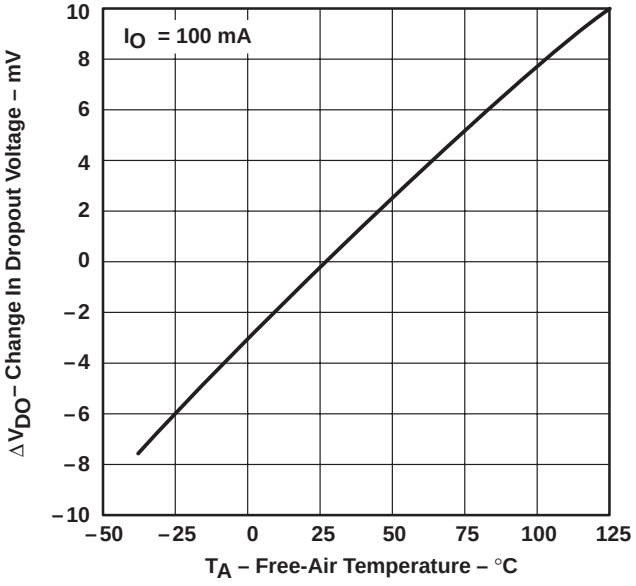


Figure 9

DROPOUT VOLTAGE vs OUTPUT CURRENT

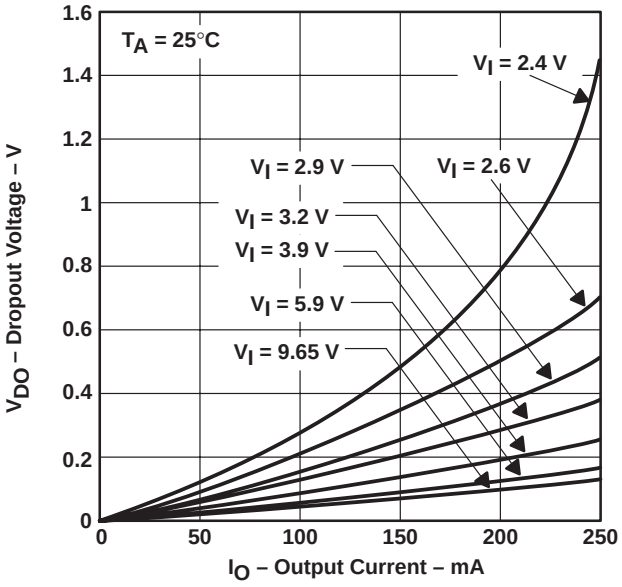


Figure 10

CHANGE IN OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

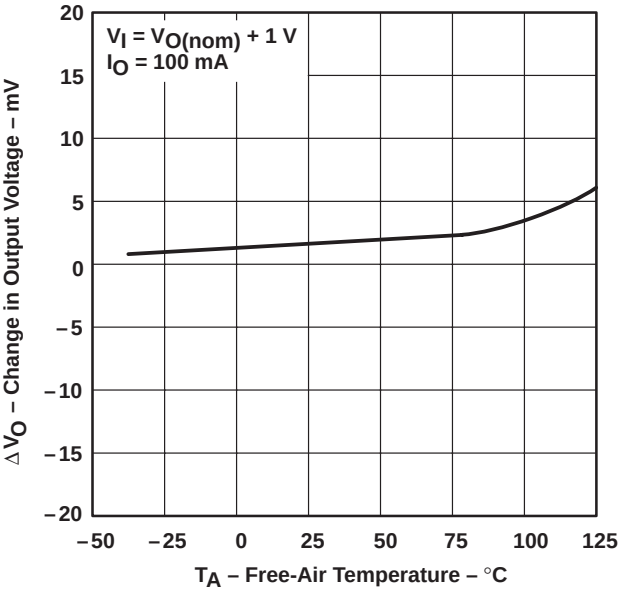


Figure 11

OUTPUT VOLTAGE vs INPUT VOLTAGE

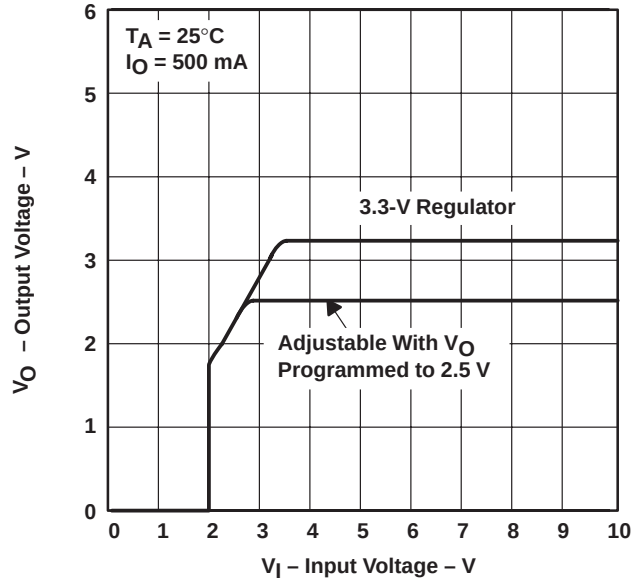


Figure 12

TYPICAL CHARACTERISTICS

LINE REGULATION

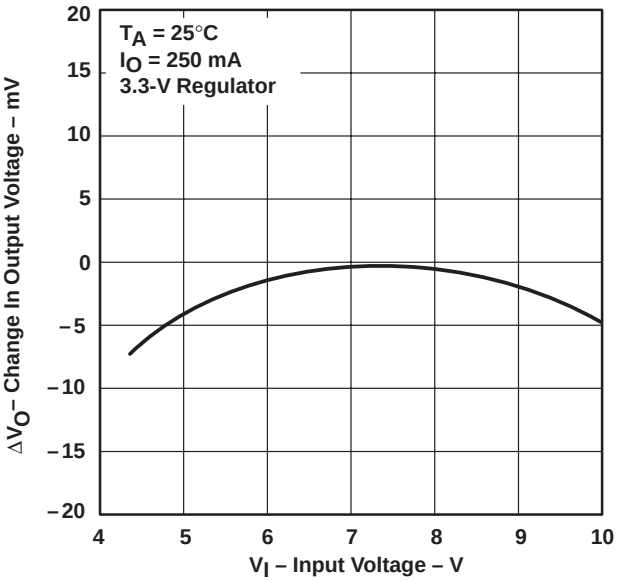


Figure 13

OUTPUT VOLTAGE vs OUTPUT CURRENT

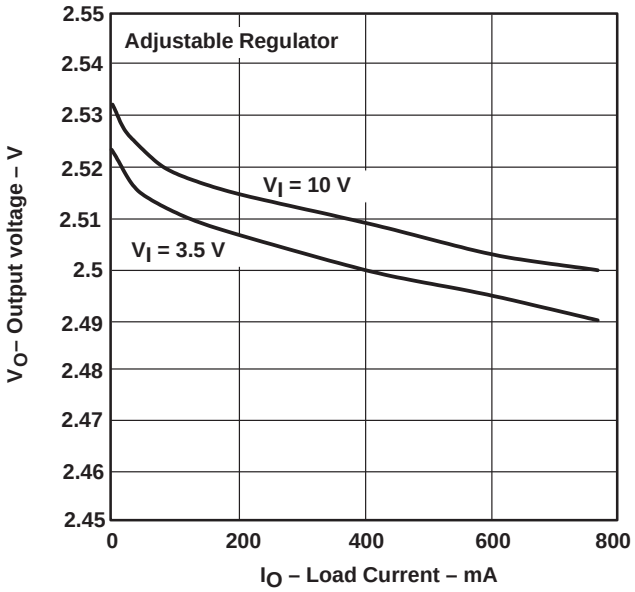


Figure 14

OUTPUT VOLTAGE vs OUTPUT CURRENT

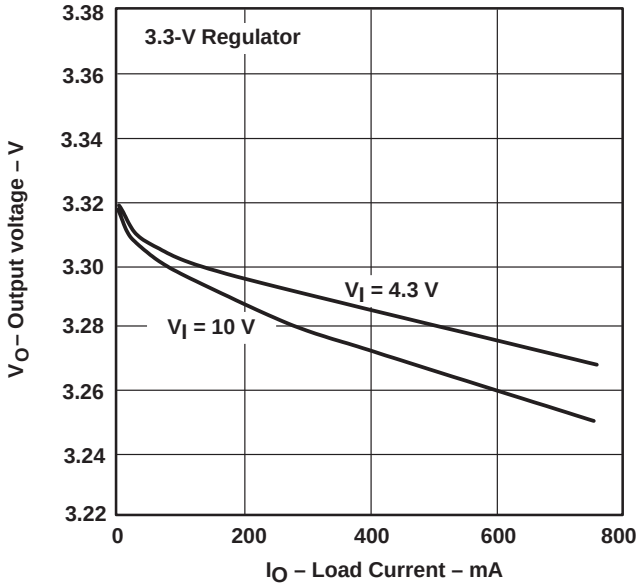


Figure 15

TYPICAL CHARACTERISTICS

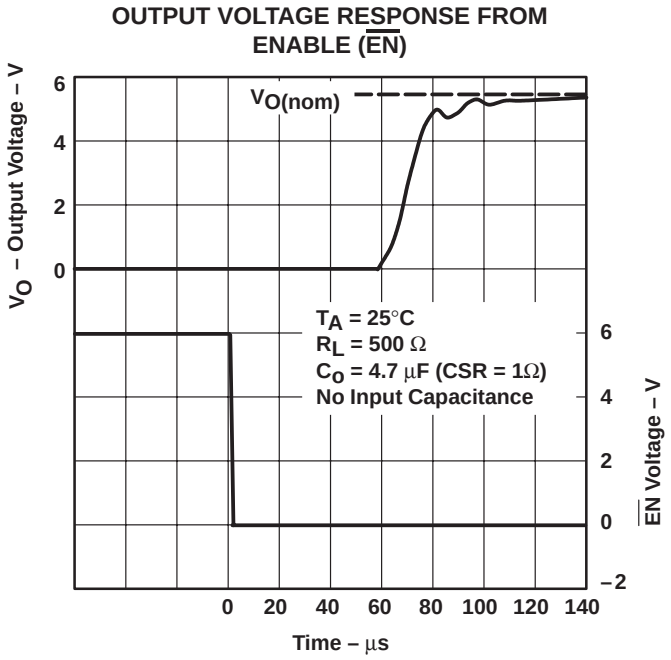


Figure 16

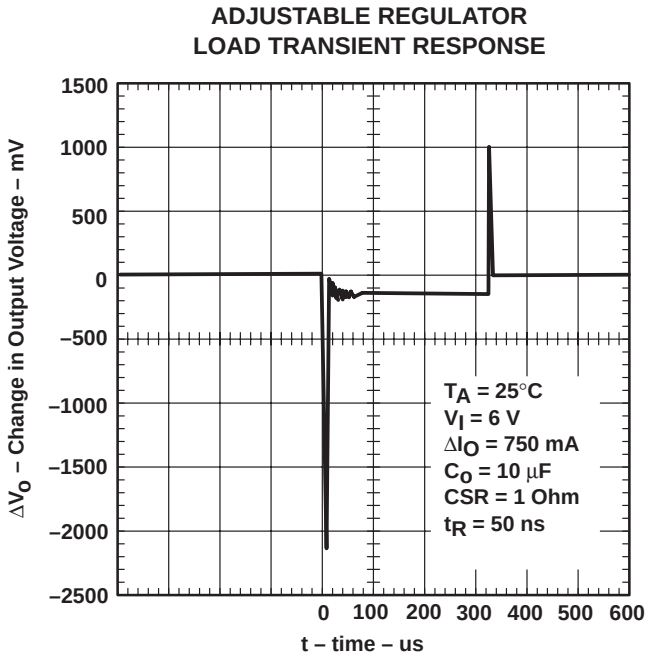


Figure 17

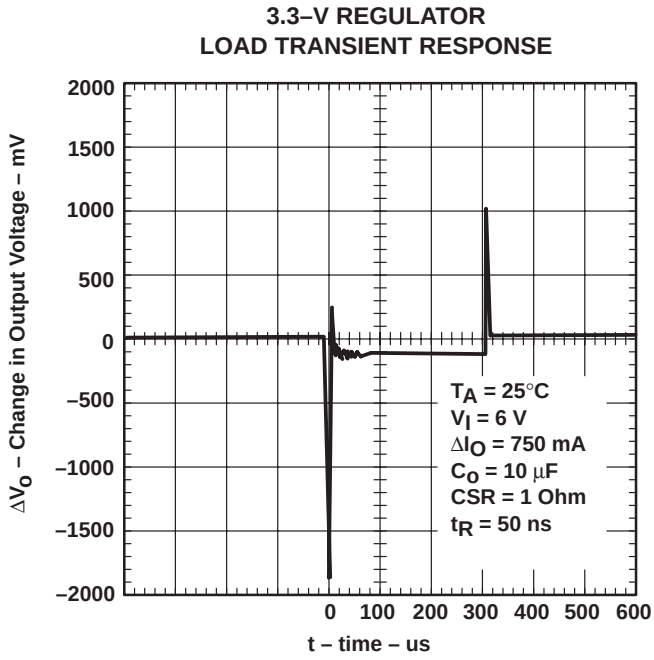


Figure 18

TYPICAL CHARACTERISTICS

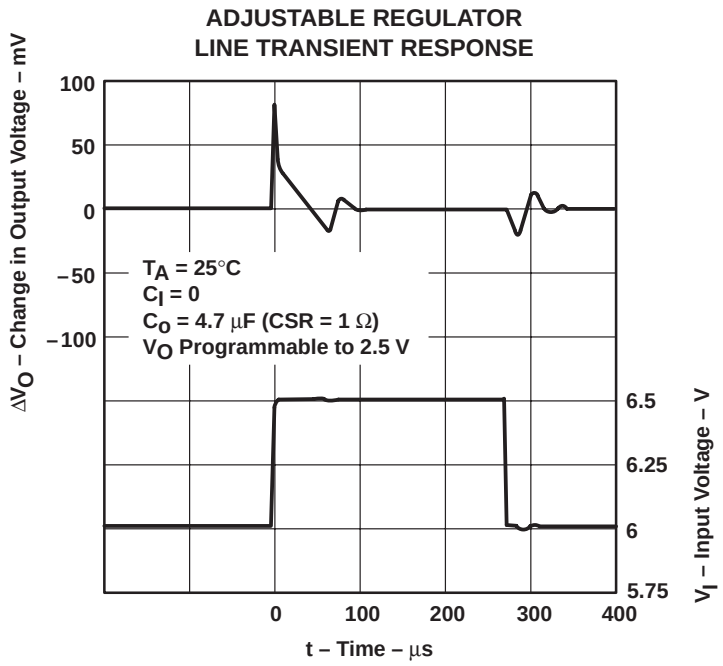


Figure 19

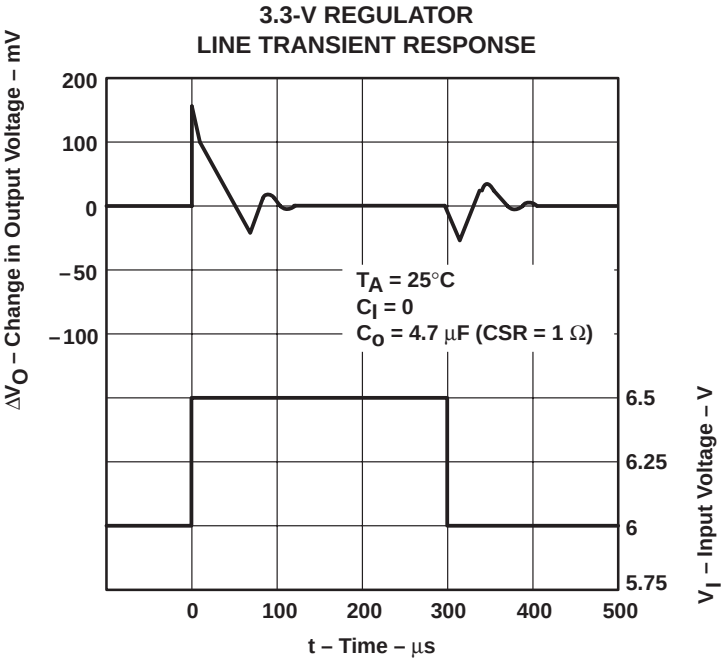


Figure 20

TYPICAL CHARACTERISTICS

RIPPLE REJECTION
vs
FREQUENCY

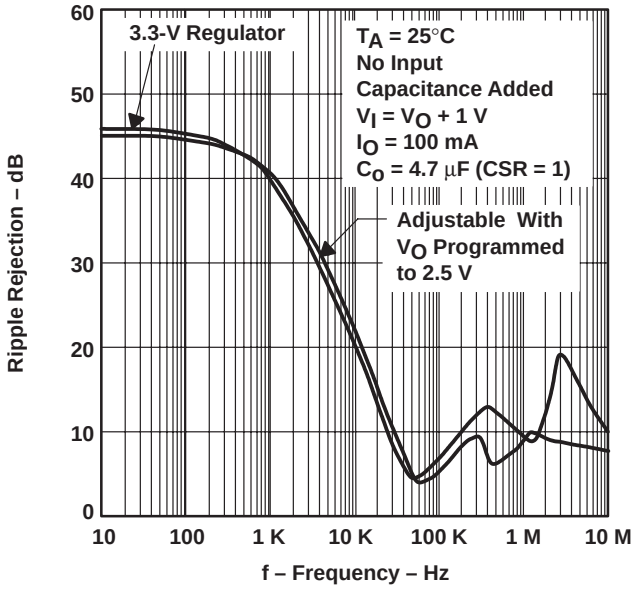


Figure 21

OUTPUT SPECTRAL-NOISE DENSITY
vs
FREQUENCY

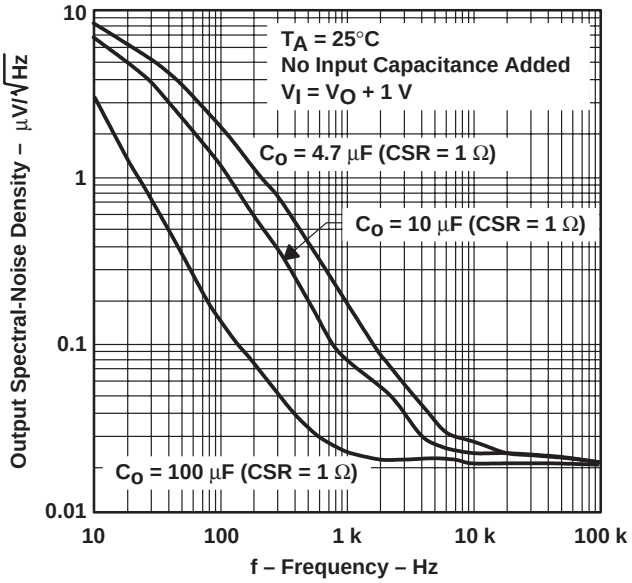


Figure 22

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
OUTPUT CURRENT

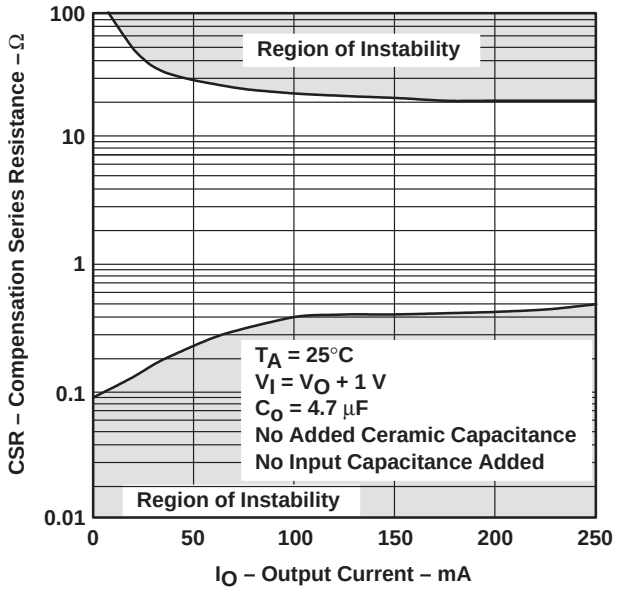


Figure 23

TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE (CSR)†
vs
ADDED CERAMIC CAPACITANCE

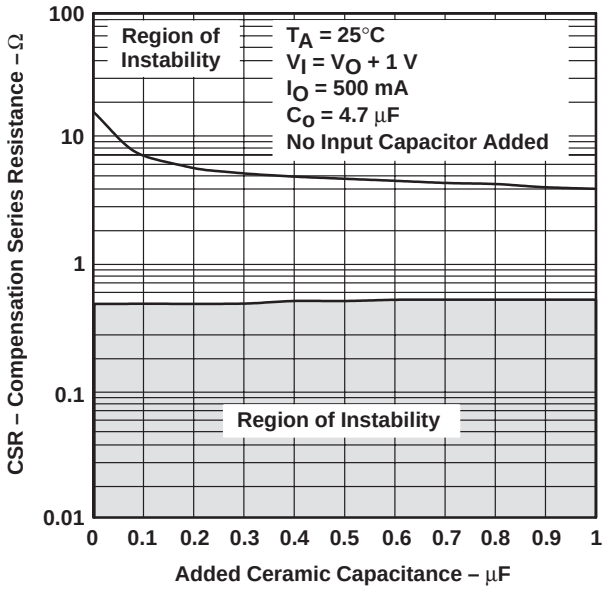


Figure 24

TYPICAL CHARACTERISTICS

ADJUSTABLE REGULATOR TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

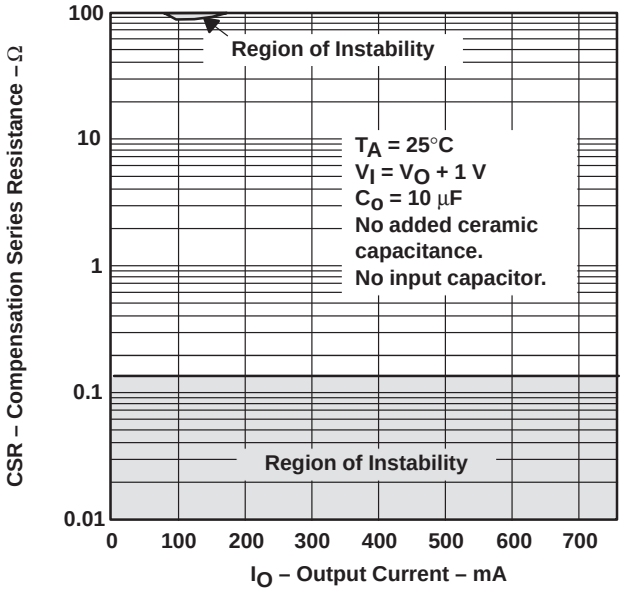


Figure 25

3.3–V REGULATOR TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
OUTPUT CURRENT

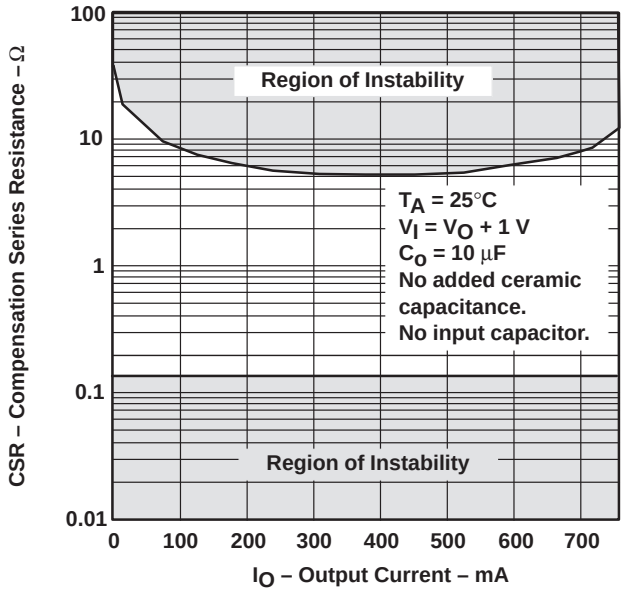


Figure 26

ADJUSTABLE REGULATOR TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

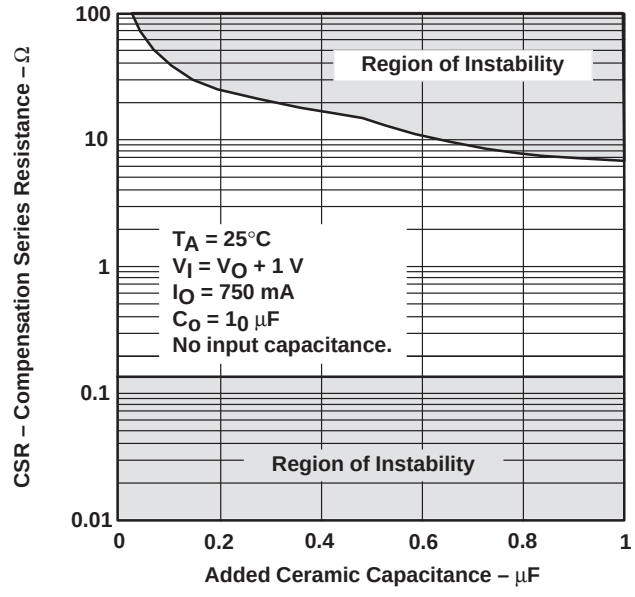


Figure 27

3.3-V REGULATOR TYPICAL REGIONS OF STABILITY
COMPENSATION SERIES RESISTANCE
vs
ADDED CERAMIC CAPACITANCE

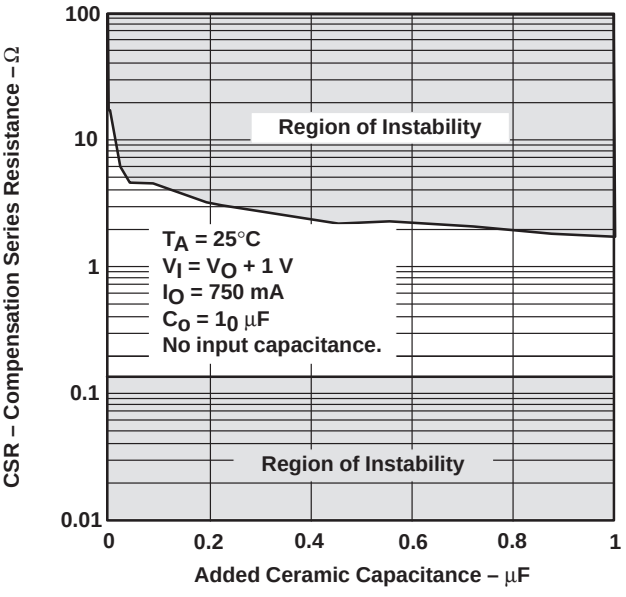


Figure 28

TYPICAL CHARACTERISTICS

PASS-ELEMENT RESISTANCE vs INPUT VOLTAGE

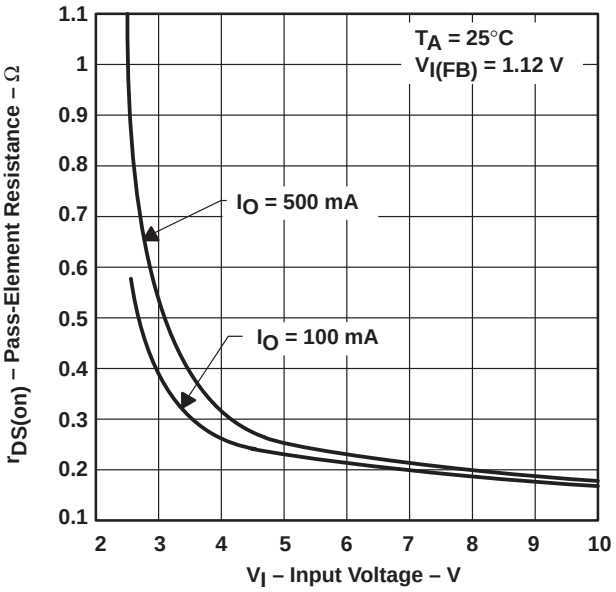


Figure 29

MINIMUM INPUT VOLTAGE FOR VALID $\overline{\text{RESET}}$ vs FREE-AIR TEMPERATURE

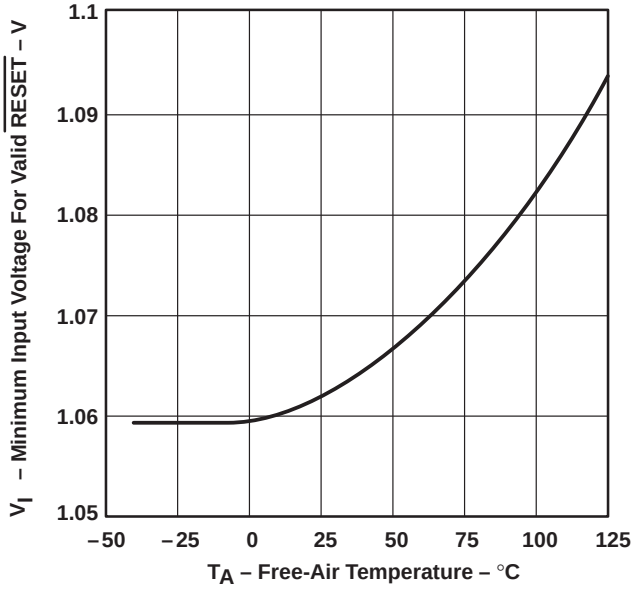


Figure 30

NEGATIVE-GOING RESET THRESHOLD vs FREE-AIR TEMPERATURE

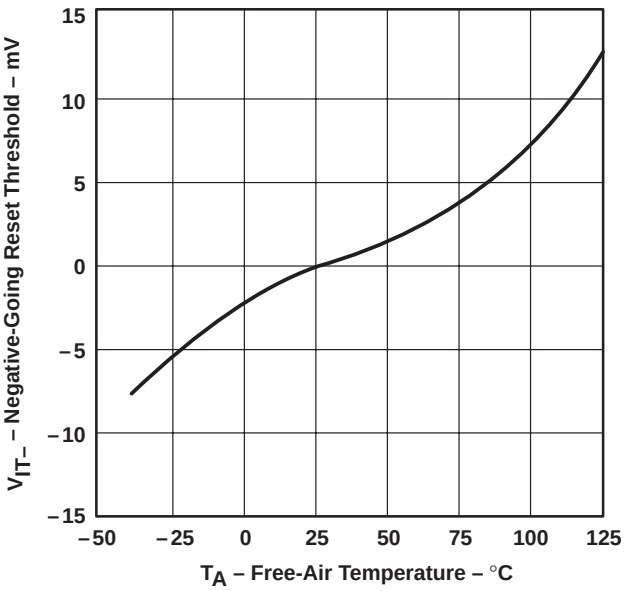


Figure 31

$\overline{\text{RESET}}$ OUTPUT CURRENT vs INPUT VOLTAGE

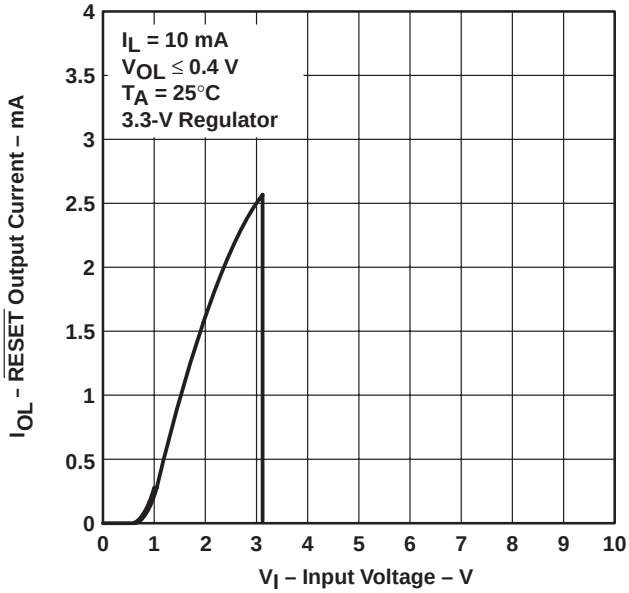


Figure 32

TYPICAL CHARACTERISTICS

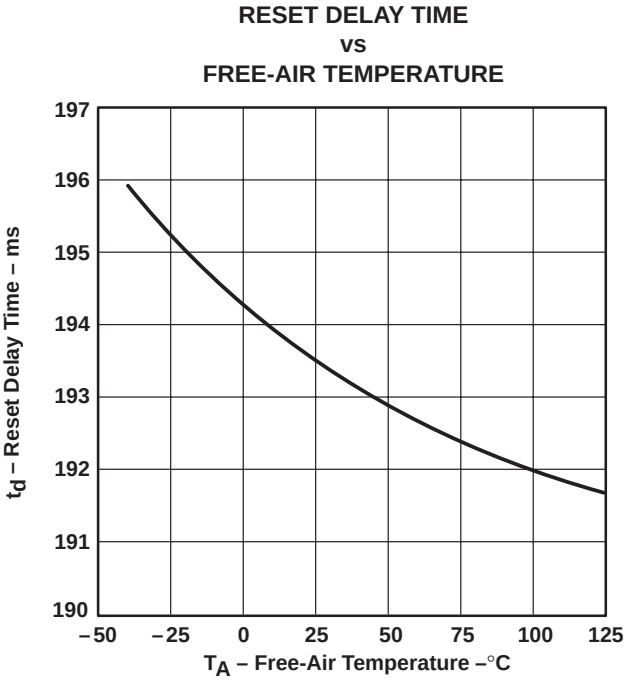


Figure 33

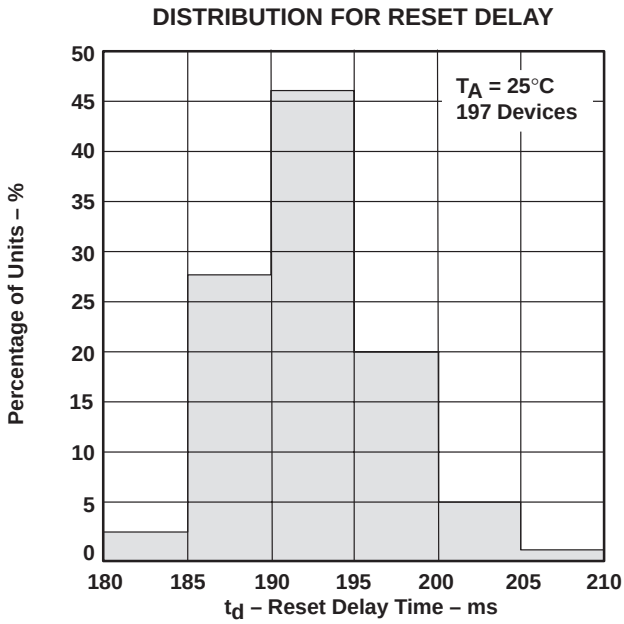


Figure 34

APPLICATION INFORMATION

Capitalizing upon the features of the TPS73xx Family (low-dropout voltage, low quiescent current, power-saving shutdown mode, and a supply-voltage supervisor) and the power-dissipation properties of the TSSOP PowerPAD package has enabled the integration of the TPS73HD301 dual LDO regulator with high output current for use in DSP and other multiple voltage applications. Figure 35 shown a typical dual-voltage DSP application

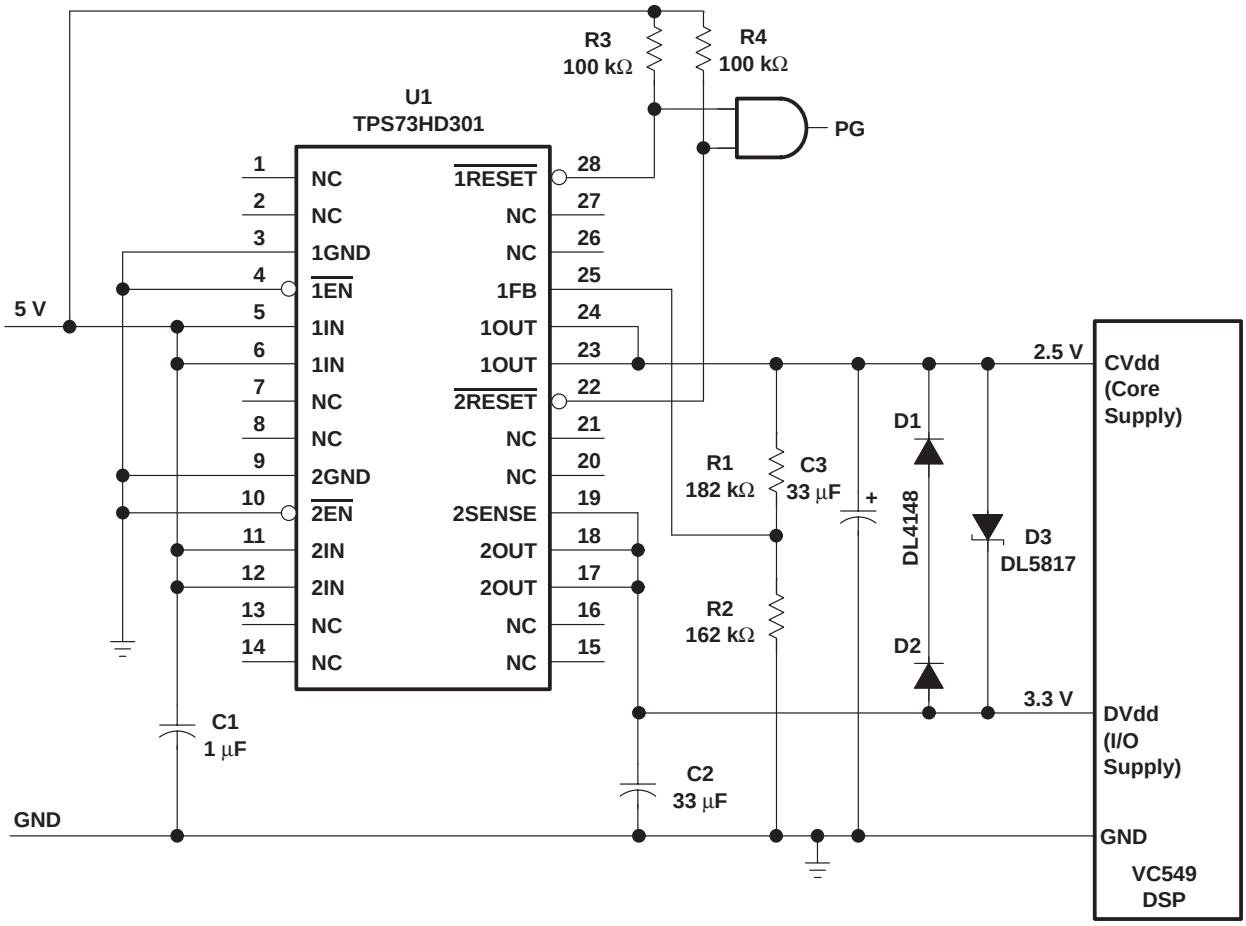


Figure 35. Dual-Voltage DSP Application

DSP power requirements include very high transient currents that must be considered in the initial design. This design uses higher-valued output capacitors to handle the large transient currents. Details of this type of design are shown in the application report, *Designing Power Supplies for TMS320VC549 DSP Systems.*

minimum load requirements

The TPS73HD301 is stable even at zero load; no minimum load is required for operation.

APPLICATION INFORMATION

SENSE connection

The SENSE terminal of fixed-output devices must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network, and noise pickup feeds through to the regulator output. It is essential to route the SENSE connection in such a way as to minimize/avoid noise pickup. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not required; however, a ceramic bypass capacitor (0.047 pF to 0.1 μF) improves load transient response and noise rejection when the TPS73HD301 is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

As with most LDO regulators, the TPS73HD301 requires an output capacitor for stability. A low-ESR 10-μF solid-tantalum capacitor connected from the regulator output to ground is sufficient to ensure stability over the full load range (see Figure 36). Adding high-frequency ceramic or film capacitors (such as power-supply bypass capacitors for digital or analog ICs) can cause the regulator to become unstable unless the ESR of the tantalum capacitor is less than 1.2 Ω over temperature. Capacitors with published ESR specifications such as the AVX TPSD106M035R0300 and the Sprague 593D106X0035D2W work well because the maximum ESR at 25°C is 300 mΩ (typically, the ESR in solid-tantalum capacitors increases by a factor of 2 or less when the temperature drops from 25°C to –40°C). Where component height and/or mounting area is a problem, physically smaller, 10-μF devices can be screened for ESR. Figures 23 through 28 show the stable regions of operation using different values of output capacitance with various values of ceramic load capacitance.

Due to the reduced stability range available when using output capacitors smaller than 10 μF, capacitors in this range are not recommended. Larger capacitors provide a wider range of stability and better load transient response. Because capacitor minimum ESR is seldom if ever specified, it may be necessary to add a 0.5-Ω to 1-Ω resistor in series with the capacitor and limit ESR to 1.5 Ω maximum. As shown in the CSR graphs (Figures 23 through 28), minimum ESR is not a problem when using 10-μF or larger output capacitors.

Below is a partial listing of surface-mount capacitors usable with the TPS73HD301. This information, along with the CSR graphs, is included to assist in selection of suitable capacitance for the user's application. When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the guidelines above.

APPLICATION INFORMATION

external capacitor requirements (continued)

All load and temperature conditions with up to 1 μF of added ceramic load capacitance:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
T421C226M010AS	Kemet	22 μF, 10 V	0.5	2.8 × 6 × 3.2
593D156X0025D2W	Sprague	15 μF, 25 V	0.3	2.8 × 7.3 × 4.3
593D106X0035D2W	Sprague	10 μF, 35 V	0.3	2.8 × 7.3 × 4.3
TPSD106M035R0300	AVX	10 μF, 35 V	0.3	2.8 × 7.3 × 4.3

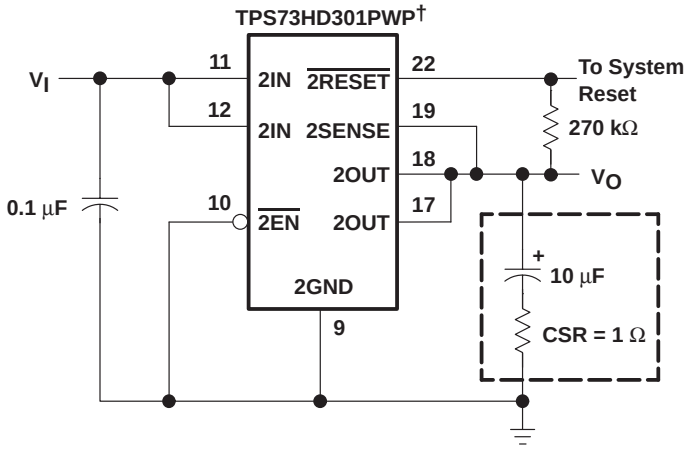
Load < 200 mA, ceramic load capacitance < 0.2 μF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
592D156X0020R2T	Sprague	15 μF, 20 V	1.1	1.2 × 7.2 × 6
595D156X0025C2T	Sprague	15 μF, 25 V	1	2.5 × 7.1 × 3.2
595D106X0025C2T	Sprague	10 μF, 25 V	1.2	2.5 × 7.1 × 3.2
293D226X0016D2W	Sprague	22 μF, 16 V	1.1	2.8 × 7.3 × 4.3

Load < 100 mA, ceramic load capacitance < 0.2 μF, full temperature range:

PART NO.	MFR.	VALUE	MAX ESR†	SIZE (H × L × W)†
195D106X06R3V2T	Sprague	10 μF, 6.3 V	1.5	1.3 × 3.5 × 2.7
195D106X0016X2T	Sprague	10 μF, 16 V	1.5	1.3 × 7 × 2.7
595D156X0016B2T	Sprague	15 μF, 16 V	1.8	1.6 × 3.8 × 2.6
695D226X0015F2T	Sprague	22 μF, 15 V	1.4	1.8 × 6.5 × 3.4
695D156X0020F2T	Sprague	15 μF, 20 V	1.5	1.8 × 6.5 × 3.4
695D106X0035G2T	Sprague	10 μF, 35 V	1.3	2.5 × 7.6 × 2.5

† Size is in mm. ESR is maximum resistance at 100 kHz and T_A = 25°C. Listings are sorted by height.



† 3.3-V fixed regulator option

Figure 36. Typical Application Circuit

APPLICATION INFORMATION

programming the adjustable LDO regulator output

Programming the adjustable regulator is done using an external resistor divider as shown in Figure 37. The equation governing the output voltage is:

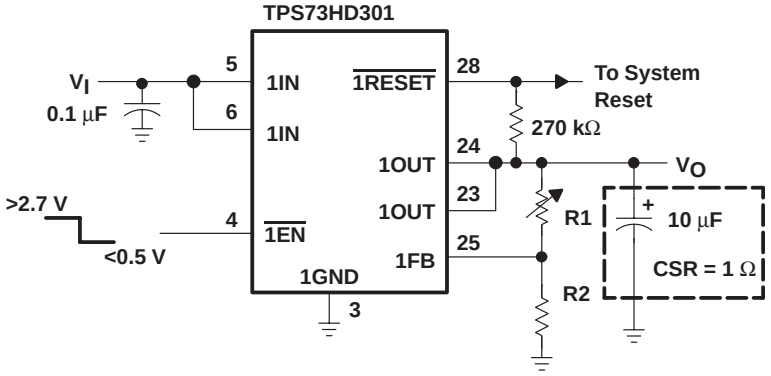
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right)$$

where

V_{ref} = reference voltage, 1.182 V typ

Resistors R1 and R2 should be chosen for approximately 7-μA divider current. A recommended value for R2 is 169 kΩ with R1 adjusted for the desired output voltage. Smaller resistors can be used, but offer no inherent advantage and consume more power. Larger values of R1 and R2 should be avoided as leakage currents at FB will introduce an error. Solving for R1 yields a more useful equation for choosing the appropriate resistance:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
1.8 V	88.7	169	kΩ
1.5 V	45.3	169	kΩ
2.5 V	191	169	kΩ
3.3 V	309	169	kΩ
3.6 V	348	169	kΩ
4 V	402	169	kΩ
5 V	549	169	kΩ
6.4 V	750	169	kΩ

Figure 37. TPS7301 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

undervoltage supervisor function

The $\overline{\text{RESET}}$ outputs of the TPS73HD301 initiate a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS73HD301 monitors the output voltage of the regulator to detect the undervoltage condition. When that occurs, the $\overline{\text{RESET}}$ output transistor turns on, taking the $\overline{\text{RESET}}$ signal low.

At programmed output voltages below 1.9 V (on the adjustable regulator only), the reset function becomes unusable. With a minimum output voltage requirement for a valid $\overline{\text{RESET}}$ signal (over temperature) being 1.9 V, $\overline{\text{RESET}}$ will not operate reliably in this range.

On power up, the output voltage tracks the input voltage. The $\overline{\text{RESET}}$ output becomes active (low) as V_I approaches the minimum required for a valid $\overline{\text{RESET}}$ signal (specified at 1.5 V for 25°C and 1.9 V over full recommended operating temperature range). When the output voltage reaches the appropriate positive-going input threshold (V_{IT+}), a 200-ms (typical) timeout period begins during which the $\overline{\text{RESET}}$ output remains low. Once the timeout has expired, the $\overline{\text{RESET}}$ output becomes inactive. Since the $\overline{\text{RESET}}$ output is an open-drain NMOS, a pullup resistor should be used to ensure that a logic-high signal is indicated.

The supply-voltage-supervisor function is also activated during power-down. As the input voltage decays and after the dropout voltage is reached, the output voltage tracks linearly with the decaying input voltage. When the output voltage drops below the specified negative-going input threshold (V_{IT-} — see electrical characteristics tables), the $\overline{\text{RESET}}$ output becomes active (low). It is important to note that if the input voltage decays below the minimum required for a valid $\overline{\text{RESET}}$, the $\overline{\text{RESET}}$ is undefined.

Since the circuit is monitoring the regulator output voltage, the $\overline{\text{RESET}}$ output can also be triggered by disabling the regulator or by any fault condition that causes the output to drop below V_{IT-}. Examples of fault conditions include a short circuit on the output and a low input voltage. Once the output voltage is reestablished, either by reenabling the regulator or removing the fault condition, then the internal timer is initiated, which holds the $\overline{\text{RESET}}$ signal active during the 200-ms (typical) timeout period.

Transient loads or line pulses can also cause a reset to occur if proper care is not taken in selecting the input and output capacitors. Load transients that are faster than 5 μs can cause a reset if high-ESR output capacitors (greater than approximately 7 Ω) are used. A 1-μs transient causes a reset when using an output capacitor with greater than 3.5 Ω of ESR. Note that the output-voltage spike during the transient can drop well below the reset threshold and still not trip if the transient duration is short. A 1-μs transient must drop at least 500 mV below the threshold before tripping the reset circuit. A 2-μs transient trips $\overline{\text{RESET}}$ at just 400 mV below the threshold. Lower-ESR output capacitors help by reducing the drop in output voltage during a transient and should be used when fast transients are expected.

NOTE:
$V_{IT+} = V_{IT-}$ +Hysteresis

output noise

The TPS73HD301 has very low output noise, with a spectral noise density < 2 μV/$\sqrt{\text{Hz}}$. This is important when noise-susceptible systems, such as audio amplifiers, are powered by the regulator.

APPLICATION INFORMATION

regulator protection

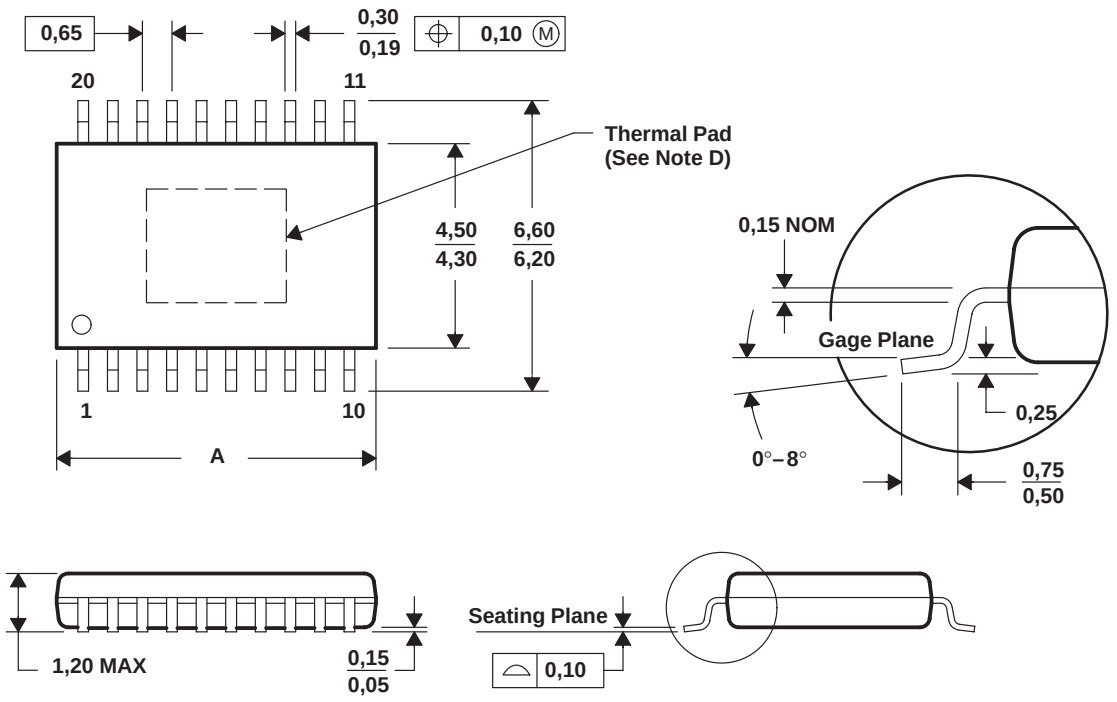
The TPS73HD301 PMOS-pass transistors have built-in back diodes that safely conduct reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS73HD301 also features internal current limiting and thermal protection. During normal operation, the TPS73HD301 limits output current to approximately 1 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled, regulator operation resumes.

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

20-PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/E 03/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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