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SLVP089 Synchronous Buck Converter Evaluation Module

User's Guide

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Preface

Read This First

About This Manual

This user's guide is a reference manual for the SLVP089 Synchronous Buck Converter Evaluation Module used to evaluate the performance of the TL5001 PWM Controller. This document provides information to assist managers and hardware engineers in application development.

How to Use This Manual

This manual provides the information and instructions necessary to design, construct, operate, and understand the SLVP089. Chapter 1 describes and lists the hardware requirements; Chapter 2 describes design considerations and procedures; and Appendix A contains the data sheet for the TL5001 PWM Controller

Related Documentation From Texas Instruments

The following books describe the TL5001 and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924. When ordering, please identify the book by its title and literature number.

TL5001 Pulse-Width-Modulation Control Circuits Data Sheet (Literature number SLVS084C). It contains electrical specifications, available temperature options, general overview of the device, and application information.

Designing with the TL5001C PWM Controller Application Report (Literature number SLVA034).

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Contents

Figures

Tables

Chapter 1

Hardware

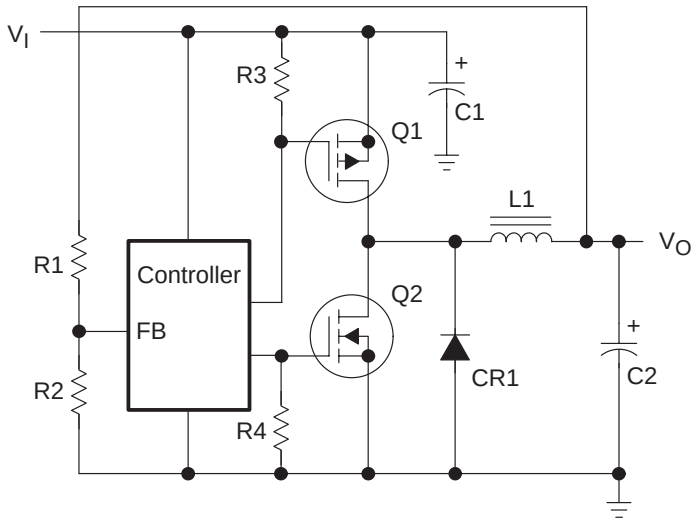
The SLVP089 Synchronous Buck Converter Evaluation Module (SLVP089) provides a method for evaluating the performance of the TL5001 pulse-width-modulation (PWM) controller. The device contains all of the circuitry necessary to control a switch-mode power supply in a voltage-mode configuration. This manual explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop. This chapter includes the following topics:

Topic **Page**

1.1 Introduction

Synchronous buck converters provide the smaller size and higher efficiency required by electronic equipment, particularly portable battery-operated equipment. The synchronous buck converter reduces power losses associated with a standard buck converter by substituting a power MOSFET for the commutating diode. This reduces the typical 0.5-V to 1-V diode drop to 0.3 V or less and increases system efficiency by up to 10 percent. Continuous-current mode is desirable and is used in this EVM for the low peak-to-average current ratio. Figure 1–1 shows a typical synchronous buck converter.

Figure 1–1. Typical Synchronous Buck Converter

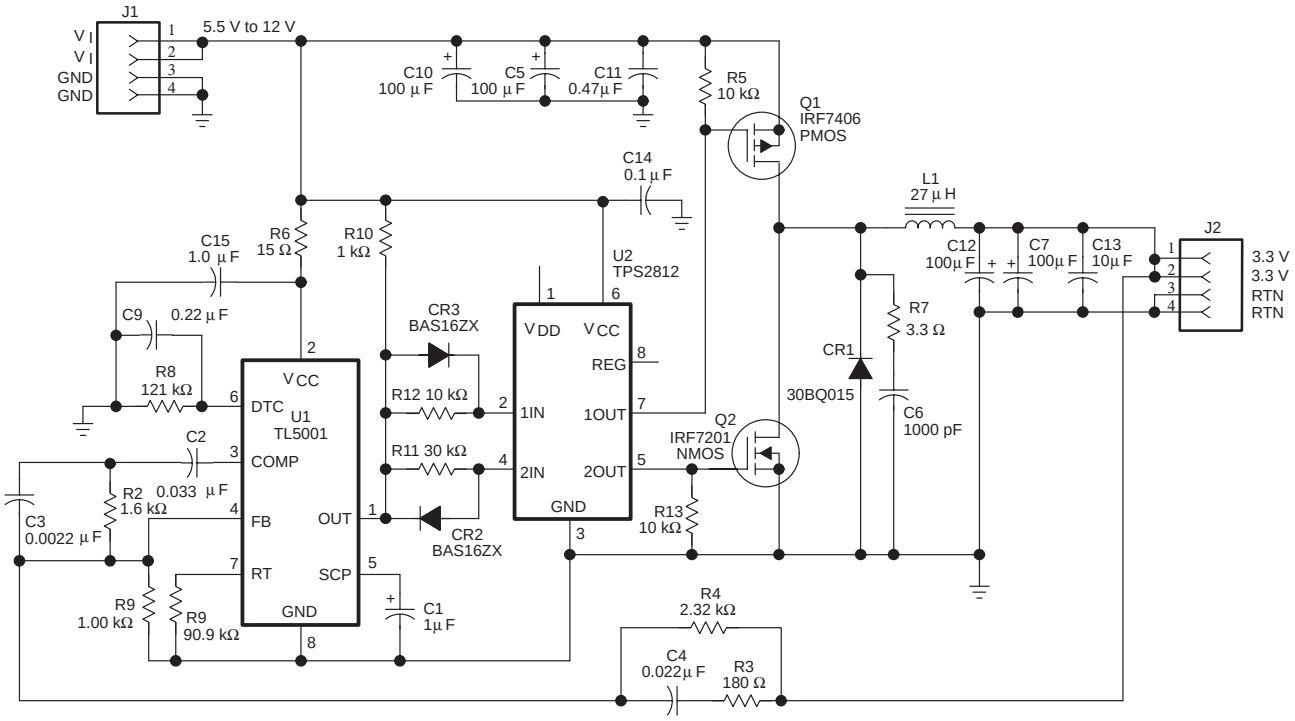


Transistor Q1 is the power switch and Q2 is the synchronous switch. A diode in parallel with Q2 allows inductor current flow during the dead time when both transistors are turned off. If dead time is not present in this configuration, high transient shoot-through currents will flow during the transition when one transistor is turning on and the other is turning off, usually resulting in destruction of the power stage switches.

The SLVP089 evaluation module will supply a nominal 3.3-V output over a load range from 0 to 3 A using a dc input voltage of 5.5 V to 12 V. Full load efficiency is typically 90 percent.

1.2 Schematic

Figure 1–2. Schematic Diagram

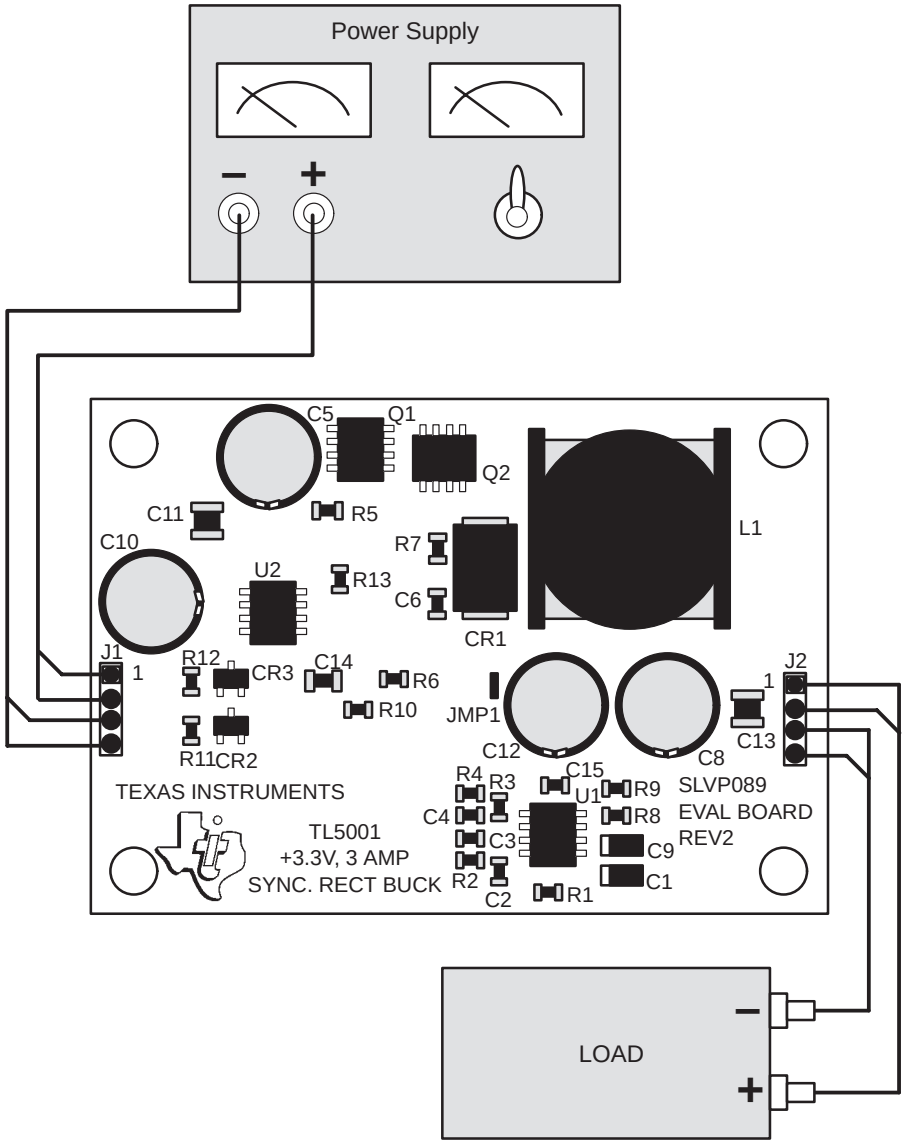


Note: Frequency is set to 100 kHz by R9. See TL5001 data sheet for the curve of oscillator frequency versus timing resistance.

1.3 Input/Output Connections

Figure 1–3 shows the input/output connections to the SLVP089.

Figure 1–3. Input/Output Connections



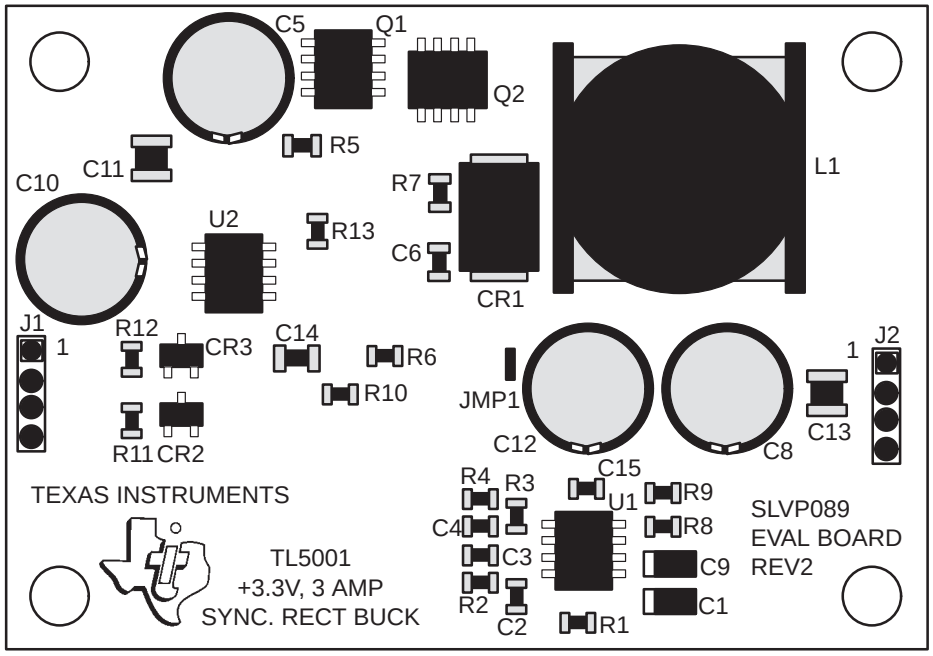
Notes: 1) Source power should be able to supply a minimum of 2.5 A at 5.5-V input and/or 1.1-A at 12-V input.

2) Load should be able to sink up to 3A with adequate power rating. Resistive loads with adequate ratings may be used.

1.4 Board Layout

Figure 1–4 shows the SLVP089 board layout.

Figure 1–4. Board Layout



1.5 Bill of Materials

Table 1–1 lists materials required for the SLVP089.

Table 1–1. Bill of Materials

Qty	Reference	Part Number	Mfr	Description
1	C1	ECS-T1CY105R	Panasonic	Capacitor, Tant, 1 μF, 20%, A Case
1	C11	Standard		Capacitor, Cer, 0.47 μF, 10%, X7R, 1210
1	C13	C3225Y5V1C106Z	TDK	Capacitor, Cer, 10 μF, 10 V, Y5V,3225
1	C14	Standard		Capacitor, Cer, 0.1 μF, 10%, X7R, 1206
1	C2	Standard		Capacitor, Cer, 0.033 μF, 10%, X7R, 1206
1	C3	Standard		Capacitor, Cer, 0.0022 μF, 10%, X7R, 0805
1	C4	Standard		Capacitor, Cer, 0.022 μF, 10%, X7R, 0805
4	C5, C7, C10, C12	TPSD107M010R0100	AVX	Capacitor, Tant, 100 μF, 10 V, D Case
1	C6	Standard		Capacitor, Cer, 1000 pF, 5%, NPO, 0805
1	C9	Standard		Capacitor, Cer, 0.22 μF, 10%, X7R, 1210
1	CR1	30BQ015	IR	Rectifier, Schottky, 3 A, 15 V
2	CR2, CR3	BAS16ZXCT	Zetex	Diode, Signal, SOT-23
2	J1, J2	Standard		Connector, 4-pin header, 25 Mil, 0.1″ Sp. Gold
1	L1	NOVA 1	Nova Mag	Inductor, 27 μH, 20%, 3A
1	Q1	IRF7406	IR	Transistor, P-CH FET, 30 V, 0.04 Ω, 4.7 A, SO-8
1	Q2	IRF7201	IR	Transistor, N-CH FET, 30 V, 0.03 Ω, 7 A, SO-8
1	R1	Standard		Resistor, 1.00 kΩ, 1%, 0805
2	R12, R13	Standard		Resistor, 10 kΩ, 5%, 0805
1	R2	Standard		Resistor, 1.6 kΩ, 5%, 0805
1	R3	Standard		Resistor, 180 Ω, 5%, 0805
1	R4	Standard		Resistor, 2.32 kΩ, 1%, 0805
1	R5	Standard		Resistor, 10 kΩ, 1%, 0805
1	R6	Standard		Resistor, 15 Ω, 5%, 0805
1	R7	Standard		Resistor, 3.3 Ω, 5%, 0805
1	R8	Standard		Resistor, 121 kΩ, 1%, 0805
1	U1	TL5001CD	TI	IC, PWM, SO-8
1	U2	TPS2812D	TI	IC, dual MOSFET driver, SO-8
1		SLVP089		PWB

1.6 Test Results

Tables 1–2 and 1–3, along with Figures 1–5 through 1–8, show the test results for the SLVP089.

Table 1–2. Line/Load Regulation, 3.3-V (Total Variation)

Line/Load		0.3 A	0.9 A	1.5 A	3.0 A	5.0 A	Load Reg.
5.5 V	Vo(V)	3.330	3.329	3.328	3.324	3.320	0.18%
6.0 V	Vo(V)	3.330	3.329	3.328	3.324	3.320	0.18%
7.0 V	Vo(V)	3.330	3.328	3.328	3.325	3.321	0.15%
8.0 V	Vo(V)	3.330	3.329	3.328	3.325	3.321	0.15%
9.0 V	Vo(V)	3.331	3.330	3.328	3.325	3.321	0.18%
10 V	Vo(V)	3.331	3.330	3.328	3.325	3.321	0.18%
11 V	Vo(V)	3.331	3.330	3.328	3.325	3.321	0.18%
12 V	Vo(V)	3.331	3.330	3.329	3.325	3.321	0.18%
Line Reg.		0.03%	0.06%	0.03%	0.03%	0.03%	

Note: The calculation for load regulation only accounts for the worst case of load variation under the normal voltage condition (i.e., 3.3 V at 3 A). All voltages were measured at the PCB header pins.

Table 1–3. Load Regulation and Ripple, 3.3-V (9-V Input)

Load	No Load	0.50 A	1.0 A	2.0 A	3.0 A	5.0 A	Reg.
Vo(V)	3.331	3.330	3.329	3.327	3.325	3.321	0.18%
Vo Ripple (mV P–P)	16	16	18	24	24	32	
Vo Spikes (mV P–P)	0	24	24	34	48	60	

Figure 1–5. Efficiency Vs Load

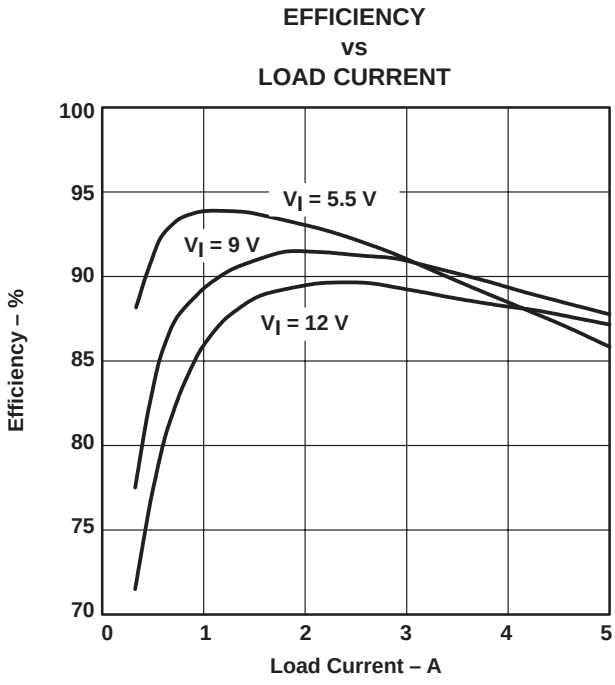


Figure 1–6. Power Switch Turn-On and Delay from Q2 Off

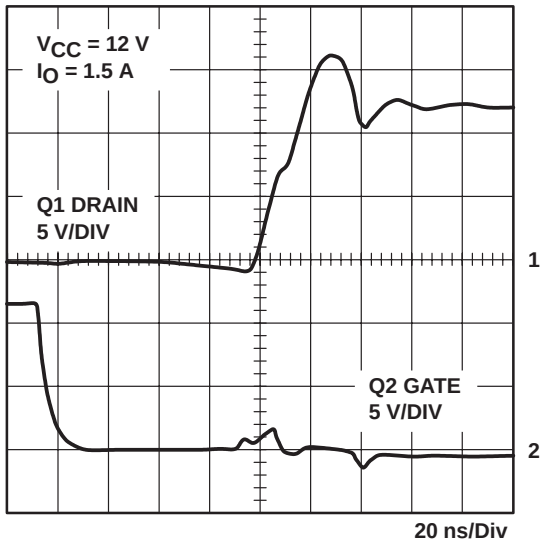


Figure 1–7. Power Switch Turn-Off and Delay to Q2 On

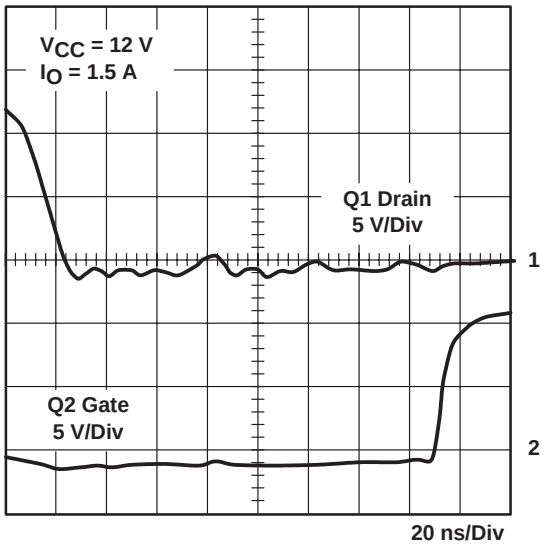
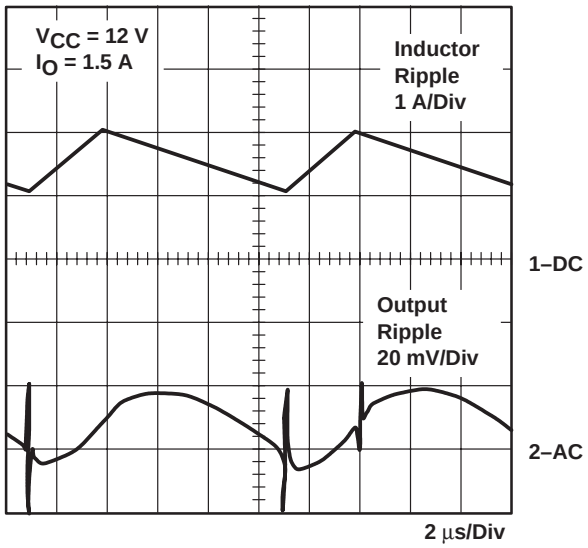


Figure 1–8. Inductor and Output Ripple



Chapter 2

Design Procedure

There are many possible ways to proceed when designing power supplies. This chapter shows the procedure used in the design of the SLVP089. The chapter includes the following topics:

Topic **Page**

2.1 Introduction

The SLVP089 is a dc-dc synchronous buck converter module that provides a 3.3-V output at up to 3 A with an input voltage range of 5.5 V to 12 V. The PWM controller is a TL5001 operating at a nominal frequency of 100 kHz. The TL5001 is configured for a maximum duty cycle of 100 percent and has short-circuit protection built in. The synchronous power stage consists of a PMOS switch and an NMOS synchronous rectifier.

2.2 Operating Specifications

Table 2–1 lists the operating specifications for the SLVP089.

Table 2–1. Operating Specifications

Specification	Min	Typ	Max	Units
Input Voltage Range	5.5		12	V
Output Voltage Range	3.10	3.30	3.50	V
Output Current Range	0		3	A
Operating Frequency		100		kHz
Output Ripple			50	mV
Efficiency (V_i = 9 V, I_O = 3 A)	85%	90%		

2.3 Design Procedures

Detailed steps in the design of a buck-mode converter may be found in *Designing With the TL5001C PWM Controller* (literature number SLVA034) from TI. This section shows the basic steps involved in this design.

2.3.1 Duty Cycle Estimate

The duty cycle for a continuous-mode step-down converter is approximately:

$$D = \frac{V_O + V_d}{V_I - V_{SAT}}$$

Assuming the diode or synchronous switch forward voltage V_d = 0.12 V and the power-switch-on voltage V_{SAT} = 0.15 V, the duty cycle for V_I = 5.5, 9, and 12 V is 0.64, 0.39, and 0.29, respectively.

2.3.2 Output Filter

A synchronous buck converter uses a single-stage LC filter. Choose an inductor to maintain continuous-mode operation down to 15 percent of the rated output load:

$$\Delta I_O = 2 \times 0.15 \times I_O = 2 \times 0.15 \times 3 = 0.9\ A$$

The inductor value is:

$$L = \frac{\left(V_I - V_{SAT} - V_O\right) \times D \times t}{\Delta I_O}$$

$$= \frac{(12 - 0.15 - 3.3) \times 0.29 \times \left(10 \times 10^{-6}\right)}{0.9} = 27.6\ \mu H$$

Assuming that all of the inductor ripple current flows through the capacitor and the effective series resistance (ESR) is zero, the capacitance needed is:

$$C = \frac{\Delta I_O}{8 \times f \times \left(\Delta V_O\right)} = \frac{0.9}{8 \times \left(100 \times 10^3\right) \times 0.05} = 22.5\ \mu F$$

Assuming the capacitance is very large, the ESR needed to limit the ripple to 50 mV is:

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05}{0.9} = 0.056\ \Omega$$

The output filter capacitor should be rated at least ten times the calculated capacitance and 30–50 percent lower than the calculated ESR. This design used two 100-μF capacitors in parallel with a multilayer ceramic to reduce ESR.

2.3.3 Power Switch

Based on the preliminary estimate, $r_{DS(ON)}$ should be less than 0.015 V ÷ 3A = 50 mΩ. The IRF7406 is a 30-V p-channel MOSFET with $r_{DS(ON)}$ = 40 mΩ.

The power dissipation (conduction + switching losses) can be approximated as:

$$P_D = \left(I_O^2 \times r_{DS(ON)} \times D\right) + \left(0.5 \times V_I \times I_O \times t_{r+f} \times f\right)$$

Assuming total switching time, t_{r+f}, = 100 ns, a 55°C maximum ambient temperature, and $r_{DS(ON)}$ adjustment factor = 1.6, then:

$$P_D = \left[3^2 \times (0.04 \times 1.6) \times 0.64\right] + \left[0.5 \times 5.5 \times 3 \times \left(0.1 \times 10^{-6}\right) \times \left(100 \times 10^3\right)\right] = 0.45\ W$$

The thermal impedance for Q1 $R_{\theta JA}$ = 90°C/W for FR-4 with 2-oz. copper and a one-inch-square pattern, thus:

$$T_J = T_A + \left(R_{\theta JA} \times P_D\right) = 55 + (90 \times 0.45) = 96°C$$

2.3.4 Synchronous Switch and Rectifier

The synchronous switch calculations follow the same path as the power switch except that the duty cycle is 1–D. Then $r_{DS(ON)}$ should be less than 0.012 V÷ 3A = 40 mΩ. Selecting an IRF7201 with an $r_{DS(ON)}$ = 30 mΩ, then:

$$P_D = \left[3^2 \times (0.03 \times 1.6) \times 0.36\right] + \left[0.5 \times 5.5 \times 3 \times \left(0.1 \times 10^{-6}\right) \times \left(100 \times 10^3\right)\right] = 0.238\ W$$

$$T_J = T_A + \left(R_{\theta JA} \times P_D\right) = 55 + (90 \times 0.238) = 76°C$$

The catch rectifier serves as a backup device for the synchronous switch and conducts during the time interval when both devices are off. The 30BQ015 is a 3-A, 15-V rectifier in an SMC power surface-mount package. If the synchronous switch were not used, the power dissipation for the catch diode would be:

$$P_D = I_O \times V_D \left(1 - D_{Min}\right) = 3 \times 0.7 \times 0.71 = 1.491\ W$$

However, since the catch diode actually conducts only during the deadtime and switching time, the power dissipation is:

$$P_D = I_O \times V_D \times t_{r+f} \times f = 3 \times 0.7 \times \left(0.1 \times 10^{-6}\right) \times \left(100 \times 10^3\right) = 2.1\ mW$$

2.3.5 Snubber Network

A snubber network is usually needed to suppress the ringing at the node where the power switch drain, output inductor, and synchronous switch drain connect. This is usually a trial-and-error sequence of steps to optimize the network, but as a starting point, select a snubber capacitor with a value that is 4–10 times larger than the estimated capacitance of the synchronous switch and catch rectifier. Then, measuring a ringing time constant of 3 ns, R is:

$$R = \frac{3 \times 10^{-9}}{C} = \frac{3 \times 10^{-9}}{1000 \times 10^{-12}} = 3\ \Omega$$

2.3.6 Controller Functions

The controller functions, oscillator frequency, soft-start, dead-time-control, short-circuit protection, and sense-divider-network are discussed in this section.

The oscillator frequency is set by selecting the resistance value from the graph in figure 6 of the TL5001 data sheet. For 100 kHz, a value of 90.9 kΩ is selected.

Dead-time control provides a minimum off-time for the power switch in each cycle. Set this time by connecting a resistor between DTC and GND. For this design, a maximum duty cycle of 100% is chosen. Then R8 is calculated as:

$$R8 = (R9 + 1.25) \times 10^3 \times \left[D\left(V_{O(100\%)} - V_{O(0\%)} \right) + V_{O(0\%)} \right]$$

$$= (90.9 + 1.25) \times 10^3 \times [1(1.3 - 0.65) + 0.65]$$

$$= 119.8\ K\Omega \Rightarrow 121\ k\Omega$$

Soft-start is added to reduce power-up transients. This is implemented by adding a capacitor across the dead-time resistor. In this design, a soft-start time of 25 ms is used:

$$C = \frac{t_R}{R_{DT}} = \frac{0.025\ s}{121\ k\Omega} = 0.21\ \mu F$$

The TL5001 has short circuit protection instead of a current sense circuit. If not used, the SCP terminal must be connected to ground to allow the converter to start up. If a timing capacitor is connected to SCP, it should have a time constant that is greater than the soft-start time constant. This time constant is chosen to be 75 ms:

$$C(\mu F) = 12.46 \times t_{SCP} = 12.46 \times 0.075\ s = 0.93\ \mu F$$

2.3.7 Loop Compensation

Loop compensation is necessary to stabilize the converter over the full range of load, line, and gain conditions. A buck-mode converter has a two-pole LC output filter with a 40-dB-per-decade rolloff. The total closed-loop response needed for stability is a 20-dB-per-decade rolloff with a minimum phase margin of 30 degrees over the full bandwidth for all conditions. In addition, sufficient bandwidth must be designed into the circuit to assure that the converter will have good transient response. Both of these requirements are achieved by adding compensation components around the error amplifier to modify the total loop response.

The first step in design of the loop compensation network is the design of the output sense divider. This sets the output voltage and the top resistor determines the relative size of the rest of the compensation design. Since the TL5001 input bias current is 0.5 μA (worst case), the divider current should be at least 0.5 mA. Using a 1-kΩ resistor for the bottom of the divider gives a divider current of 1 mA. The top of the divider is calculated as:

$$R = \frac{\left(V_O - 1 \right)}{1\ mA} = \frac{(3.3\ -1)}{0.001} = 2.3\ k\Omega$$

Calculating the pulse-width-modulator gain as the change in output voltage divided by the change in PWM input voltage gives:

$$A_{PWM} = \frac{\Delta V_O}{\Delta V_{COMP}} = \frac{9 - 0}{1.3 - 0.65} = 13.85 \Rightarrow 22.8\ db$$

The LC filter has a double pole at:

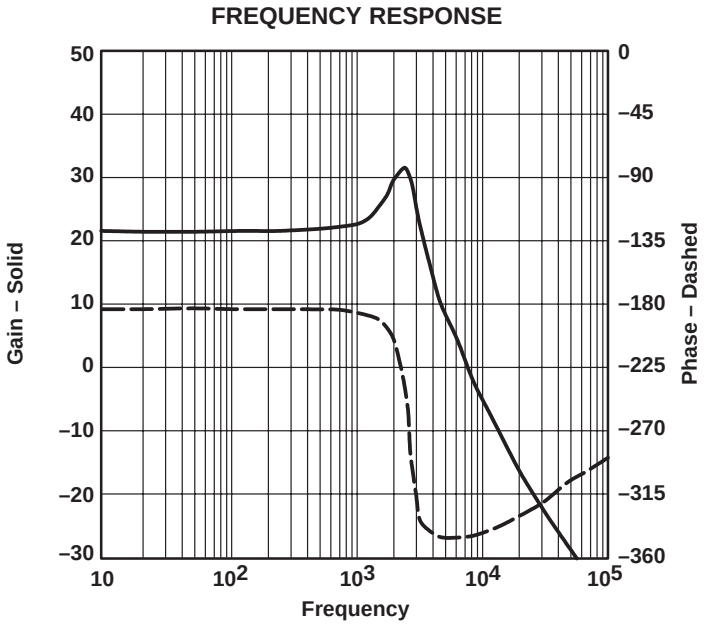
$$\frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{21.6\ \mu H \times 168\ \mu F}} = 2.64\ kHz$$

(worst case values) and rolls off at 40-dB per decade after that until the ESR zero is reached at:

$$\frac{1}{2\pi RC} = \frac{1}{2\pi(0.025)\left(210 \times 10^{-6}\right)} = 38\ kHz$$

This information is enough to calculate the required compensation values. Figure 2–1 shows the power stage gain and phase plots.

Figure 2–1. Power Stage Bode Plot

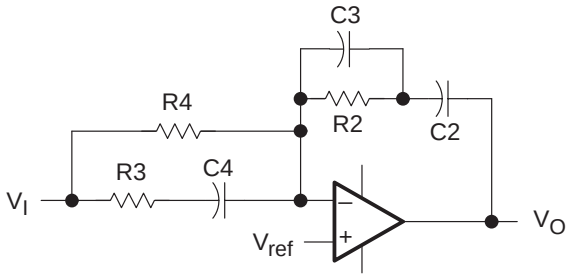


This response must be corrected by addition of the following:

- ❑ A pole at zero to give high dc gain
- ❑ Two zeroes at approximately 2.6 kHz to cancel the LC poles
- ❑ A pole at approximately 38 kHz to cancel the ESR zero
- ❑ A final pole to roll off high-frequency gain

The compensation circuit shown in figure 2–2 can be used to implement the above conditions.

Figure 2–2. Compensation Network



The transfer function for this circuit is:

$$\frac{V_O}{V_I} = \frac{[1 + sR2(C2 + C3)]\,[1 + sC4(R3 + R4)]}{sC2R4\,[1 + sC3R2]\,[1 + sC4R3]} = \frac{(f_{Z1})(f_{Z2})}{(f_{P1})(f_{P2})(f_{P3})}$$

The desired output regulation is ±6 percent total deviation. The PWM controller tolerance is ±5 percent, and the divider resistors are 1 percent; therefore, the control loop must be very precise. A minimum dc gain of 1000 (60 dB) gives a 0.1 percent tolerance. The integrator (R4, C2) sets the gain of the compensation network. The minimum modulator gain is 18 dB, therefore the compensation network must have a gain of at least 42 dB. With a desired crossover frequency of 20 kHz and a desired slope of 20 dB per decade, choose an integrator frequency of 2 kHz. This gives a gain of 46 dB at 10 Hz, which is sufficient for this application. If more gain is needed, increase the integrator frequency. R4 is already known, so C2 is calculated as:.

$$C2 = \frac{1}{2\pi(f_{P1})(R4)} = \frac{1}{2\pi(2\ kHz)(2.32\ k\Omega)} = 0.034\ \mu F \Rightarrow 0.033\ \mu F$$

Setting f_{Z2} = 3 kHz to compensate for one of the LC poles gives:

$$C4 = \frac{1}{2\pi(f_{Z2})(R4)} = \frac{1}{2\pi(3\ kHz)(2.32\ k\Omega)} = 0.023\ \mu F \Rightarrow 0.022\ \mu F$$

Now R3 can be calculated using f_{P3} (40 kHz), the ESR compensator:

$$R3 = \frac{1}{2\pi(f_{P3})(C4)} = \frac{1}{2\pi(40\ kHz)(0.022\ \mu F)} = 181\ \Omega \Rightarrow 180\ \Omega$$

The other LC filter compensator uses R2 and C2:

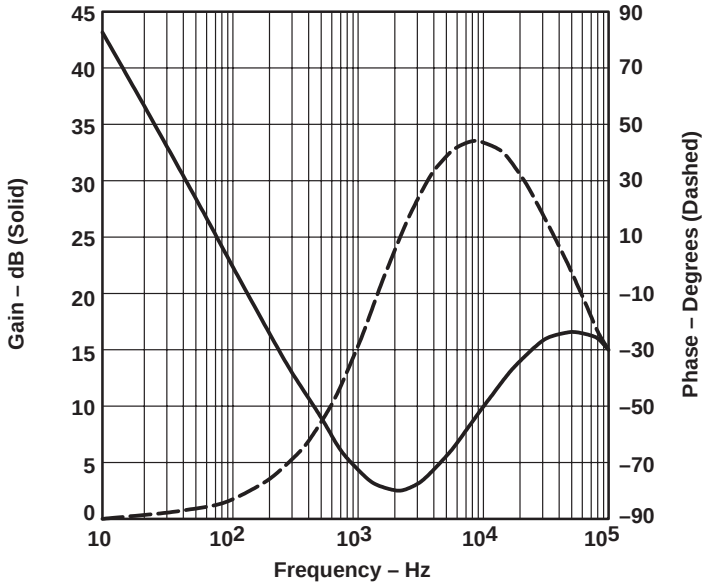
$$R2 = \frac{1}{2\pi(f_{Z1})(C2)} = \frac{1}{2\pi(3\ kHz)(0.033\ \mu F)} = 1.6\ k\Omega$$

The final rolloff pole (selected at 50 kHz) uses C3 and R2:

$$C3 = \frac{1}{2\pi(f_{P2})(R2)} = \frac{1}{2\pi(50\ kHz)(1.6\ k\Omega)} = 0.002\ \mu F \Rightarrow 0.0022\ \mu F$$

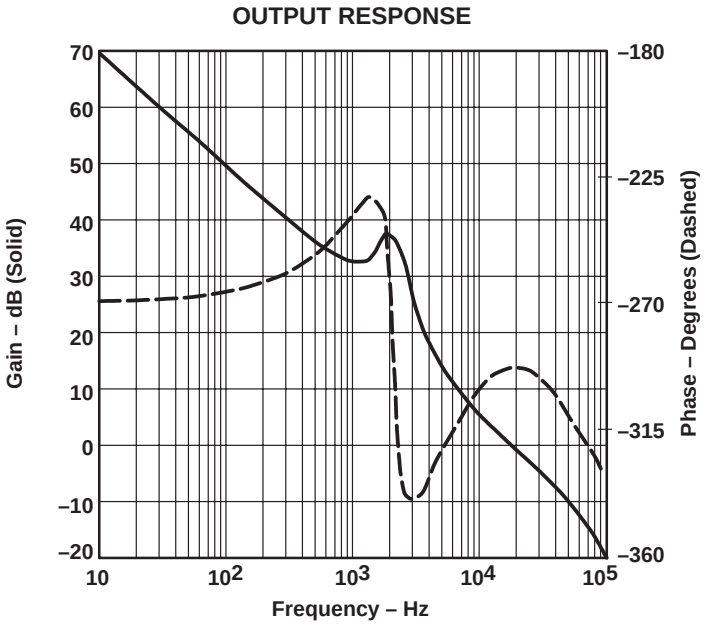
Figure 2–3 shows the bode plot for the compensation network.

Figure 2–3. Bode Plot



Note from the output response shown in Figure 2–4 that the minimum phase margin is 40 degrees and the bandwidth is 18 kHz under nominal operating conditions.

Figure 2–4. Output Response



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