SLVP097 Buck Converter Evaluation Module User's Guide

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Preface

Read This First

About This Manual

This user's guide is a reference manual for the SLVP097 Buck Converter Evaluation Module. This document provides information to assist managers and hardware engineers in application development.

How to Use This Manual

This manual provides the information and instructions necessary to design, construct, operate, and understand the SLVP097. Chapter 1 describes and lists the hardware requirements; Chapter 2 describes design considerations and procedures.

Related Documentation From Texas Instruments

The following books describe the TL5001 and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924. When ordering, please identify the book by its title and literature number.

TL5001 Pulse-Width-Modulation Control Circuits Data Sheet (Literature number SLVS084C).

Designing with the TL5001C PWM Controller Application Report (Literature number SLVA034).

TPS2816, TPS2817, TPS2818, and TPS2819 Single-Channel High-Speed MOSFET Driver Data Sheet (Literature number SLVS160)

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Figures

Chapter 1

Hardware

The SLVP097 Buck Converter Evaluation Module (SLVP097) provides a method for evaluating the performance of a buck converter using the TL5001 pulse-width-modulation (PWM) controller coupled with a TPS2817 MOSFET driver. This manual explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop. This chapter includes the following topics:

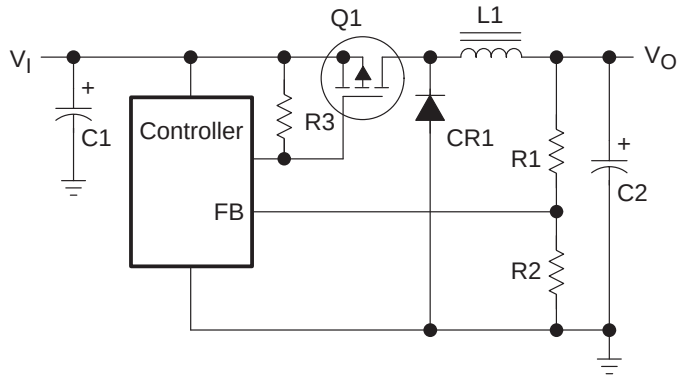
Topic **Page**

1.1 Introduction

Low cost and design simplicity make buck converters popular solutions in dc/dc step-down applications where lack of isolation from the input source is not a concern. Loop compensation for the buck converter can be set for high bandwidths. This mode is desirable for the low peak-to-average current ratio, easing the component worst-case design parameters.

Figure 1–1 shows a block diagram of a typical buck converter. The converter passes a duty-cycle modulated waveform through a low-pass output filter. To maintain the desired output voltage, a controller senses the output voltage, compares it to an internal reference voltage and adjusts the width of the power switch (Q1) on time, . A commutating diode (CR1) maintains continuous current through the inductor when the power switch is turned off.

Figure 1–1. Typical Buck Converter Block Diagram



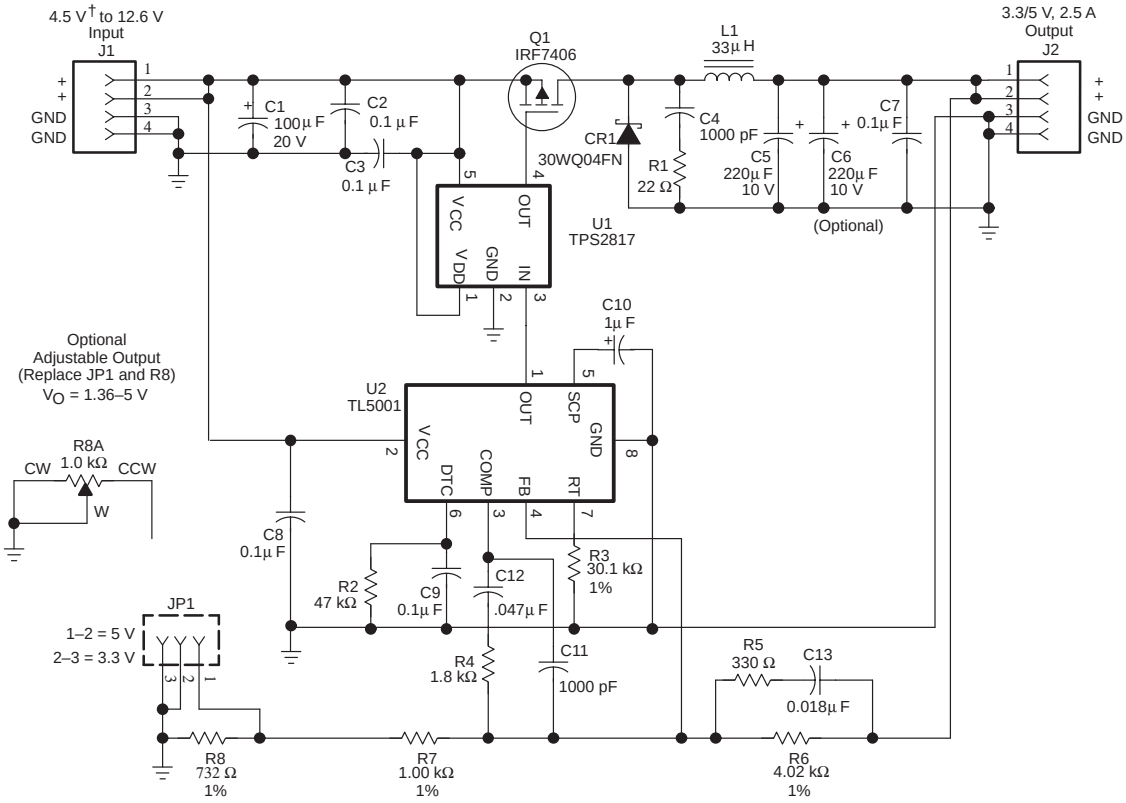
The SLVP097 buck converter uses the TI TL5001 PWM controller and the TPS2817 MOSFET driver to give a 0- to 2.5-A output with a selectable output voltage of either 3.3 V or 5 V. The converter operates over an input voltage range of 5.5 V to 12 V with a typical efficiency of 90 percent. Chapter 2 lists full design specifications.

Note: Peak currents in excess of 2.5 A may be obtained from this EVM, but due to thermal restraints, should not be subtained. This EVM shuts down when a short circuit is encountered. Input power must be recycled to restart the module.

1.2 Schematic

Figure 1–2 shows the SLVP097 schematic.

Figure 1–2. SLVP097 Schematic



† Input voltage range for 3.3 V output. When using 5-V output, minimum input voltage must be greater than 5.5 V.

Notes: 1) Frequency set to 275 kHz by R3.

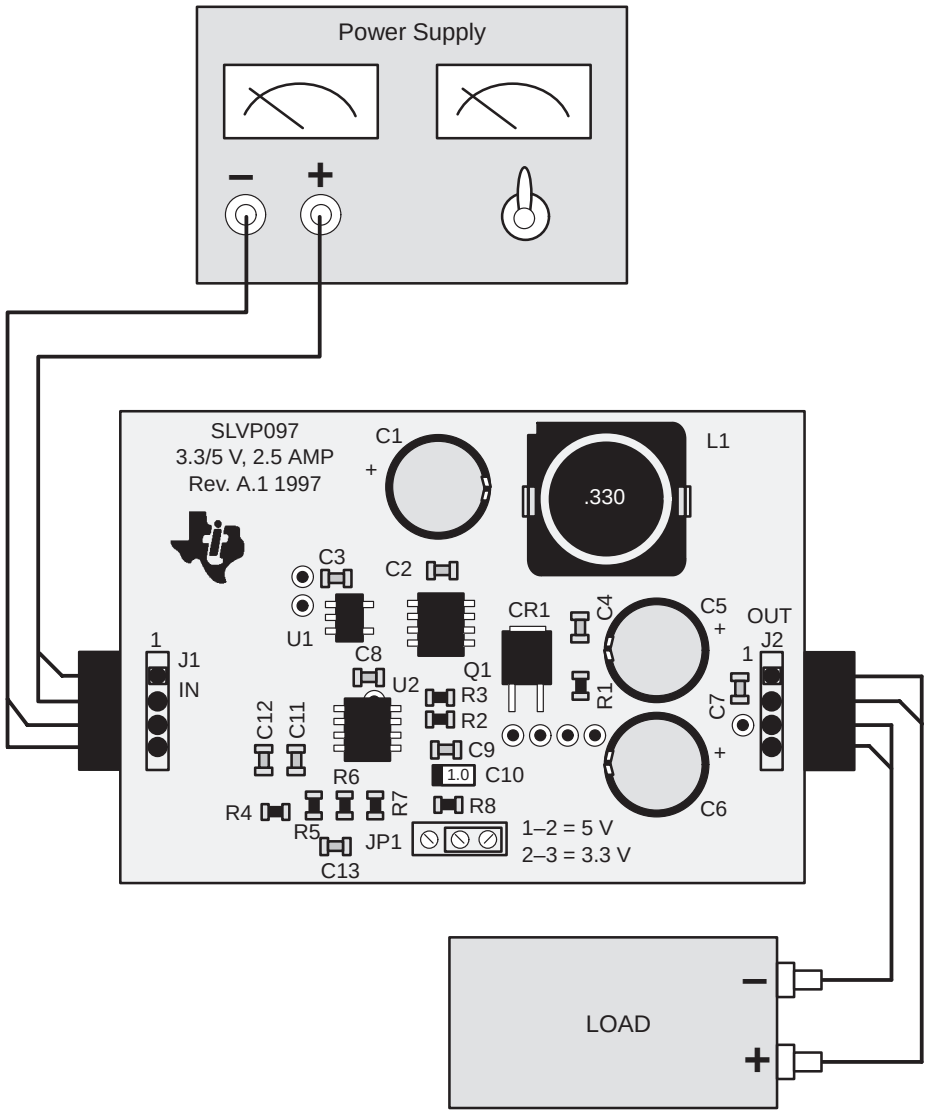
2) This unit and the components are thermally rated to 2.5 A. The output current should not exceed 2.5 A unless proper thermal management is put in place.

3) DO NOT change the set output voltage jumper (JP1) while power is applied to the unit.

1.3 Input/Output Connections

Figure 1–3 shows the SLVP097 input and output connections.

Figure 1–3. I/O Connections



Notes: 1) The input power supply should be rated at least 3 A with current limit set high enough for proper operation.
2) The load should be rated at least 2.5 A with proper power dissipation. Fixed or variable resistors may be used.

1.4 Board Layout

Figures 1–4 through 1–6 show the SLVP097 board layout.

Figure 1–4. Board Layout

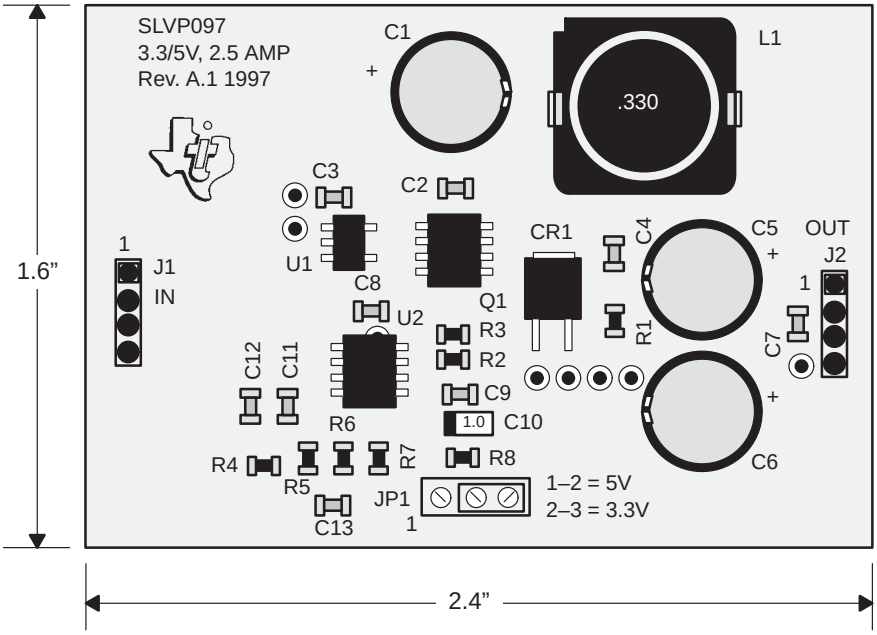


Figure 1–5. Top Layer

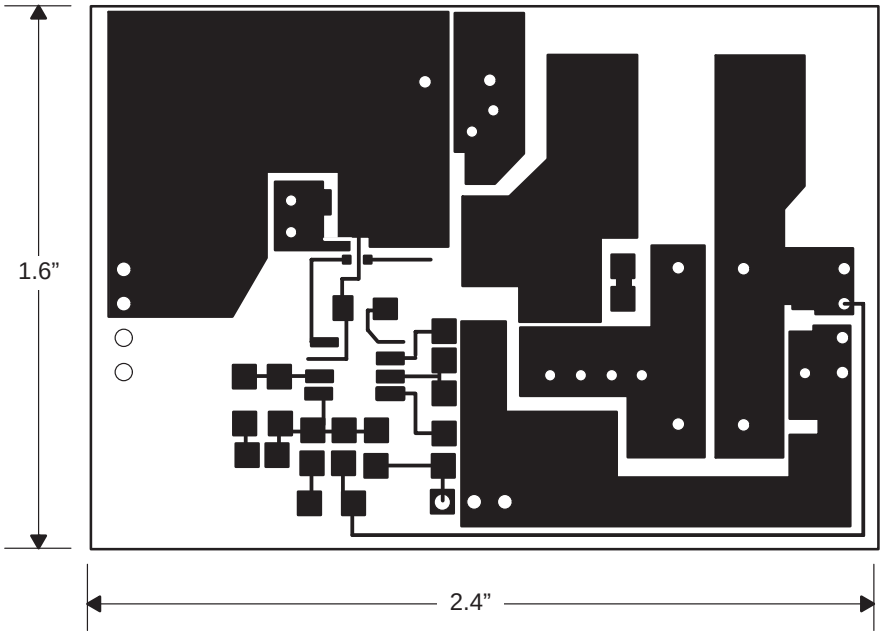
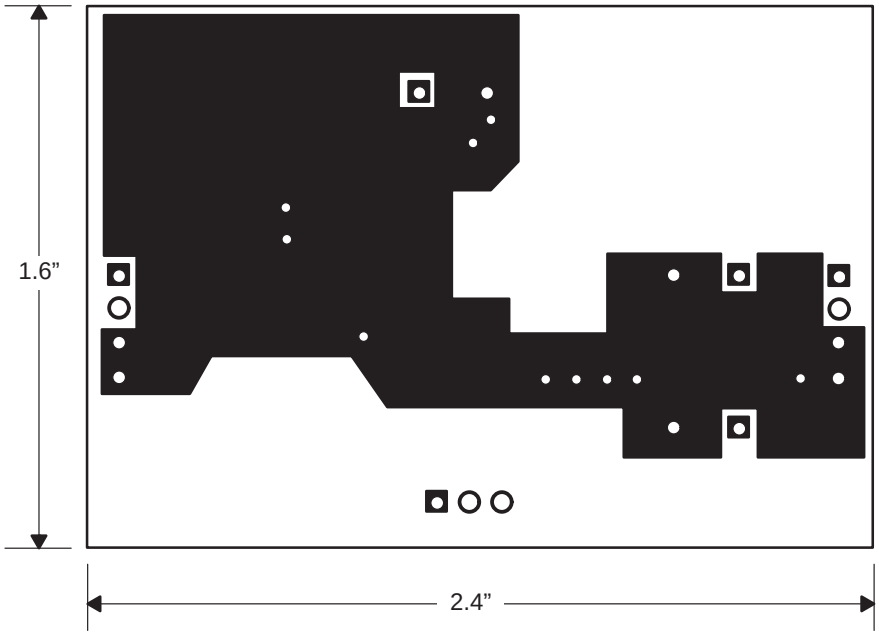


Figure 1–6. Bottom Layer



1.5 Bill of Material

Table 1–1 lists materials required for the SLVP097.

Table 1–1. Bill of Materials

Reference	Part Number	Mfr	Description
C1	20SA100M	Sanyo	Capacitor, Os-Con, 100 μF, 20 V, F-case
C2			Capacitor, Ceramic, 0.1 μF, 50 V, 1206
C3			Capacitor, Ceramic, 0.1 μF, 50 V, 1206
C4			Capacitor, Ceramic, 1000 pF, 50 V, 1206
C5	10SA220M	Sanyo	Capacitor, Os-Con, 220 μF, 10 V, F-case
C6*	10SA220M	Sanyo	Capacitor, Os-Con, 220 μF, 10 V, F-case
C7			Capacitor, Ceramic, 0.1 μF, 50 V, 1206
C8			Capacitor, Ceramic, 0.1 μF, 50 V, 1206
C9			Capacitor, Ceramic, 0.1 μF, 50 V, 1206
C10	ECS-T1EY105R	Digikey	Capacitor, Tantalum, 1.0 μF, 25 V, 1206
C11			Capacitor, Ceramic, 1000 pF, 50 V, 1206
C12			Capacitor, Ceramic, 0.047 μF, 50 V, 1206
C13			Capacitor, Ceramic, 0.018 μF, 50 V, 1206
CR1	30WQ04FN	IR	Diode, Schottky, 3.3 A, 40 V, D-Pak
J1			Header, 4-pin, 0.025” sq × 0.100” centers
J2			Header, 4-pin, 0.025” sq × 0.100” centers
JP1			Header, 3-pin, 0.025” sq × 0.100” centers
L1	SLF12565-330M2R8	TDK	Inductor, 33 μH, 2.8 A, 0.041 Ω, 0.50” square
Q1	IRF7406		MOSFET, P-Ch, 30 V, 0.045 Ω, 4.7 A, SO-8
R1			Resistor, CF, 22 Ω, 1/10 W, 5%, 1206
R2			Resistor, CF, 47 kΩ, 1/10 W, 5%, 0805
R3			Resistor, MF, 30.1 kΩ, 1/10 W, 1%, 0805
R4			Resistor, CF, 1.8 kΩ, 1/10 W, 5%, 0805
R5			Resistor, CF, 330 Ω, 1/10 W, 5%, 0805
R6			Resistor, MF, 4.02 kΩ, 1/10 W, 1%, 0805
R7			Resistor, MF, 1.00 kΩ, 1/10 W, 1%, 0805
R8			Resistor, MF, 732 Ω, 1/10 W, 1%, 0805
R8A*	CT9W102-ND	Digikey	Potentiometer, 1 kΩ, 10%, 18-turn, 9mm-square
U1	TPS2817DBV	TI	MOSFET driver, noninverting, single channel, SOT-25
U2	TL5001CD	TI	PWM controller, SO-8
—			Shunt, standard profile
—	SLVP097	TI	PCB, TPS2817 EVM, 2.40” × 1.60”

* Optional parts not on present board.

1.6 Test Results

Figures 1–7 through 1–11 show test results for the the SLVP097.

Figure 1–7. Output Voltage Vs Output Current (3.3-V Mode)

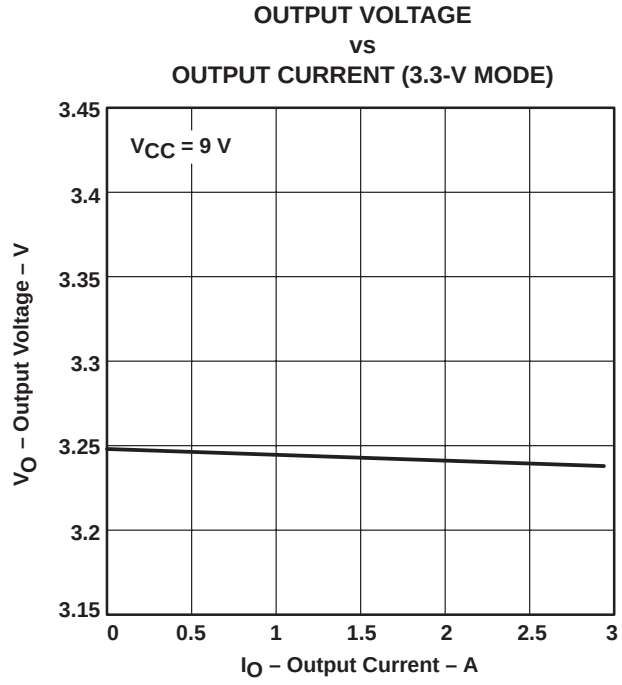


Figure 1–8. Output Voltage Vs Output Current (5-V Mode)

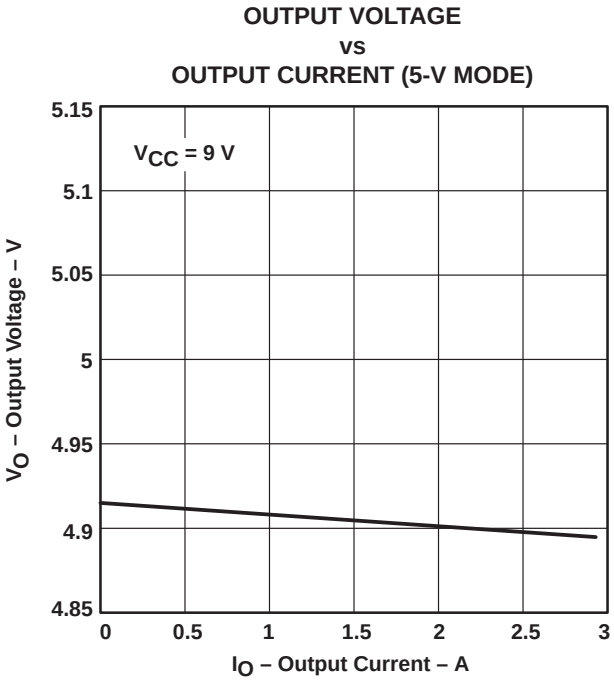


Figure 1–9. Output Voltage Vs Supply Voltage (3.3-V Mode)

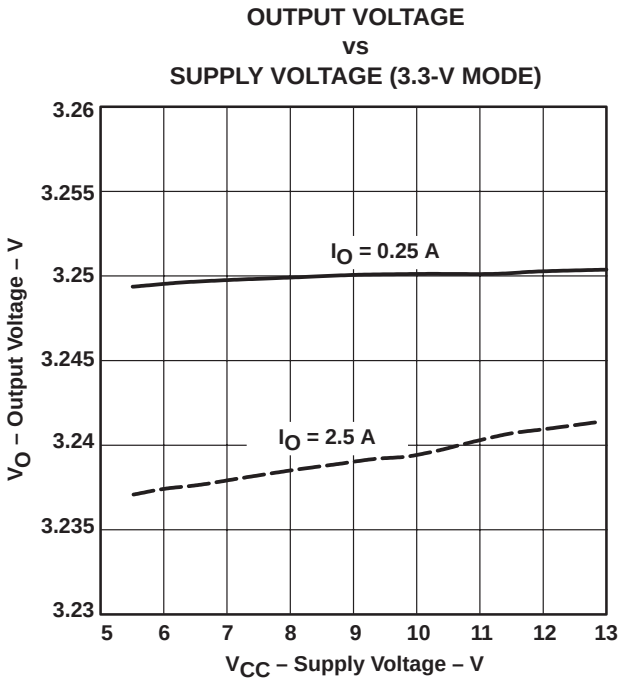


Figure 1–10. Output Voltage Vs Supply Voltage (5-V Mode)

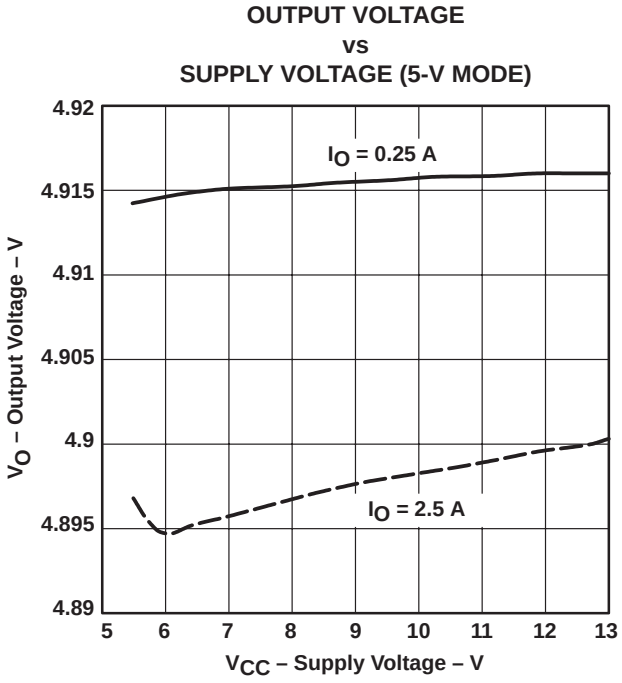
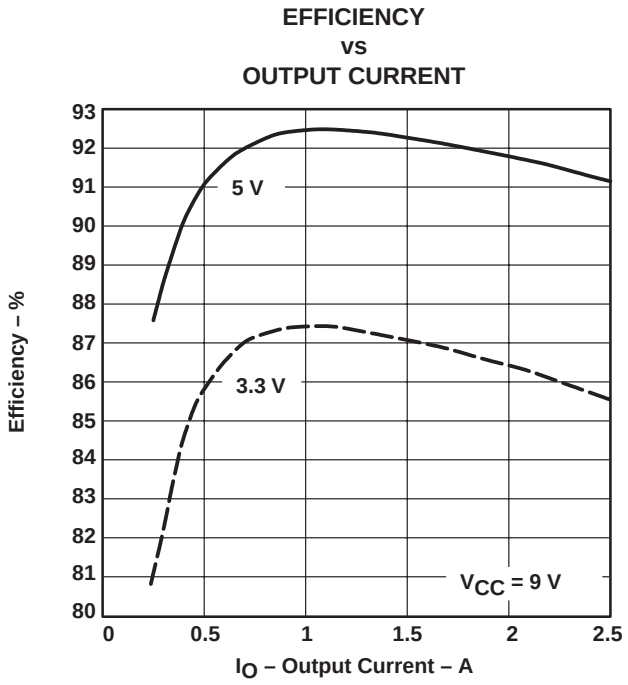


Figure 1–11. Efficiency Vs Output Current (5-V Mode)



Chapter 2

Design Procedure

The SLVP097 evaluation module provides a method for evaluating the performance of the TPS2817 MOSFET driver and the TL5001 PWM controller. The TPS2817 contains all of the circuitry necessary to drive large MOSFETs, including a voltage regulator for higher voltage applications. This section explains how to construct basic power conversion circuits including the design of the control chip functions and the basic loop. This chapter includes the following topics:

Topic **Page**

2.1 Introduction

The SLVP097 is a dc-dc buck converter module that provides a 5-V or 3.3-V output at up to 2.5 A with an input voltage range of 5.5 V to 12 V. The controller is a TL5001 PWM operating at a nominal frequency of 275 kHz. The TL5001 is configured for a maximum duty cycle of 100 percent and has short-circuit protection built in. Output voltage selection is implemented with jumper JP1.

2.2 Operating Specifications

Table 2–1 lists the operating specifications for the SLVP097.

Table 2–1. Operating Specifications

Specification	Min	Typ	Max	Units
Input Voltage Range	4.5†		12.6	V
Output Voltage Range				
5-V Mode	4.7	5.0	5.3	V
3.3-V Mode	3.1	3.3	3.5	V
Output Current Range	0		2.6	A
Operating Frequency		275		kHz
Output Ripple			50	mV
Efficiency	85%	90%		

† For 3.3 V only, minimum input voltage for 5 V output is 5.5 V.

2.3 Design Procedures

Detailed steps in the design of a buck-mode converter may be found in *Designing With the TL5001C PWM Controller* (literature number SLVA034) from Texas Instruments. This section shows the basic steps involved in this design, using the 3.3-V output mode.

2.3.1 Duty Cycle Estimate

The duty cycle for a continuous-mode step-down converter is approximately:

$$D = \frac{V_O + V_d}{V_I - V_{SAT}}$$

Assuming the commutating diode forward voltage V_d = 0.5 V and the power switch on voltage V_{SAT} = 0.1 V, the duty cycle for V_i = 5.5, 9, and 12 V is 0.70, 0.42, and 0.32, respectively.

2.3.2 Output Filter

A buck converter uses a single-stage LC filter. Choose an inductor to maintain continuous-mode operation down to 6 percent of the rated output load:

$$\Delta I_O = 2 \times 0.06 \times I_O = 2 \times 0.06 \times 2.5 = 0.30 \text{ A}$$

The inductor value is:

$$L = \frac{(V_I - V_{SAT} - V_O) \times D \times t}{\Delta I_O}$$

$$= \frac{(12 - 0.1 - 3.3) \times 0.32 \times \left(3.63 \times 10^{-6}\right)}{0.30} = 33.3 \ \mu\text{H}$$

Assuming that all of the inductor ripple current flows through the capacitor and the effective series resistance (ESR) is zero, the capacitance needed is:

$$C = \frac{\Delta I_O}{8 \times f \times \left(\Delta V_O\right)} = \frac{0.3}{8 \times \left(275 \times 10^3\right) \times 0.05} = 2.73 \ \mu\text{F}$$

Assuming the capacitance is very large, the ESR needed to limit the ripple to 50 mV is:

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05}{0.3} = 0.167 \ \Omega$$

The output filter capacitor should be rated at least ten times the calculated capacitance and 30–50 percent lower than the calculated ESR. This design used a 220-μF OS-Con capacitor in parallel with a ceramic to reduce ESR.

2.3.3 Power Switch

Based on the preliminary estimate, $r_{DS(ON)}$ should be less than 0.10 V ÷ 2.5 A = 40 mΩ. The IRF7406 is a 30-V p-channel MOSFET with $r_{DS(ON)}$ = 40 mΩ. Power dissipation (conduction + switching losses) can be estimated as:

$$P_D = \left(I_O^2 \times r_{DS(ON)} \times D\right) + \left(0.5 \times V_i \times I_O \times t_{r+f} \times f\right)$$

Assuming total switching time, t_{r+f}, = 100 ns, a 55°C maximum ambient temperature, and $r_{DS(ON)}$ adjustment factor (for high temperature) = 1.6, then:

$$P_D = \left[2.5^2 \times (0.04 \times 1.6) \times 0.7\right] + \left[0.5 \times 5.5 \times 2.5 \times \left(0.1 \times 10^{-6}\right) \times \left(275 \times 10^3\right)\right] = 0.41 \text{ W}$$

The thermal impedance $R_{\theta JA}$ = 90°C/W for FR-4 with 2-oz. copper and a one-inch-square pattern, thus:

$$T_J = T_A + \left(R_{\theta JA} \times P_D\right) = 55 + (90 \times 0.41) = 92°C$$

2.3.4 Rectifier

The catch rectifier conducts during the time interval when the MOSFET is off. The 30WQ04 is a 3.3-A, 40-V rectifier in a D-Pak power surface-mount package. The power dissipation is:

$$P_D = I_O \times V_D\left(1 - D_{Min}\right) = 2.5 \times 0.6 \times 0.68 = 1.02 \text{ W}$$

2.3.5 Snubber Network

A snubber network is usually needed to suppress the ringing at the node where the power switch drain, output inductor, and the rectifier connect. This is usually a trial-and-error sequence of steps to optimize the network; but as a starting point, select a snubber capacitor with a value that is 4–10 times larger than the estimated capacitance of the catch rectifier. The 30WQ04 has a capacitance of 110 pF, resulting in a snubber capacitor of 1000 pF. Then, measuring a ringing time constant of 20 ns, R is:

$$R = \frac{20 \times 10^{-9}}{C} = \frac{20 \times 10^{-9}}{1000 \times 10^{-12}} = 20\ \Omega$$

A 22-Ω resistor is used in the design.

2.3.6 Controller Functions

The controller functions, oscillator frequency, soft-start, dead-time control, short-circuit protection, and sense-divider network are discussed in this section.

The oscillator frequency is set by selecting the resistance value from the graph in Figure 6 of the TL5001 data sheet. For 275 kHz, a value of 30.1 kΩ is selected.

Dead-time control provides a minimum off-time for the power switch in each cycle. Set this time by connecting a resistor between DTC and GND. For this design, a maximum duty cycle of 100% is chosen. Then *R* is calculated as:

$$R = \left(R_{OSC} + 1.25\ \text{k}\Omega\right)\left[D(V_{0(100\%)} - V_{0(0\%)}) + V_{0(0\%)}\right] = (30.1\ \text{k}\Omega + 1.25\ \text{k}\Omega)[1(1.4 - 0.6) + 0.60] = 44\ \text{k}\Omega \Rightarrow 47\ \text{k}\Omega$$

Soft-start is added to reduce power-up transients. This is implemented by adding a capacitor across the dead-time resistor. In this design, a soft-start time of 5 ms is used:

$$C = \frac{t_R}{R_{DT}} = \frac{0.005\ s}{47\ k\Omega} = 0.1\ \mu F$$

The TL5001 has short circuit protection (SCP) instead of a current sense circuit. If not used, the SCP terminal must be connected to ground to allow the converter to start up. If a timing capacitor is connected to SCP, it should have a time constant that is greater than the soft-start time constant. This time constant is chosen to be 75 ms:

$$C(\mu F) = 12.46 \times t_{SCP} = 12.46 \times 0.075\ s = 0.93\ \mu F$$

2.3.7 Loop Compensation

Loop compensation is necessary to stabilize the converter over the full range of load, line, and gain conditions. A buck-mode converter has a two-pole LC output filter with a 40-dB-per-decade rolloff. The total closed-loop response needed for stability is a 20-dB-per-decade rolloff with a minimum phase margin of 30 degrees over the full bandwidth for all conditions. In addition, sufficient bandwidth must be designed into the circuit to assure that the converter has good transient response. Both of these requirements are met by adding compensation components around the error amplifier to modify the total loop response.

The first step in design of the loop compensation network is the design of the output sense divider. This sets the output voltage and the top resistor determines the relative size of the rest of the compensation design. Since the TL5001 input bias current is 0.5 μA (worst case), the divider current should be at least 0.5 mA. Using a 1-kΩ resistor for the bottom of the divider gives a divider current of 1 mA. Since this is a dual-voltage output, the divider must be selectable. For a 5-V output, the divider was set for 1 kΩ and 4 kΩ. The bottom of the divider is calculated for the 3-V mode as:

$$R = \frac{R_T}{V_O - V_{REF}} = \frac{4\ k\Omega}{3.3 - 1} = 1.74\ k\Omega$$

The pulse-width modulator gain can be approximated as the change in output voltage divided by the change in PWM input voltage:

$$A_{PWM} = \frac{\Delta V_O}{\Delta V_{COMP}} = \frac{9–0}{1.4–0.6} = 11.25 \Rightarrow 21\ dB$$

The LC filter has a double pole at:

$$\frac{1}{2\pi\sqrt{LC}} = 1.87\ kHz$$

and rolls off at 40-dB per decade after that until the ESR zero is reached at:

$$\frac{1}{2\pi R_{ESR} C} = \frac{1}{2\pi(0.027)\left(220 \times 10^{-6}\right)} = 26.8\ kHz$$

This information is enough to calculate the required compensation values. Figure 2–1 shows the power stage gain and phase plots.

Figure 2–1. Power Stage Response

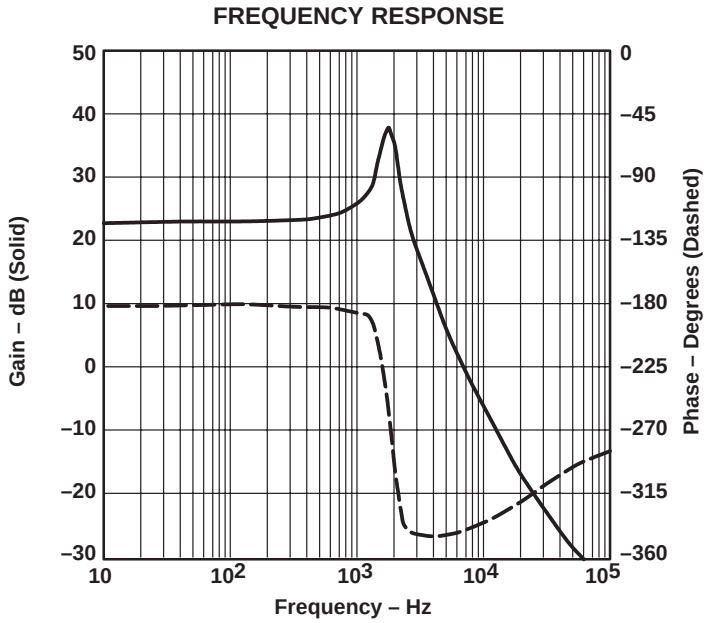
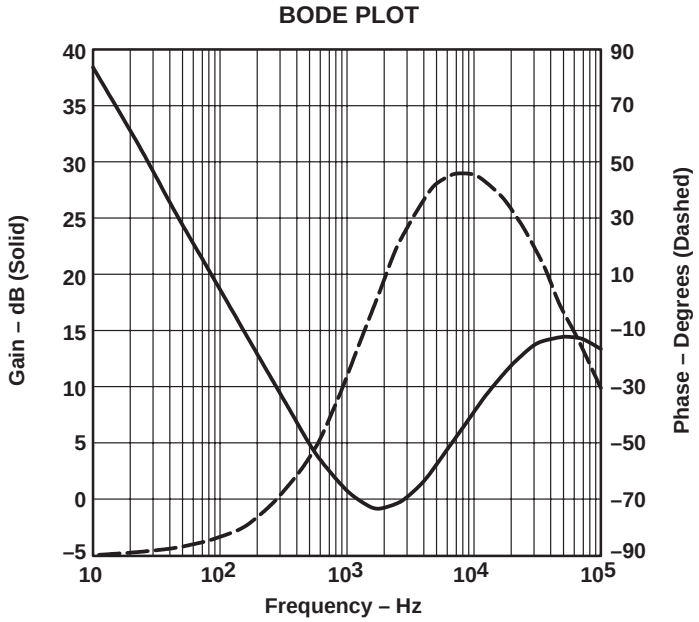


Figure 2–2 shows the required error amplifier compensation response.

Figure 2–2. Required Compensation Response



This response can be met with the following:

- ❑ A pole at zero to give high dc gain
- ❑ Two zeroes at 1.87 kHz to cancel the LC poles
- ❑ A pole at 26.8 kHz to cancel the ESR zero
- ❑ A final pole to roll off high-frequency gain above 100 kHz

The sum of the gains of the modulator, the LC filter, and the error amplifier needs to be 0 dB at the selected unity-gain frequency of 20 kHz. The modulator and LC filter gain is –14 dB. The two zeroes at 1.87 kHz in the compensation network that cancels the LC poles will have a total gain of 41.2 dB at 20 kHz. Therefore, the pole at zero frequency needs to furnish 0–(–14+41.2) = –27.2 dB (voltage gain = 0.04365) at 20 kHz. R5 and C12 provide this pole. R6 is already chosen as 4 kΩ. Calculate C12 as:

$$C12 + C11 = \frac{1}{(2\pi)(f)(R6)(\text{Required Gain})}$$

In practice C12 is much greater than *C*11, therefore:

$$C12 = \frac{1}{(2\pi)(20\ \text{kHz})(4\ \text{k}\Omega)(0.04365)} = 0.045\ \mu\text{F} \quad \text{Use C12} = 0.047\ \mu\text{F}$$

R4 provides the first zero at the LC break point:

$$R4 = \frac{1}{(2\pi)(1.87\ \text{kHz})(C12)} = 1.89\ \text{k}\Omega \qquad \text{Use R4} = 1.8\ \text{k}\Omega$$

C13 provides the other zero at the LC break point:

$$C13 = \frac{\frac{1}{(1.87\ \text{kHz})} - \frac{1}{(20\ \text{kHz})}}{2\pi(R6)} = 0.019\ \mu\text{F} \qquad \text{Use C13} = 0.018\ \mu\text{F}$$

R5 provides the compensation for the ESR zero:

$$R5 = \frac{1}{(2\pi)(26.8\ \text{kHz})(C13)} = 330\ \Omega$$

Finally, C11 provides a rolloff filter at high frequency, chosen at 100 kHz:

$$C11 = \frac{1}{(2\pi)(100\ \text{kHz})(R4)} = 0.00088\ \mu\text{F} \qquad \text{Use C11} = 1000\ \text{pF}$$