TEXAS INSTRUMENTS

Thermal Considerations for RF Power Amplifier Devices

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ABSTRACT

The fundamentals of printed circuit board (PCB) layout, thermal heatsink definition, and die temperature calculations are examined. PCB layout approaches that enhance heat transfer are also discussed, along with the influence of typical air interface standards and practical application of theory. Examples are included that apply these first-order methods to the calculation of permissible power levels for wireless power amplifiers based on commercially available Texas Instruments (TI™) power amplifier products.

1 Introduction

This application report outlines thermal considerations when designing RF power amplifiers using surface mount devices. Section 2 provides general board layout and device mounting schemes. Section 3 gives an overview of basic heat transfer analysis and describes its application. Section 4 demonstrates approximate methods for the calculation of permissible dissipated powers for systems based on the TRF8010 radio frequency (RF) transmit driver, the TRF7003 RF power amplifier, and the TRF7610 global systems for mobile communications (GSM) RF power amplifier, all from Texas Instruments Incorporated.

2 PCB Layout and Mounting Scheme

In a packaged device, the semiconductor die is usually attached to a package mounting surface by means of epoxy or solder die attach materials, as shown in Figure 1. The figure illustrates a typical assembly and mounting scheme for a surface-mount radio frequency (RF) power amplifier device.

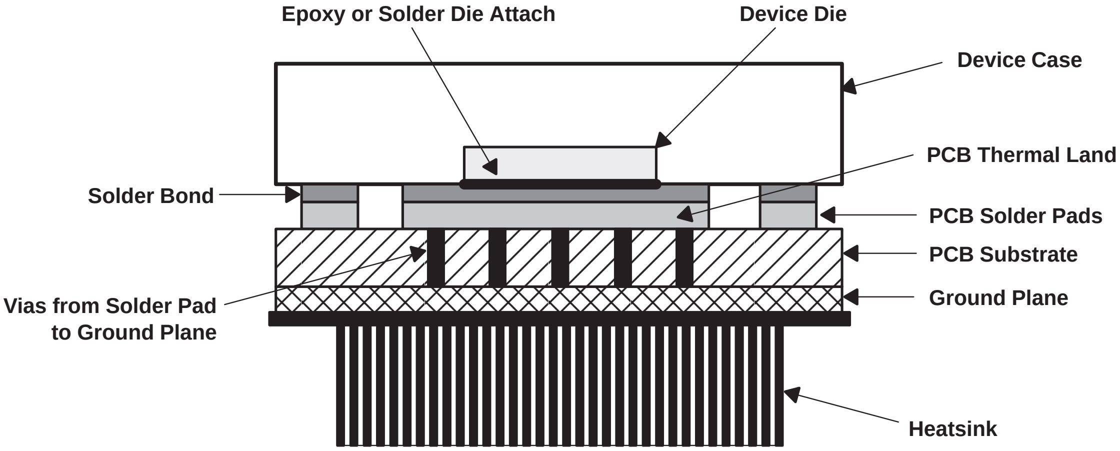
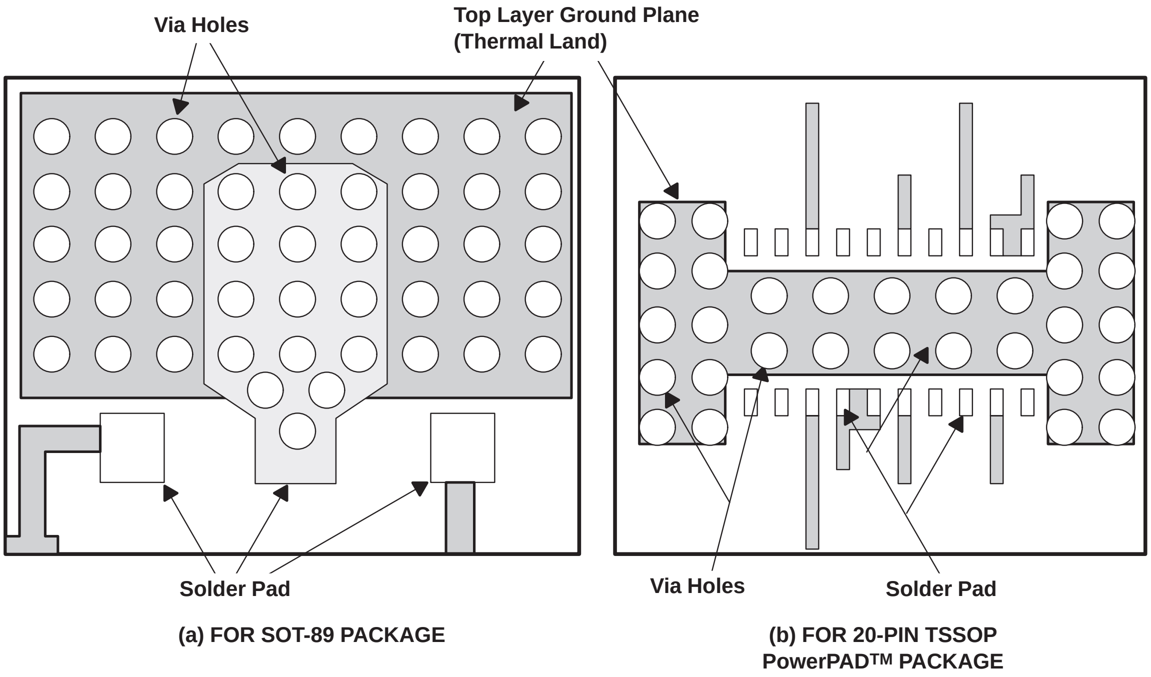


Figure 1. Typical Cross-Sectional View of a Surface-Mount Power Device and Thermal Transfer System

PCB solder pads provide a thermal path between the packaged semiconductor and the PCB. Vias from the front side to back side of the PCB conduct heat away from the semiconductor device case to an internal or backside ground plane and then to a heatsink, if necessary. In an RF design, the thermal paths must also provide good RF performance. Solder pad layouts, or thermal lands, for SOT-89 and 20-pin TSSOP PowerPAD™ packages are shown in Figure 2.

PowerPAD is a trademark of Texas Instruments Incorporated.



(a) FOR SOT-89 PACKAGE

(b) FOR 20-PIN TSSOP PowerPAD™ PACKAGE

Figure 2. Typical Circuit Layout – Top View

Computer simulation indicates that there is a point beyond which additional vias do not significantly improve thermal transfer through the PCB. Ideally, the thermal vias should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent solder from wicking away from the interface between the package body and the thermal land during solder reflow. If the vias are not plugged, a solder mask material must be used to cap the vias.

PCB layout and thermal design for TI’s PowerPAD™ package is contained in the Texas Instruments technical brief SLMA002, “PowerPAD™ Thermally Enhanced Package”. This brief describes PCB design considerations in detail, including correct design and use of thermal lands and vias, as well as information on assembly and rework techniques.

3 Basic Thermal Analysis

The effectiveness of a design to remove heat from the semiconductor junction and its package is guaged by parameters known as thermal conductivity and thermal resistance (thermal resistance =1/thermal conductivity x thickness/ area). These parameters are somewhat analogous to electrical conductivity and resistance because heat (like current and charge) can be transferred at different rates depending upon the geometry and the material properties of a junction.

For clarity, it helps to liken the flow of heat through a device and its surroundings to the flow of current through a circuit. In the manner that electrical relationships in a circuit are defined by Ohm’s law, thermal relationships can be defined by a current source representing the dissipated power and a network of thermal resistances.

Referring to the device assembly drawing and heatsink system illustrated in Figure 1, the steady-state flow of thermal energy can be modeled by the equivalent electrical analog circuit shown in Figure 3.

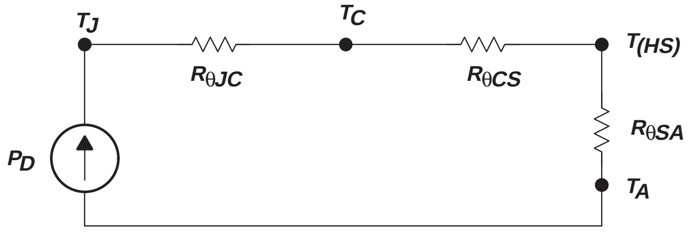


Figure 3. The Equivalent Steady-State Thermal Energy Flow Model of the Heat Flow in Figure 1

where:

$R_{\theta JC}$: thermal resistance junction-to-case, [°C/W]

$R_{\theta CS}$: thermal resistance case-to-heatsink, [°C/W]

$R_{\theta SA}$: thermal resistance heatsink-to-ambient, [°C/W]

T_J: junction temperature, [°C]

T_C: case temperature, [°C]

$T_{(HS)}$: heatsink temperature, [°C]

T_A: ambient temperature, [°C]

P_D: power dissipation, [W].

Under steady-state conditions, thermal energy is transferred between two objects at a rate shown in equation (1).

$$P_D = (KA/L) \times \Delta T = (KA/L) \times (T_1 - T_2),\ [W] \tag{1}$$

where:

K: thermal conductivity coefficient, [W°C/cm]
A: cross-sectional area perpendicular to heat flux vector, [cm^2]
L: length of thermal path, [cm]
T_1: temperature of heat source, [°C]
T_2: temperature of contact material, [°C]

Equation (1) can be rewritten as:

$$P_D = \left(T_1 - T_2\right) \div \left(L/KA\right) = -\left(1/R_\theta\right) \times \left(T_2 - T_1\right),\ [W] \tag{2}$$

where:

$$R_\theta = L/KA,\ \left[{}^\circ C/W\right] \tag{3}$$

is the thermal resistance between the objects.

The thermal conductivity coefficient, *K*, is different from one material to another and also varies with temperature, position/geometry, fabrication/processing, and other environmental factors.

With the basic thermal transfer equations defined, their applicability to integrated circuit (IC) thermal considerations can be described.

The total internal dissipated power of the device while operating is:

$$P_{D(actual,\ oper.)} = P_{(DC)} + P_{(RFIN)} - P_{(RFOUT)},\ [W] \tag{4}$$

where:

$P_{(DC)}$: DC power into the device, [W]
$P_{(RFIN)}$: RF power into the device, [W]
$P_{(RFOUT)}$: RF power delivered to the load, [W].

In practice, case scenarios for power dissipation must be considered. The worst case scenario assumes the drain voltage of the device is significantly higher than the typical operating point, which is usually the case during battery charging. Additional RF power can also be introduced into the device by reflections from an antenna that is not fully extended. However, for first-order approximations, the use of equation (4) is sufficient.

From the thermal properties, the maximum case temperature is given by:

$$T_{C(max)} = T_{J(max)} - R_{\theta JC}P_D,\ [{}^\circ C\,] \tag{5}$$

where:

$T_{J(max)}$: maximum junction temperature, [°C]
$R_{\theta CS}$: case-to-heatsink thermal resistance, [°C/W].

The same relationship is applied to the heatsink temperature. Therefore, the maximum heatsink temperature is given by:

$$T_{(HS)\,(max)} = T_{C(max)} - R_{\theta CS}P_D,\ [{}^\circ C] \tag{6}$$

where:

$T_{C(max)}$: maximum case temperature, [°C]
$R_{\theta CS}$: case-to-heatsink thermal resistance, [°C/W].

The heatsink-to-ambient thermal resistance is calculated using:

$$R_{\theta SA} = \left(T_S - T_A\right)/P_D,\ \left[{}^\circ C/W\right]. \tag{7}$$

Referring to the model shown in Figure 3, the junction-to-ambient thermal resistance is:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA},\ [°C/W]. \tag{8}$$

where:

$$R_{\theta CA} = R_{\theta CS} + R_{\theta SA},\ [°C/W] \tag{9}$$

is the thermal resistance case-to-ambient.

Thus,

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA},\ [°C/W]. \tag{10}$$

The total power that can be dissipated by the system in Figure 3 is:

$$P_D = -\left(1/R_{\theta JA}\right) \times \left(T_A - T_J\right),\ [W]. \tag{11}$$

Using equation (10), equation (11), and the model in Figure 3, the amount of power that can be dissipated, P_D, is maximum if $R_{\theta CS}$ and $R_{\theta SA}$ are minimum at a given temperature; this assumes that $R_{\theta JC}$ is fixed. Figure 4 illustrates both the permissible region of dissipated power when $R_{\theta CS}$ and $R_{\theta SA}$ are negligible – the so-called infinite heatsink condition – and the region where the case-to-ambient thermal resistance is not negligible.

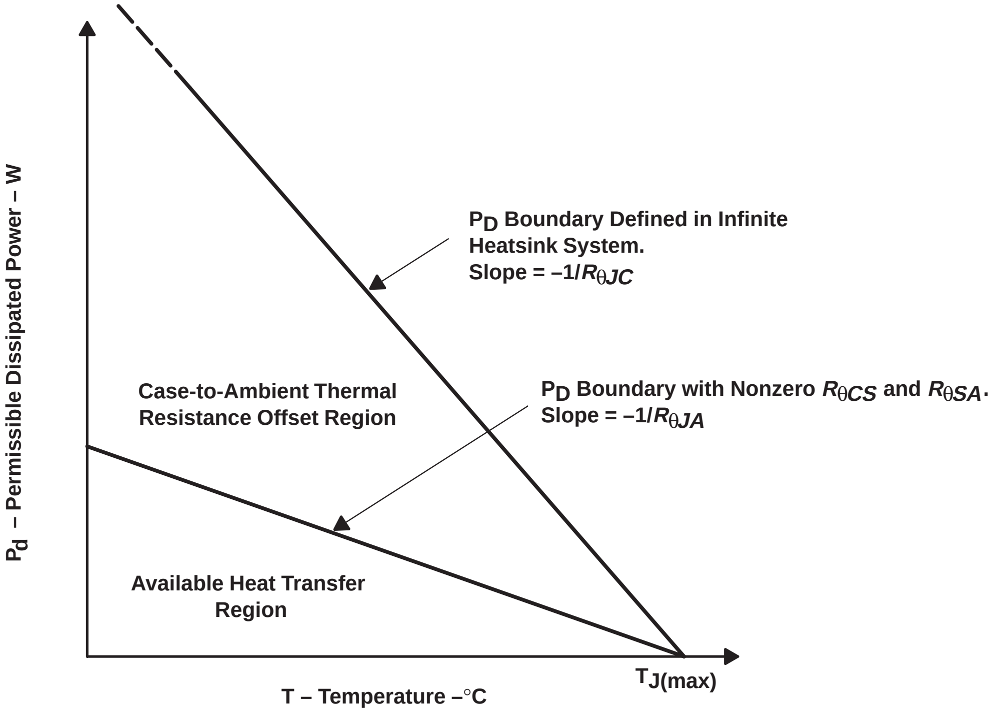


Figure 4. The Permissible Regions of Dissipated Power

Figure 4 shows the offset region due to $R_{\theta CA}$. The offset region due to $R_{\theta CA}$ is the difference between the maximum permissible dissipated power under the infinite heatsink condition and the dissipated power with a nonzero $R_{\theta CA}$. If $R_{\theta CA}$ tends toward zero, the line with slope $-1/R_{\theta JA}$ tends toward the ideal line with slope $-1/R_{\theta JC}$ thus increasing the permissible dissipated power of the system.

In reality, $R_{\theta JC}$ is not a constant. However, for this application, it is acceptable to approximate $R_{\theta JC}$ as a constant.

In considering the junction-to-ambient thermal resistance, $R_{\theta JA}$, described in equation (10), the junction-to-case thermal resistance, $R_{\theta JC}$, is defined by the manufacturer. The end user has no influence on this value. The case-to-heatsink thermal resistance, $R_{\theta CS}$, however, depends upon the mounting scheme and board design. As mentioned earlier, using a sufficient number of vias and using materials with good thermal conductivity can reduce the case-to-heatsink thermal resistance, $R_{\theta CS}$. The choice of heatsinking system with a low heatsink-to-ambient thermal resistance, $R_{\theta SA}$, will also improve the transfer of heat and reduce $R_{\theta JA}$. Thus, the case-to-ambient thermal resistance, $R_{\theta CA} = R_{\theta CS} + R_{\theta SA}$, is determined by the end user. A thermal management system with a low case-to-ambient thermal resistance increases the transfer of heat from the junction of the device by reducing the overall junction-to-ambient thermal resistance.

Along with the maximum ratings of junction temperature and the junction-to-case thermal resistance, other information that may be provided with a device includes a power derating curve as illustrated in Figure 5. This power derating curve indicates the maximum permissible dissipated power of the device as a function of the case temperature. P_D decreases with a slope of $-1/R_{\theta JC}$, where $R_{\theta JC}$ is described in equation (5).

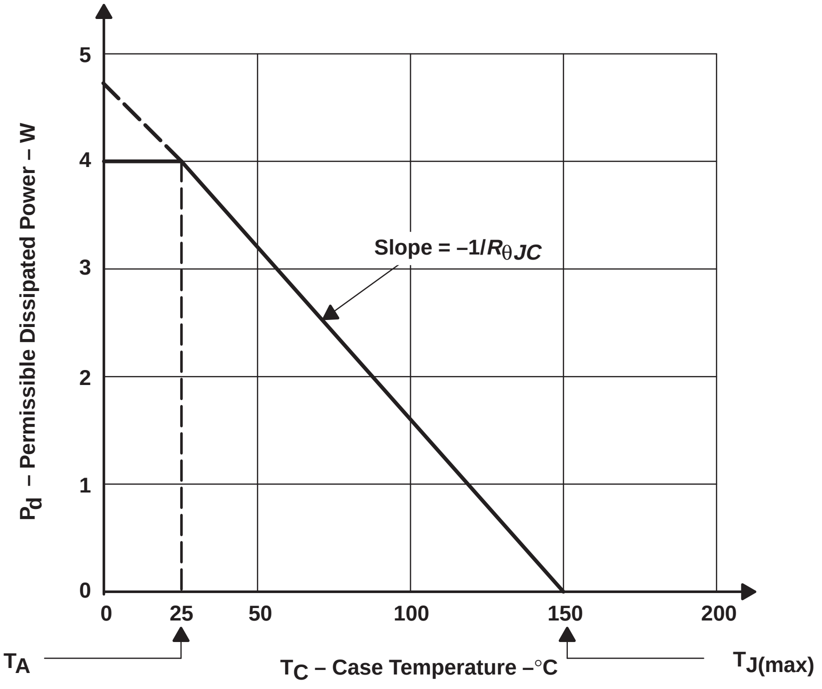


Figure 5. Typical Power Derating Curve

The line defined by ($-1/R_{\theta JC}$) in Figure 5 is the best case infinite heatsink condition. The end user must accurately design and model the system in use to determine $R_{\theta CS}$ and $R_{\theta SA}$ to minimize $R_{\theta JA}$.

3.1 Pulsed Operation Considerations

In the previous sections, the steady-state flow of thermal energy for a RF power amplifier that operates in continuous wave (CW) was considered. Equally important are the thermal characteristics of power amplifiers that operate under pulsed conditions. A factor in these thermal characteristics is the specific heat capacity of the device and the thermal management system. As the DC thermal resistance is analogous to a resistor in the electrical circuit, the specific heat capacity is analogous to a capacitor. Whereas a capacitor stores electrical energy, a material's ability to store energy in the form of heat is expressed as specific heat capacity. The thermal time constant of a material defines how fast a material heats up or cools down, and is analogous to the RC time constant of an electrical circuit.

Any material in a device or PCB assembly can be thermally modeled by its thermal resistance in parallel with a capacitor representing the material's specific heat capacity, as shown in Figure 6.

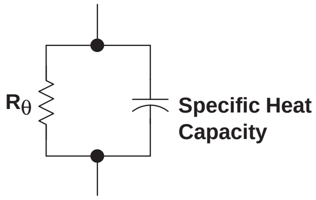


Figure 6. Thermal Impedance in Parallel With Specific Heat Capacity

The parallel combination of the thermal resistance and specific heat capacity is known as the thermal impedance. When the RF power amplifier operates under pulsed conditions, this phenomenon manifests itself as illustrated in Figure 7.

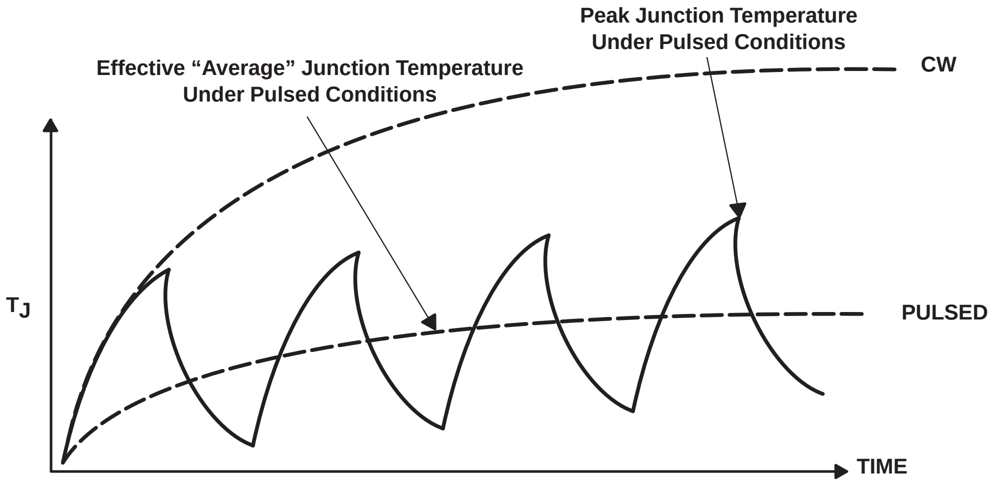


Figure 7. Typical Junction Temperature vs. Time in a Pulsed Application as Compared to a CW Application

As the power amplifier is pulsed, the peak junction temperature, T_J, increases and then decreases along with the pulse. The effect of the specific heat capacity is the slow rise of the average T_J over many pulses. Overall, operating an RF power amplifier under pulsed conditions can effectively reduce its junction temperature as compared to operating under CW conditions.

Thus, in pulsed operation, the concept of DC thermal resistance is replaced by the concept of thermal impedance. Manufacturers can produce a graph, specific to a device, which provides the user with transient thermal impedance curves, normalized with respect to the DC thermal resistance, versus pulse duration. Knowing the pulse duration and the duty cycle, a normalization factor, ρ, which relates the thermal impedance to the DC thermal resistance, can be obtained. The temperature rise can then be calculated using only the DC thermal resistance, R_θ , as:

Temperature rise = $P_D \times \rho \times R_\theta$

During pulsed operation, the actual operating dissipated power is a function of duty cycle. The actual operating dissipated power is reduced with a decrease in the duty cycle. The average power dissipation, $P_{(AV)}$, is approximately equal to the peak dissipated power multiplied by the duty cycle:

$P_{(AV)} = P_D \times$ duty cycle

The applicable relationship for P_D [equation (11)] can be solved for the required case-to-ambient thermal resistance for a thermal design, given the device operating conditions and the junction-to-case thermal resistance. The resulting equation is useful for first-order approximations of thermal management:

$$P_{D(actual,\ oper.)} \times Duty\ Cycle \le \left(T_{J(max,\ oper.)} - T_{A(max)}\right) \div R_{\theta JA},\ \ [\mathrm{W}] \qquad (12)$$

where:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$, [°C/W].

$T_{J(max,\ oper.)}$ is the maximum junction temperature under operating conditions, is less than or equal to $T_{J(max)}$, and may be specified based on reliability data and/or design analysis.

With $P_{D(actual,\ oper.)}$, $T_{J(max,\ oper.)}$, $T_{A(max)}$, and $R_{\theta JC}$ given and the duty cycle specified by the application, equation (12) can be solved for the first-order approximation of the required case-to-ambient thermal resistance for a given system as:

$$R_{\theta CA} \le \left[\left(T_{J(max,\ oper.)} - T_{A(max)}\right) \div \left(P_{D(actual,\ oper.)} \times Duty\ Cycle\right)\right] - R_{\theta JC},\ [^\circ C/W] \qquad (13)$$

For CW operation, the duty cycle is equal to one. Under pulsed conditions, the duty cycle is always less than one.

4 Numerical Examples

To clarify the preceding discussion, the following numerical examples are based on the TRF8010 RF Transmit Driver, the TRF7003 power amplifier, and the TRF7610 GSM RF Power Amplifier from Texas Instruments Incorporated.

4.1 TRF8010 RF Transmit Driver

The TRF8010 is an RF transmit driver housed in a 20-pin TSSOP PowerPAD™ package. This package uses an integrated backside thermal pad for optimum heat transfer from the device die to the thermal management system. The following information is extracted from the product data sheet:

4.1.1 Absolute maximum ratings over operating free-air temperature range

Maximum operating junction temperature, T_J . . . . 110°C

Maximum junction temperature, $T_{J(max)}$ . . . . 150°C

$R_{\theta JA}$ thermal resistance, junction-to-ambient with the device thermal pad soldered down to 1-oz. Cu ground plane on FR4 PCB with zero air flow . . . . 32°C/W

$R_{\theta JC}$ thermal resistance, junction-to-case, assuming an infinite heatsink and zero air flow . . . . 3.5°C/W

4.1.2 Recommended operating conditions

Operating free-air temperature range, T_A . . . . –40°C to 85°C

4.2 TRF8010 Thermal Calculations

From equation (11), the maximum permissible dissipated power in the infinite heatsink system is defined as:

$$P_{D(max)} = -\left(1/R_{\theta JC}\right) \times \left(T_C - T_{J(max)}\right), \ [W]. \tag{14}$$

At a case temperature of 0°C, the permissible dissipated power is:

$$P_{D(max)\ T_C = 0^0} = -(1/3.5) \times (0–150) = 42.8 \ W. \tag{15}$$

At a case temperature of 25°C in the same system, the permissible dissipated power is:

$$P_{D(max)\ T_C = 25^0} = -(1/3.5) \times (25–150) = 35.7 \ W. \tag{1}$$

When the package thermal pad is soldered to the ground plane of an FR4 PCB, the permissible dissipated power is:

$$P_{D(max)} = -\left(1/R_{\theta JA}\right) \times \left(T_A - T_{J(max)}\right), \ [W]$$

and at an ambient temperature of 0°C is:

$$P_{D(max)\ T_A = 0^0} = -(1/32) \times (0–150) = 4.7 \ W.$$

At an ambient temperature of 25°C, the permissible dissipated power is:

$$P_{D(max)\ T_A = 25^0} = -\left(1/32\right) \times (25–150) = 3.9\ W. \tag{2}$$

Results (1) and (2) are known as the absolute maximum ratings of continuous total power dissipation at T_C of 25°C and T_A of 25°C, respectively. Figure 8 shows both results.

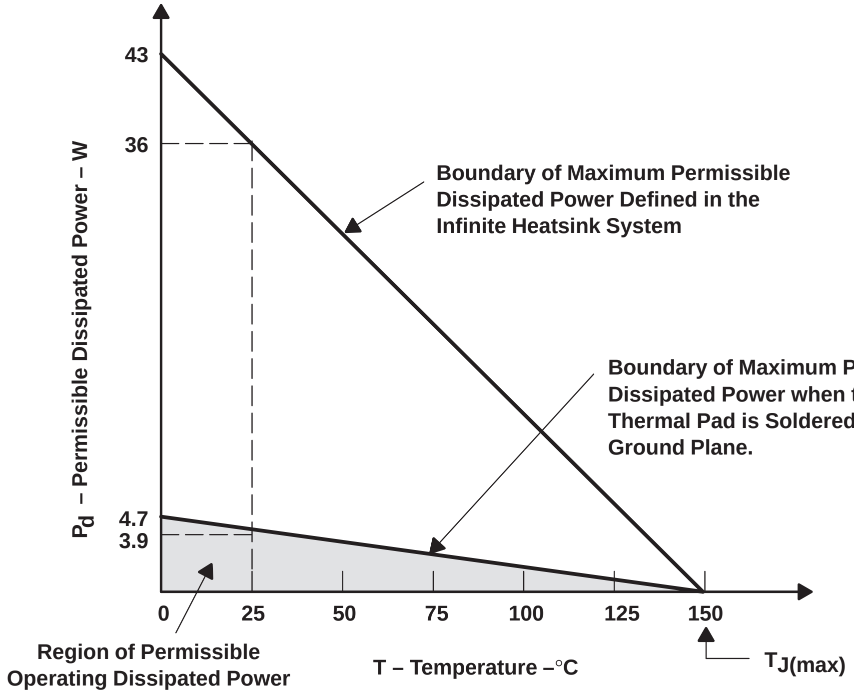


Figure 8. Absolute Maximum Ratings of Continuous Total Power Dissipation for TRF8010

Equation (11) can be rewritten to calculate the maximum operational dissipated power of the device under the maximum recommended operating conditions, $T_{A(max,\ oper.)} = 85°C$ and $T_{J(max,\ oper.)} = 110°C$, as:

$$P_{D,(max,\ oper.)} = -\left(1/R_{\theta JA}\right) \times \left(T_{A(max,\ oper.)} - T_{J(max,\ oper.)}\right),\ [W]. \tag{16}$$

The maximum operational dissipated power of the device is:

$$P_{D(max,\ oper.)} = -\left(1/32\right) \times (85–110) = 0.78\ W.$$

As an experiment, a test circuit of the TRF8010 was built on an FR4 type PCB with a 1-oz copper ground plane, and a PCB layout similar to that shown in Figure 2b. The laboratory data, under CW operation, was:

Vcc = 4.8 V; Ic = 0.17 A; VPC = 3 V

$P_{(RFIN)}$ = 0 dBm or 0.001 W

$P_{(RFOUT)}$ = 22 dBm or 0.158 W

Applying equation (4), the actual operational power dissipated by the device is found as follows:

$$
\begin{aligned}
P_{D(actual,\ oper.)} &= P_{(DC)} + P_{(RFIN)} - P_{(RFOUT)}\ ,\ [W] \\
&= (4.8\ \times 0.17)\ +\ 0.001\ -\ 0.158 \qquad (17) \\
P_{D(actual,\ oper.)} &\cong 0.66\ W
\end{aligned}
$$

which is less than the maximum permissible operating dissipated power of 0.78 Watts. Therefore, it is safe to operate the device in a CW system at an ambient temperature of 85°C.

Figure 9 shows the permissible operating dissipated power region and the tested dissipated line. The junction-to-ambient thermal resistance can be reduced, thus increasing the maximum operating dissipated power, if a different heatsink system is used. With $R_{\theta JC}$ fixed, $R_{\theta JA}$ can be reduced by reducing $R_{\theta CA}$. By reducing $R_{\theta CA}$, the permissible dissipated power region would be larger and, therefore, the device could be operated with higher dissipated power. Figure 9 illustrates this point.

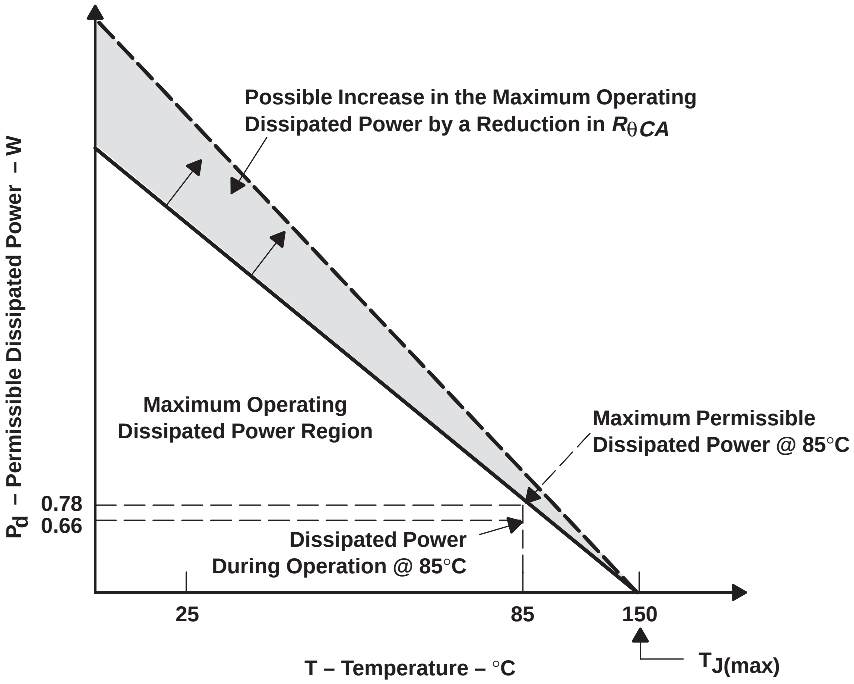


Figure 9. Permissible Operating Dissipated Power Region of TRF8010

As with the TRF8010 device, thermal considerations for the TRF7003 and TRF7610 Power Amplifiers were investigated. The TRF7003 is housed in a SOT-89 (PK) package, while the TRF7610 is housed in a 24-pin TSSOP PowerPAD™ package. The results are presented next for reference.

4.3 TRF7003 Silicon RF Power Amplifier

4.3.1 *Absolute maximum ratings over operating free-air temperature range*

Maximum junction temperature, $T_{J(max)}$	150°C
$R_{\theta JC}$ thermal resistance, junction-to-case, assuming an infinite heatsink and zero air flow	10°C/W
Total device power dissipation @ T_C = 25°C	12.5 W
Derate above 25°C	100 mW/°C

4.3.2 *Recommended operating conditions*

Operating free-air temperature range, T_A	–40 to 85°C
Maximum drain current, I_D	2 A

4.4 TRF7003 Thermal Calculations

Using equation (11), the maximum permissible power dissipated by the system at an ambient temperature of 25°C, assuming an infinite heatsink and zero air flow system, can be calculated as

$$\begin{aligned} P_{D(max)} &= -\left(1/R_{\theta JC}\right) \times \left(T_A - T_{J(max)}\right),\ [W] \\ &= -(1/10)\ \times\ (25–150) \\ P_{D(max)} &= 12.5\ W. \end{aligned} \tag{18}$$

With $R_{\theta JC}$ = 10°C/W, the derating curve shown in Figure 10 can be constructed.

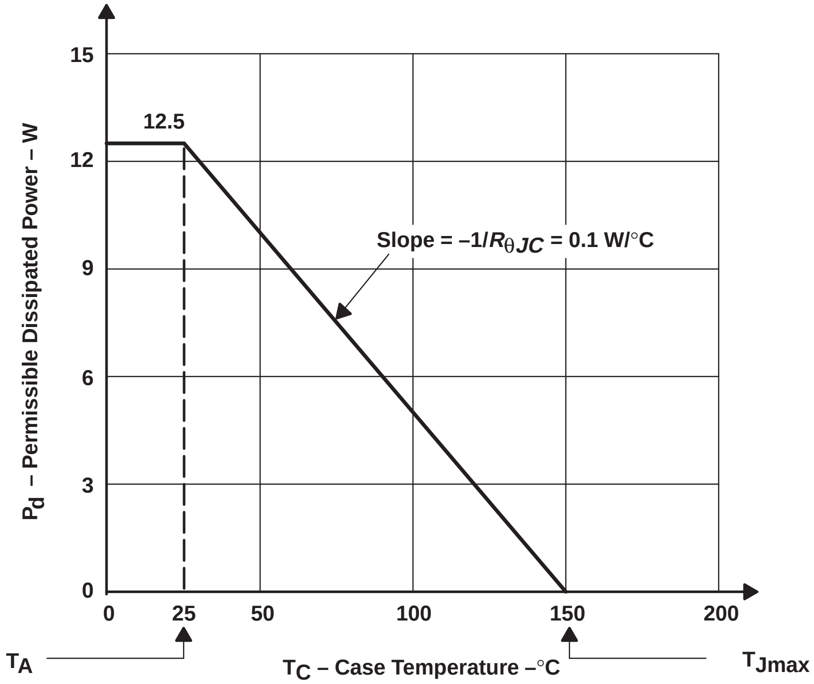


Figure 10. TRF7003 Derating Curve

When $T_C = T_{J(max)}$, the power that can be dissipated, P_D, is zero.

Based upon laboratory results and equation (4), the actual operating power dissipated by the device when operated in a CW mode with 4.8-V drain bias applied is:

$$\begin{aligned} P_{D(actual,\ oper.)} &= P_{(DC)} + P_{(RFIN)} - P_{(RFOUT)}\ ,\ [W] \\ &= (0.71 \times 4.8) + 0.2 - 1.8 \\ P_{D(actual,\ oper.)} &\cong 1.8\ W. \end{aligned} \tag{19}$$

To maintain a junction temperature less than 150°C at 85°C ambient temperature, the required thermal case-to-ambient thermal resistance, using equation (13) with duty cycle equal to 1 is:

$$\begin{aligned} R_{\theta CA} &\leq [(150 - 85) \div (1.8 \times 1)] - 10\ [^{\circ}C/W] \\ R_{\theta CA} &\leq 26\ [^{\circ}C/W]. \end{aligned} \tag{20}$$

A check of this calculation using $T_C = T_J - (P_D \times R_{\theta JC})$ (21)

with $T_J = 150^{\circ}C,\ P_D = 1.8\ W$ and $R_{\theta JC} = 10\ [^{\circ}C/W]$

gives T_c = 132°C.

Using $T_A = T_C - (P_D \times R_{\theta JA})$ (22)

with $T_C = 132^{\circ}C,\ P_D = 1.8\ W$ and $R_{\theta JA} = 26\ [^{\circ}C/W]$

gives $T_A = 132 - (1.8 \text{ x } 26) \cong 85^{\circ}C$.

Thus, a case-to-ambient thermal resistance of less than 26°C/W is sufficient to maintain the device junction temperatue less than 150°C.

4.5 TRF7610 GSM RF Power Amplifier

4.5.1 Absolute maximum ratings over operating free-air temperature range

Maximum operating junction temperature, T_J . . . . 110°C

Maximum junction temperature, $T_{J(max)}$ . . . . 150°C

$R_{\theta JC}$ thermal resistance, junction-to-case, assuming an infinite heatsink and zero air flow . . . . 3.5°C/W

4.5.2 Recommended operating conditions

Supply current . . . . 2-A TYP

Operating free-air temperature range, T_A . . . . –40 to 85°C

4.6 TRF7610 Thermal Calculations

The Texas Instruments TRF7610 is designed for use in a 900-MHz GSM system. The GSM air interface employs the TDMA/FDMA access method, and the transmit frequency band is 880 to 915 MHz. This transmit frequency band is broken up into 124 channels with eight users per channel and a channel spacing of 200 kHz.

The frame period is 4.6152 ms (216.675 Hz), while the timeslot period is 576.9 μs. The TDMA burst (each eight timeslots) is comprised of a 28-μs ramp up, a 542.8-μs data burst, and a 28-μs ramp down. The 28-μs ramp up and ramp down include portions of other users’ timeslots. Eight timeslots make up one frame.

A typical power amplifier burst of 543- to 560-µs in a GSM application is usually assumed, but the actual duration depends on the system implementation. For this example, a 560 µs burst that repeats at a 216.675-Hz rate is assumed. The corresponding duty cycle is about 13 percent.

When the amplifier is operating with a DC bias of 4.8 V and 1.9 A, an input power of 3.16 mW, and an output power of 35.7 dBm, the dissipated power is:

$$P_D = P_{(DC)} + P_{(RFIN)} - P_{(RFOUT)} = (4.8 \times 1.9) + 0.00316 - 3.7 \tag{23}$$

$$P_D \cong 5.4\ W$$

The pulsed operating conditions for the TRF7610 were modeled in the TSSOP PowerPAD™ package and the results are shown in Figure 11, including the temperature rise resulting from simulated CW operation, and the peak and average temperature rise resulting from simulated operation under pulsed conditions.

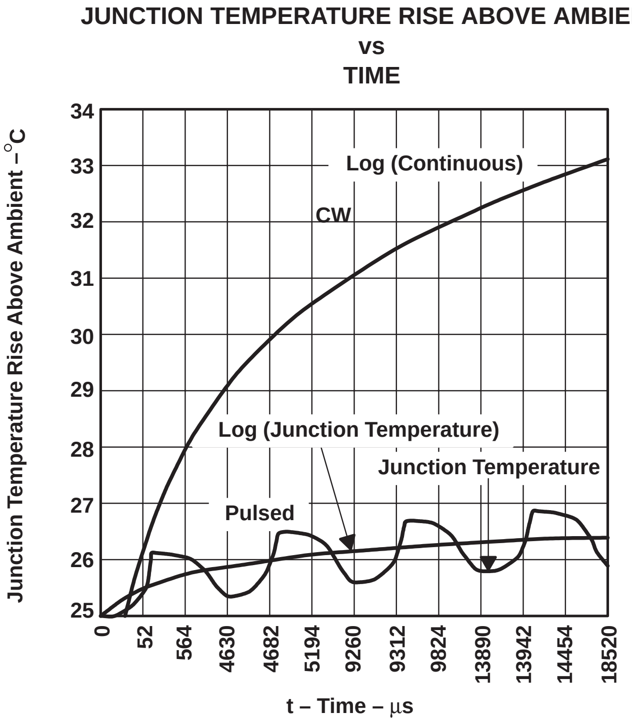


Figure 11. **Simulated Junction Temperature Rise vs. Time for the TRF7610 in a 24-Pin TSSOP PowerPAD™ Package**

Most important is the relative relationship between the simulated CW operation and simulated pulsed operation. The ratio of the corresponding temperature rises is approximately 0.13, which closely approximates the duty cycle of the TRF7610 when operated in a GSM system. It is important to note that the TRF7610 was not designed to work under CW conditions with a similar dissipated power as given in equation (23).

In a GSM system with a 13-percent duty cycle, the average amount of dissipated power during operation is only 0.13 x 5.4 W or 0.7 W. Using this value in the calculation of the required case-to-ambient thermal resistance for a GSM system yields:

$$R_{\theta CA} \leq [(T_{J(max)} - T_{A(max)}) \div (\mathrm{P_D\ x\ duty\ cycle})] - R_{\theta JC}\ (in\ ^{\circ}C/W) \tag{24}$$

$$\leq [(150 – 85) \div (5.4 \times 0.13)] - 3.5 \cong 89.4\ ^{\circ}C/W$$

As a result of this calculation, the thermal transfer system should have a thermal resistance that is lower than 89 °C/W for GSM applications to maintain a junction temperature less than 150 °C at an ambient temperature of 85 °C.

5 Summary

Circuit designers must always consider the effects of thermal stackup – the cascaded effect of the transfer of heat from a device die to the surrounding package, from the package to a PCB or board-mounted heatsink, and finally from the heatsink to ambient. The flow of heat from the device die to ambient must be sufficient to maintain an acceptably low junction temperature, and with it maximize device reliability.

The total thermal resistance can be found from the sum of the individual thermal resistances between the device junction and ambient. Since the circuit designer cannot control a device's junction-to-case thermal resistance, special attention must be paid to controlling the thermal resistance from the device case to ambient, which includes the case-to-sink and the heatsink-to-ambient thermal resistances.

One of the circuit designer's goals is to minimize the thermal resistance of the entire circuit. Equations, analysis procedures, and examples are provided here to assist the designer in understanding the thermal characteristics of surface-mount RF power devices and the thermal performance of related materials. The methods outlined are useful for first-order approximations of the permissible dissipated powers of surface-mount integrated circuits.

6 References

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