TCM4300
Data Manual

Advanced RF Cellular Telephone Interface Circuit (ARCTIC™)

SLWS010G
February 1998

TEXAS INSTRUMENTS

Printed on Recycled Paper

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1 Introduction

Texas Instruments (TI™) TCM4300 IS-54B advanced RF cellular telephone interface circuit (ARCTIC™) provides a baseband interface between the digital signal processor (DSP), the microcontroller, and the RF modulator/demodulator in a dual-mode IS-54B cellular telephone. See the *TCM4300 functional block diagram*.

In the analog mode, the TCM4300 provides all required baseband filtering as well as transmit D/A conversion and receive A/D conversion using dual 10-bit sigma-delta converters. In addition, a wide-band data (WBD) –10 kb/s Manchester frequency shift key (FSK) demodulator is provided to allow reduced DSP processing load during subscriber standby mode.

In the digital mode, the TCM4300 accepts I and Q baseband data and performs A/D and D/A conversion and square-root raised-cosine filtering using dual 10-bit sigma-delta converters. The TCM4300 also has a $\pi/4$-DQPSK modulation encoder for dibit-to-symbol conversion in the digital transmit mode.

The microcontroller interface is compatible with a wide range of microcontrollers. A microcontroller can be used to communicate with the user interface (keyboard, display, etc.) and to program up to three frequency synthesizers by using the on-chip synthesizer interface circuit.

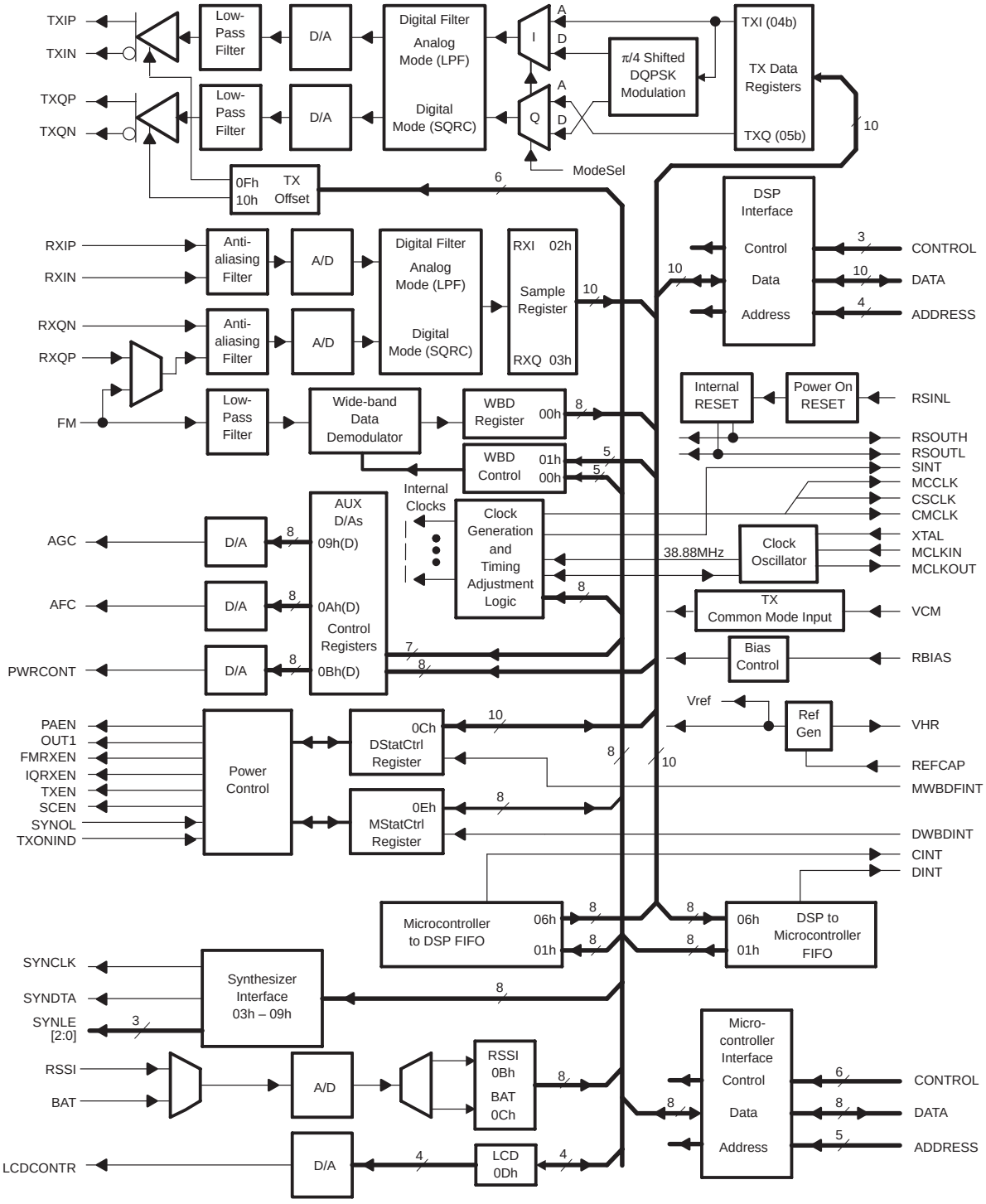
The TCM4300 provides advanced power control to minimize the power consumption of many dual-mode telephone functional blocks such as the speech codec, FM receiver, I and Q demodulator, transmitter signal processor, and RF power amplifier. In addition, the TCM4300 is designed to reduce system power consumption through low-voltage operation and standby mode.

The TCM4300 is offered in the 100-pin PZ package and is characterized for free-air operation from –40°C to 85°C.

1.1 Features

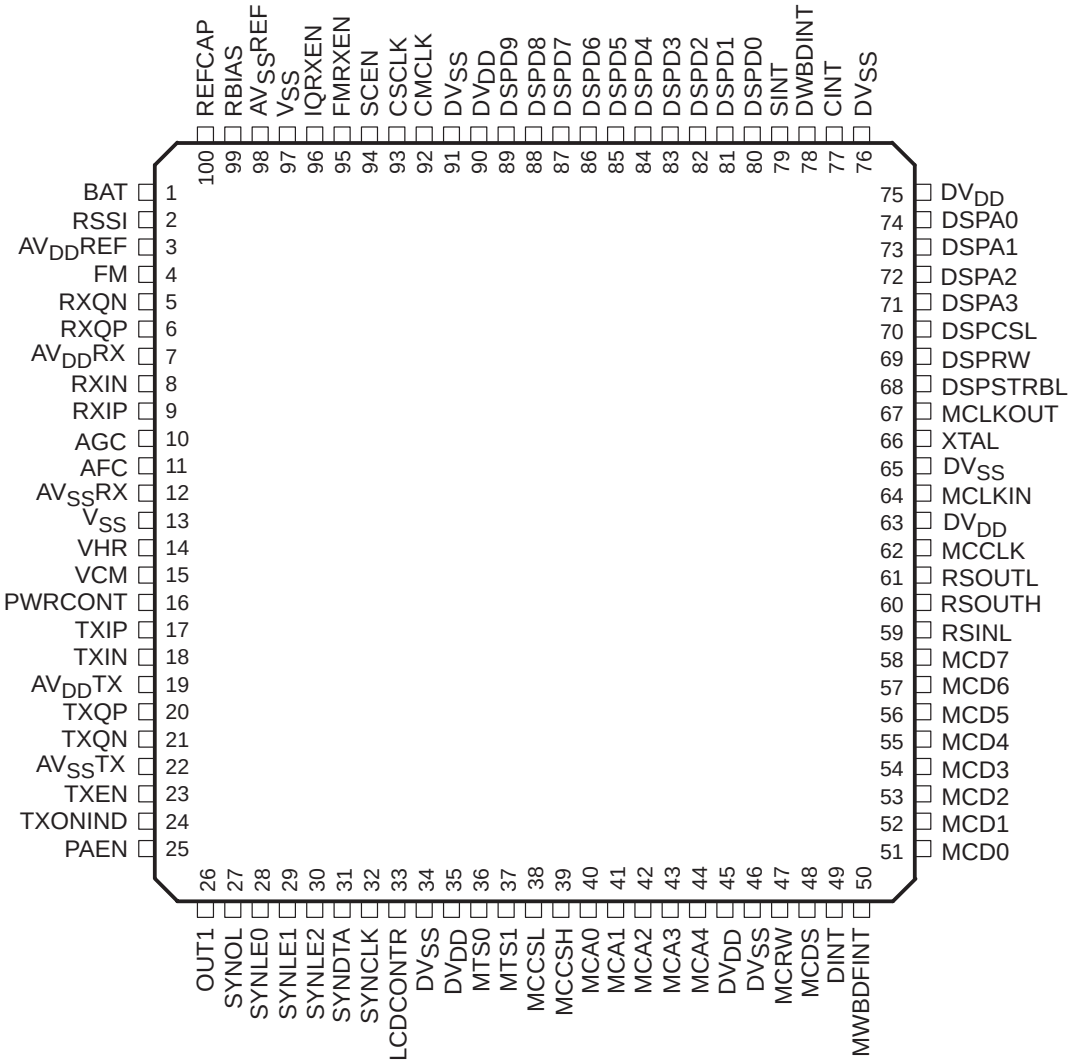
- Compliance With TIA IS-54B Dual-Mode Cellular Standard
- Baseband Transmit Digital-to-Analog (D/A) Conversion and Receive Analog-to-Digital (A/D) Conversion in Analog Transmit Mode Using Dual 10-Bit Sigma-Delta Converters
- Square Root Raised Cosine (SQRC) Filtering in the Digital Mode Using Dual 10-Bit Sigma-Delta Converters
- $\pi/4$-Differential Quadrature Phase-Shift Key (DQPSK) Modulation Encoder in Digital Transmit Mode
- Power Control Supervision for Radio Frequency (RF) Power Amplifier, Automatic Frequency Control (AFC), Automatic Gain Control (AGC), and Synthesizer
- Received Signal Strength Indicator (RSSI) and Battery-Level A/D Conversion Circuitry
- Internal Clock Generation
- WBD Clock Recovery and Manchester Decoding
- General-Purpose DSP and Microcontroller Interface
- 3.3-V and 5-V Operation
- Low Power Consumption

1.2 TCM4300 Functional Block Diagram



1.3 Pin Assignments

PZ PACKAGE
(TOP VIEW)



1.4 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AFC	11	O	Automatic frequency control. The AFC DAC output provides the means to adjust system temperature-compensated reference oscillator (TCXO).
AGC	10	O	Automatic gain control. The AGC digital-to-analog converter (DAC) output can be used to control the gain of system receiver circuits.
$AV_{DD}REF$	3	—	Analog supply voltage for FM receive path. Power applied to $AV_{DD}REF$ powers the FM receive path circuitry.
$AV_{DD}RX$	7	—	Analog supply voltage for receive path. Power applied to $AV_{DD}RX$ powers the receive path circuitry.
$AV_{DD}TX$	19	—	Analog supply voltage for transmit path. Power applied to $AV_{DD}TX$ powers the transmit path circuitry.
$AV_{SS}REF$	98	—	Analog ground for REFCAP
$AV_{SS}RX$	12	—	Analog ground for receive path
$AV_{SS}TX$	22	—	Analog ground for transmit path
BAT	1	I	Battery strength monitor. A sample of the battery voltage is applied to BAT, and this sample monitors the battery strength.
CINT	77	O	Controller data interrupt. CINT is the microcontroller data interrupt (active low) signal that is sent to the DSP. CINT is caused by a microcontroller write to the Send-C interrupt register location.
CMCLK	92	O	Codec master clock. CMCLK provides a 2.048-MHz clock that is used as the master clock and bit clock for the speech codec.
CSCLK	93	O	Codec sample clock. CSCLK provides an 8-kHz frame synchronization pulse for the speech codec. CSCLK is also connected to the DSP for speech sample interrupts.
DINT	49	O	Microcontroller interrupt request. DINT is output when the DSP writes to the SEND DINT register location. DINT can be active high or low according to the levels of the MTS0 and MTS1 signals.
DSPA0	74	I	DSP 4-bit parallel address bus. DSPA0 through DSPA3 provides the address bus for the DSP interface. DSPA3 is the MSB, and DSPA0 is the LSB.
DSPA1	73		
DSPA2	72		
DSPA3	71		
DSPCSL	70	I	DSP chip select (active low). A low signal at DSPCSL enables the specific DSP addressed.
DSPD0	80	I/O/Z	DSP 10-bit parallel data bus. DSPD0 through DSPD9 provide a 10-bit data bus for the DSP. DSPD9 is the MSB, and DSPD0 is the LSB.
DSPD1	81		
DSPD2	82		
DSPD3	83		
DSPD4	84		
DSPD5	85		
DSPD6	86		
DSPD7	87		
DSPD8	88		
DSPD9	89		

† Z = high impedance

1.4 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DSPRW	69	I	DSP read/write. A high on DSPRW enables a read operation and a low enables a write operation to the DSP.
DSPSTRBL	68	I	DSP strobe low. The DSPSTRL (active low) is used in conjunction with DSPCSL to enable read/write operations to the DSP.
DV_{DD}	35, 45, 63, 75, 90	—	Digital power supply. All supply terminals must be connected together.
DV_{SS}	34, 46, 65, 76, 91	—	Digital ground. All supply terminals must be connected together.
DWBDINT	78	O	DSP wide-band data interrupt (active low). The DWBDINT output goes low to indicate that the WBD demodulation circuits have traffic on them.
FM	4	I	Frequency modulation. FM terminal is connected to the output of the FM discriminator.
FMRXEN	95	O	FM receive path enable. A high output from FMRXEN can be used to enable the power for the receiver FM path.
IQRXEN	96	O	In-phase and quadrature receive path enable. A high output on IQRXEN can be used to enable the power for receiver I/Q path.
LCDCONTR	33	O	Liquid-crystal display (LCD) contrast. This LCDCONTR control DAC can be used to control the amount of drive to the liquid crystal display.
MCLKOUT	67	O	Master clock out. MCLKOUT is a buffered version of MCLKIN.
MCA0	40	I	Microcontroller 5-bit parallel address bus. MCA0 through MCA4 provide a 5-bit bus to address the microcontroller. MCA4 is the MSB, and MCA0 is the LSB.
MCA1	41		
MCA2	42		
MCA3	43		
MCA4	44		
MCCLK	62	O	Microcontroller clock. MCCLK provides an adjustable frequency with 1.215 MHz at powerup.
MCCSH	39	I	Microcontroller interface chip-select. A high at MCCSH in conjunction with a low at MCCSL allows the microcontroller to read from or write to the TCM4300.
MCCSL	38	I	Microcontroller interface chip-select. A low at MCCSL in conjunction with a high at the MCCSH allows the microcontroller to read from or write to the TCM4300.
MCD0	51	I/O/Z	Microcontroller 8-bit parallel data bus. MCD0 through MCD7 provides an 8-bit parallel data bus to send/receive data to/from the microcontroller. MCD7 is the MSB, and MCD0 is the LSB.
MCD1	52		
MCD2	53		
MCD3	54		
MCD4	55		
MCD5	56		
MCD6	57		
MCD7	58		

† Z = high impedance

1.4 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
MCDS	48	I	Microcontroller data strobe. MCDS is configured by the signals present on MTS0 and MTS1.
MCLKIN	64	I	Master clock input. The MCLKIN frequency input requirement is 38.88 MHz ±100 ppm. A crystal can be connected between MCLKIN and XTAL to provide an oscillator circuit. As an alternative, XTAL can be left open and an external TTL/CMOS-level clock signal can be connected to MCLKIN.
MCRW	47	I	Microcontroller read/write. Microcontroller read/write operations are selected in accordance with the signals present on MTS0 and MTS1.
MTS0	36	I	Microcontroller type select configuration-control inputs. The interface is controlled by MTS (1:0) as follows: 00 – Intel™ microcontroller interface characteristics 10 – Mitsubishi™ and Motorola™ microcontroller 16-bit bus interface characteristics 01 – Motorola™ microcontroller 8-bit bus characteristics 11 – Reserved
MTS1	37	I	
MWBDFINT	50	O	Microcontroller interrupt request. A wide-band data-ready interrupt is output when the WBD demodulator is in analog mode or when a frame interrupt is sent by the DSP in digital mode. MWDBFINT can be active high or low according to the levels of the MTS0 and MTS1 signals.
OUT1	26	O	Output number 1. OUT1 provides a user-defined general purpose data or control signal.
PAEN	25	O	Power amplifier enable. PAEN can be used to enable the transmit power amplifier. This signal is active high.
PWRCONT	16	O	Power amplifier (PA) power control. The PWRCONT DAC output can be used to control the amount of power output from the PA.
RBIAS	99	I	Input for bias current-setting resistor. To achieve correct bias voltage, a 100-kΩ, 1% tolerance resistor connected between RBIAS and AV_{SS} is recommended.
REFCAP	100	I	Reference decoupling capacitor. For proper decoupling, It is recommended that a 3.3 μF capacitor in parallel with a 470-pF capacitor be connected between REFCAP and ground.
RSINL	59	I	Reset input low. An active low applied to RSINL resets the TCM4300.
RSSI	2	I	Received signal strength indicator. RSSI samples received signal strength.
RSOUTH	60	O	Reset out high. An active high is output from RSOUTH for 10 ms after the TCM4300 is powered up.
RSOUTL	61	O	Reset out low. An active low is output from RSOUTL for 10 ms after the TCM4300 is powered up.
RXIN	8	I	Negative receive input. The in-phase differential negative baseband received signal is applied to RXIN.
RXIP	9	I	Positive receive input. The in-phase differential positive baseband received signal is applied to RXIP.
RXQN	5	I	Negative receive input. The quadrature negative baseband received signal is applied to RXQN.
RXQP	6	I	Positive receive input. The quadrature differential positive baseband received signal is applied to RXQP.

1.4 Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
SCEN	94	O	Speech CODEC enable. A high out from SCEN can enable the speech CODEC.
SINT	79	O	Sample interrupt. SINT is active low. In the analog mode, SINT occurs at 40 kHz; in the digital mode, SINT occurs at 48.6 kHz.
SYNCLK	32	O	Synthesizer clock. SYNCLK clocks the serial data stream.
SYNDTA	31	O	Synthesizer serial-data. SYNDTA provides the serial bit stream output.
SYNLE0	28	O	Synthesizer 0, 1, and 2 latch enables. An active high on SYNLE0, SYNLE1, and SYNLE2 indicates that the latch is enabled.
SYNLE1	29	O	
SYNLE2	30	O	
SYNOL	27	I	Synthesizer out-of-lock. An active high at SYNOL indicates a synthesizer is not locked.
TXEN	23	O	Transmit power enable. An active high output from TXEN can be used to enable various system transmitter-circuit devices.
TXIN	18	O	In-phase differential negative baseband transmit. The negative component of the differential baseband transmit signal is output from TXIN.
TXIP	17	O	In-phase differential positive baseband transmit. The positive component of the differential baseband transmit signal is output from TXIP.
TXONIND	24	I	Transmit on indicator. A signal is applied to TXONIND to indicate that power is applied to the power amplifier.
TXQN	21	O	Quadrature differential negative baseband transmit. The negative component of the quadrature differential transmit signal is output from TXQN.
TXQP	20	O	Quadrature differential positive baseband transmit. The positive component of the quadrature differential transmit signal is output from TXQP.
VCM	15	I	Voltage common mode. VCM establishes the dc operating point for transmit outputs and can be tied to VHR.
VHR	14	O	Voltage half-rail. The voltage level at VHR is approximately 0.5 $\times$ AV_{DD}. VHR establishes the dc operating point for receive inputs.
V_{SS}	13, 97	—	Substrate ground
XTAL	66	I	Crystal input. A crystal connected between XTAL and MCLIN forms an oscillator circuit.

2 Electrical Specifications

This section lists the electrical specifications, the absolute maximum ratings, the recommended operating conditions and operating characteristics for the TCM4300 Advanced RF Cellular Telephone Interface Circuit.

2.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage range:

- DV_{DD} (see Notes 1 and 2) . . . . . V_{SS} –0.3 V to AV_{DD} +0.3 V
- AV_{DD} (see Notes 2 and 3) . . . . . V_{SS} –0.3 V to DV_{DD} +0.3 V

Input voltage range, V_I: Digital signals . . . . . V_{SS} –0.3 V to DV_{DD} +0.3 V

Analog signals . . . . . V_{SS} –0.3 V to AV_{DD} +0.3 V

Output voltage range, V_O: Digital signals . . . . . V_{SS} to DV_{DD}

Analog signals . . . . . V_{SS} to AV_{DD}

Continuous total power dissipation . . . . . See Dissipation Rating Table

Operating free-air temperature range, T_A . . . . . –40°C to 85°C

Storage temperature range, T_{stg} . . . . . –65°C to 150°C

Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect DV_{SS}.
2. Maximum supplied voltage should not exceed 6 V.
3. Voltage values are with respect to AV_{SS}.

2.2 Dissipation Rating Table

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
PZ	1530 mW	15.25 mW/°C	615 mW

2.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, DV_{DD}		3		5.5	V
High-level input voltage, V_{IH}	Digital	0.7 DV_{DD}		DV_{DD}+0.3	V
Low-level input voltage, V_{IL}	Digital	0		0.3 DV_{DD}	V
High-level output voltage, V_{OH}	Digital	0.7 DV_{DD}		DV_{DD}	V
Low-level output voltage, V_{OL}	Digital	0		0.5	V
High-level output current at 3 V, I_{OH}	Digital	2			mA
Low-level output current at 3 V, I_{OL}	Digital	2			mA
High-level output current at 5 V, I_{OH}	Digital	2			mA
Low-level output current at 5 V, I_{OL}	Digital	2			mA
Load capacitance, transmit I and Q channel outputs			50		pF
VCM input voltage range, transmit I and Q channel outputs		1.3		AV_{DD}–1.3	V
Load resistance, auxiliary DACs			10		kΩ
Load capacitance, auxiliary DACs			50		pF
Operating free-air temperature, T_A		–40		85	°C

2.4 Electrical Characteristics Over Full Range Of Operating Conditions (Unless Otherwise Noted)

2.4.1 Power Consumption

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Analog transmitting and receiving		DV_{DD} = 3 V,	AV_{DD} = 3 V		65	75	mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		250	275	
Digital receiving		DV_{DD} = 3 V,	AV_{DD} = 3 V		55	60	mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		225	250	
Digital transmitting		DV_{DD} = 3 V,	AV_{DD} = 3 V		55	70	mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		210	250	
Idle mode	MCLKOUT enabled	DV_{DD} = 3 V,	AV_{DD} = 3 V		33	40	mW
	MCLKOUT disabled	DV_{DD} = 3 V,	AV_{DD} = 3 V		14	17	
	MCLKOUT enabled	DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		150	160	
	MCLKOUT disabled	DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		80	90	
Digital mode, 1/3 transmitting +1/3 receiving + 1/3 standby		DV_{DD} = 3 V,	AV_{DD} = 3 V		50	60	mW
		DV_{DD} = 5.5 V,	AV_{DD} = 5.5 V		205	220	

† All typical values are at T_A = 25°C.

2.4.2 Reference Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OH(VHR)}$	High-level output voltage		0.5 AV_{DD}–0.2		0.5 AV_{DD}+0.2	V
r_o	Output resistance	FMVOX or IQRXEN or TXEN = high		80	100	Ω
		FMVOX or IQRXEN or TXEN = low	15	40		kΩ

† All typical values are at DV_{DD} = 5 V, AV_{DD} = 5 V, and T_A = 25°C

2.4.3 Terminal Impedance

FUNCTION		MIN	TYP†	MAX	UNIT
Receive channel input impedance (single ended), RXIP/N and RXQP/N		40	70		kΩ
Transmit channel output impedance (single ended), TXIP/N and TXQP/N		40	50	100	Ω
FM input impedance, WBD		25	200		kΩ
MCLKOUT impedance	MCLKOUT at 3.3 V		240		Ω
	MCLKOUT at 5 V		180		

† All typical values are at DV_{DD} = 5 V, AV_{DD} = 5 V, and T_A = 25°C, unless otherwise specified.

2.4.4 RXIP, RXIN, RXQP, and RXQN Inputs (AV_{DD} = 3 V, 4.5 V, 5 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range			0.3		AV_{DD}–0.3	V
Input voltage for full-scale digital output	Differential			0.5		Vp-p
	Single ended			0.5		
Nominal operating level	Differential			0.125		Vp-p†
	Single ended			0.125		
Input CMRR (RXI, RXQ)			45			dB
Sampling frequency, SINT (digital mode)				48.6		kHz
Sampling frequency, SINT (analog mode)				40		kHz
Receive error vector magnitude (EVM)				5%	6%	
I/Q sample timing skew		Input signal 0 – 15 kHz		50		ns
A/D resolution				10		bits
Signal-to-noise plus distortion		Input at full scale – 1 dB	54	58		dB
Integral nonlinearity		0 dB to –60 dB input		1		LSB
Gain error (I or Q channel)					±7%	
Gain mismatch between I and Q					±0.3	dB
Differential dc offset voltage					±30	mV
FM input sensitivity, full scale (± 14-kHz deviation)				2.5		Vp-p
FM input dc offset (relative to VHR)					±80	mV
FM input idle channel noise, below full-scale input					–50	dB
FM gain error					±6%	
Power supply rejection		f = 0 kHz to 15 kHz		40		dB

† Provides 12-dB headroom for AGC fading conditions.

2.4.5 Transmit I and Q Channel Outputs

PARAMETER		MIN	TYP	MAX	UNIT
Peak output voltage full scale, centered at VCM	Differential		2.24		Vp
	Single ended		1.12		
Nominal output-level (constellation radius) centered at VCM	Differential		1.5		V
	Single ended		0.75		
Low-level drift			±200		PPM/°C
Transmit error vector magnitude (EVM)			3%	4%	
Transmit DACs I and Q resolution			8		bits
S/(N+D) ratio at differential outputs		48	52		dB
Gain error (I or Q channel)			±8%	±12%	
Gain mismatch between I and Q				±0.3	dB
Gain sampling mismatch between I and Q			20		ns
Zero code error, I to Q, with respect to other channel (differential or single ended)				±1.1	LSB
Residual offset error, I or Q, with respect to VCM				±0.55	LSB
Load impedance, between P and N terminals		10			kΩ
Transmit offset DACs I and Q resolution			6		bits
Transmit offset DACs I and Q average step size				5.0	mV
Transmit offset DACs differential nonlinearity				±1.1	LSB
Transmit offset DACs integral nonlinearity				±1.1	LSB

2.4.6 Auxiliary D/A Converters

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output range	AV_{DD} > 3 V†, AUXFS [1:0] = 00	0.2		2.5	V
	AV_{DD} > 4.5 V†, AUXFS [1:0] = 10	0.2		4	
	AV_{DD} > 5 V†, AUXFS [1:0] = 11	0.2		4.5	
Resolution AGC, AFC, PWRCONT DACs			8		bits
Resolution LCDCONTR DAC			4		bits
Gain + offset error (full scale) AGC, AFC, PWRCONT DAC				±3%	
Gain + offset error (full scale) LCDCONTR DAC				±7%	
Differential nonlinearity			±0.75	±1	LSB
Integral nonlinearity			±0.75	±1	LSB

† Range settings depends only on AUXFS [1:0]. The supply voltage is not detected.

2.4.7 Auxiliary D/A Converters Slope (AGC, AFC, PWRCONT)

AUXFS[1:0] SETTING	SLOPE	NOMINAL LSB VALUE (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 128 (MIDRANGE) (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 256† (MAX VALUE) (V)
00	2.5/256	0.0098	1.25	2.5
01	Do not use	Do not use	Do not use	Do not use
10	4/256	0.0156	2	4
11	4.5/256	0.0176	2.25	4.5

† The maximum input code is 255. The value shown for 256 is extrapolated.

2.4.8 Auxiliary D/A Converters Slope (LCDCONTR)

AUXFS[1:0] SETTING	SLOPE	NOMINAL LSB VALUE (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 8 (MIDRANGE) (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 16† (MAX VALUE) (V)
00	2.5/16	0.1563	1.25	2.5
01	Do not use	Do not use	Do not use	Do not use
10	4/16	0.2500	2	4
11	4.5/16	0.2813	2.25	4.5

† The maximum input code is 15. The value shown for 16 is extrapolated.

2.4.9 RSSI/Battery A/D Converter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input range	AV_{DD} = 3 V, 4.5 V, 5 V	0.2		2	V
Resolution			8		bits
Conversion time	AV_{DD} = 3 V, 4.5 V, 5 V		20		µs
Gain + offset error (full scale)			±3%	±4%	
Differential nonlinearity			±0.75	±1	LSB
Integral nonlinearity			±0.75	±1	LSB
Input resistance		1	2		MΩ

2.5 Operating Characteristics Over Full Range of Operating Conditions (Unless Otherwise Noted)

2.5.1 Receive (RX) Channel Frequency Response (RXI, RXQ Input in Digital Mode)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response	0.125 V peak-to-peak, 0 kHz to 8 kHz (see Note 4)		±0.5	±0.75	dB
	0.125 V peak-to-peak, 8 kHz to 15 kHz (see Note 5)			±1	
	0.125 V peak-to-peak, 16.2 kHz to 18 kHz (see Note 5)			–26	
	0.125 V peak-to-peak, 18 kHz to 45 kHz (see Note 5)			–30	
	0.125 V peak-to-peak, 45 kHz to 75 kHz (see Note 5)			–46	
	0.125 V peak-to-peak, > 75 kHz			–60	
Peak-to-peak group delay distortion	0.125 V peak-to-peak, 0 kHz to 15 kHz			2	µs
Absolute channel delay, RXI, Q IN to digital OUT	0.125 V peak-to-peak, 0 kHz to 15 kHz		325		µs

NOTES: 4. Deviation from ideal 0.35 square-root raised-cosine (SQRC) response
5. Stopband

2.5.2 Receive (RX) Channel Frequency Response (FM Input in Analog Mode)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response	2.5 V peak-to-peak, 0 kHz to 6 kHz (see Note 6)			±0.5	dB
	2.5 V peak-to-peak, 20 kHz to 30 kHz (see Note 5)			–18	
	2.5 V peak-to-peak, 34 kHz to 46 kHz (see Note 7)			–48	
Peak-to-peak group delay distortion	2.5 V peak-to-peak, 0 kHz to 6 kHz			2	µs
Absolute channel delay	2.5 V peak-to-peak, 0 kHz to 6 kHz		400		µs

NOTES: 5. Stopband
6. Ripple magnitude
7. Stopband and multiples of stopband

2.5.3 Transmit (TX) Channel Frequency Response (Digital Mode)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response	0 kHz to 8 kHz (see Note 4)			±0.3	dB
	8 kHz to 15 kHz (see Note 4)			±0.5	
	20 kHz to 45 kHz (see Note 5)			–29	
	45 kHz to 75 kHz (see Note 5)			–55	
	> 75 kHz (see Note 5)			–60	
	Any 30 kHz band centered at > 90 kHz (see Note 5)			–60	
Peak-to-peak group delay distortion	0 kHz to 15 kHz			3	µs
Absolute channel delay	0 kHz to 15 kHz		320		µs

NOTES: 4. Deviation from ideal 0.35 square-root raised-cosine (SQRC) response
5. Stopband

2.5.4 Transmit (TX) Channel Frequency Response (Analog Mode)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response	0 kHz to 8 kHz (see Note 4)			±0.5	dB
	8 kHz to 15 kHz (see Note 4)			±0.5	
	20 kHz to 45 kHz (see Note 5)			–31	
	45 kHz to 75 kHz (see Note 5)			–70	
	> 75 kHz (see Note 5)			–70	
	Any 30 kHz band centered at > 90 kHz (see Note 5)			–70	
Peak-to-peak group delay distortion	0 kHz to 15 kHz			3	µs
Absolute channel delay	0 kHz to 15 kHz		540		µs

NOTES: 4. Ripple magnitude
5. Stopband

3 Parameter Measurement Information

This section contains the timing waveforms and parameter values for MCLKOUT and several microcontroller interface configurations possible when using the TCM4300. The timing parameters are contained in Section 3.1 through Section 3.11. The timing waveforms are shown in Figures 3–1 through 3–11. All parameters shown in the separate waveforms have their values listed in an associated table. Not all parameter values listed in the tables are necessarily shown in an associated waveform.

3.1 MCLKOUT Timing Requirements (see Figure 3–1 and Note 1)

		MIN	NOM	MAX	UNIT
t_{wH}	Pulse duration , MCLKOUT high	9	10	12	ns
t_{wL}	Pulse duration, MCLKOUT low	9	10	12	ns
t_r	Rise time, MCLKOUT	2	3	4	ns
t_f	Fall time, MCLKOUT	2	3	4	ns

NOTE 1: Tested with 15 pF loading on MCLKOUT

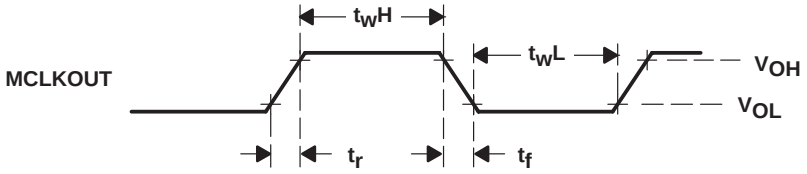
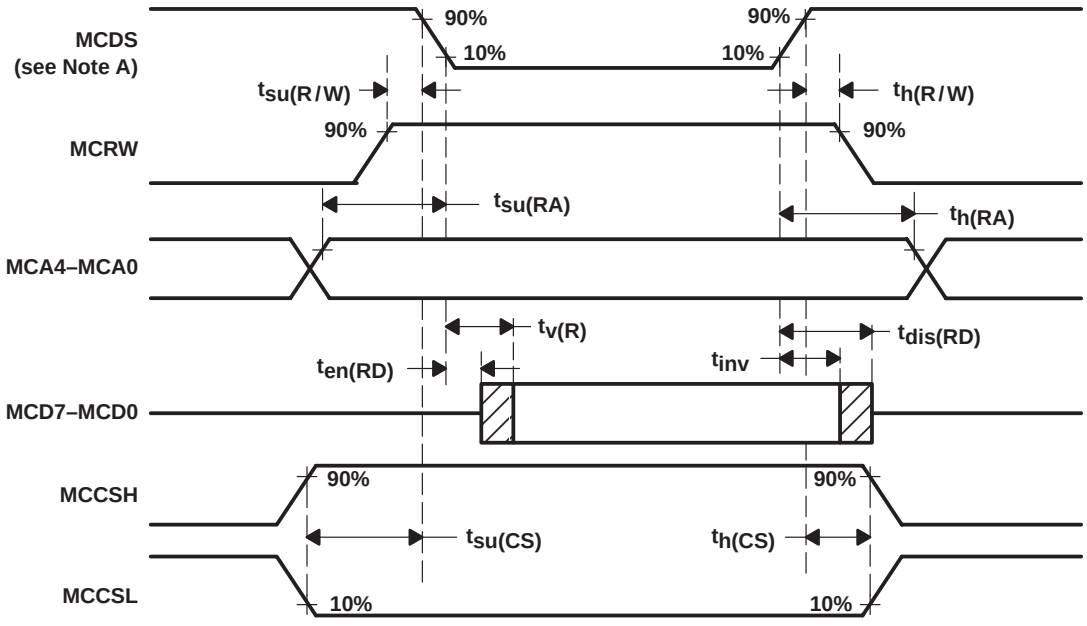


Figure 3–1. MCLKOUT Timing Diagram

3.2 TCM4300 to Microcontroller Interface Timing Requirements (Mitsubishi Read Cycle) (see Figure 3–2 and Note 2)

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write MCRW stable before falling edge of strobe MCDS	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write MCRW stable after rising edge of strobe MCDS	$TRW_{(HO)}$	10		ns
$t_{su(RA)}$	Setup time, read address MCS stable before falling edge of strobe MCDS	$TRA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address MCA stable after rising edge of strobe MCDS	$TRA_{(HO)}$	10		ns
$t_{en(RD)}$	Enable time, read data on falling edge of strobe MCDS to TCM4300 driving data bus MCD	$TRD_{(EN)}$	10		ns
$t_{v(R)}$	Valid time read data on falling edge of strobe MCDS to valid data MCD	$TRD_{(DV)}$		50	ns
$t_{(inv)}$	Data MCD invalid after rising edge of strobe MCDS	$TRD_{(INV)}$		10	ns
$t_{dis(RD)}$	Disable time, read data. TCM4300 releases MCD data bus after rising edge of strobe MCDS	$TRD_{(DIS)}$		28	ns
$t_{h(CS)}$	Hold time, chip select MCCSH and MCCSL stable before rising edge of strobe MCDS	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select MCCSH and MCCSL stable before falling edge of strobe MCDS	$TCS_{(SU)}$	0		ns

NOTE 2: Timings are based upon Mitsubishi 37732S4 (16 MHz) and Mitsubishi 3772S4L (8 MHz).



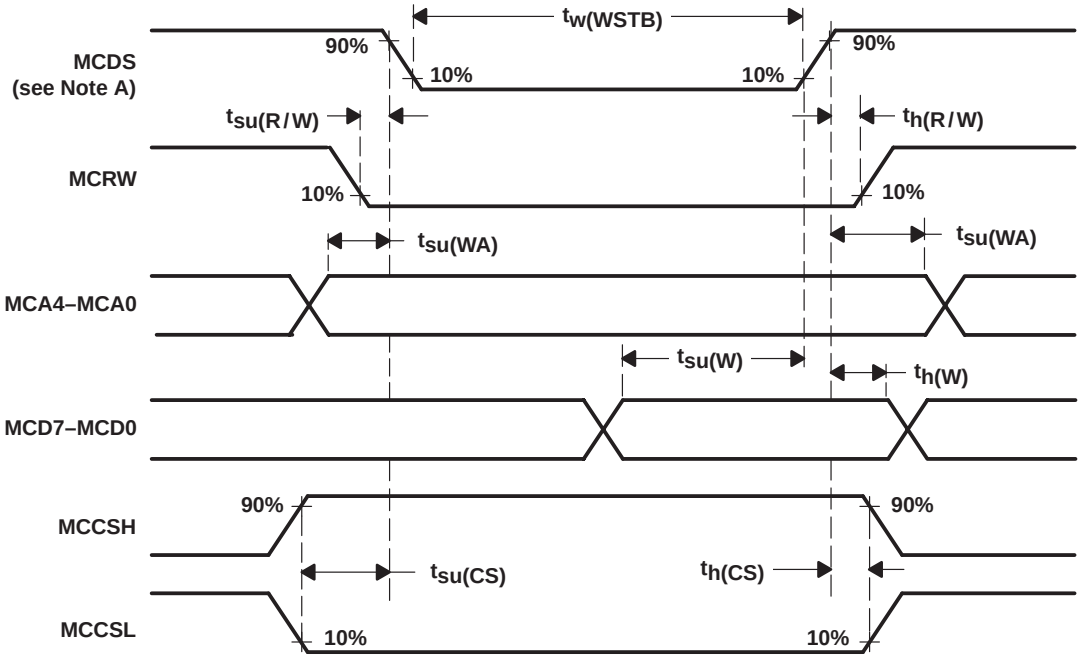
NOTE A: Chip selection is defined as both MCCS and MCDS active.

Figure 3–2. Microcontroller Interface Timing Requirements (Mitsubishi Configuration Read Cycle, MTS [1:0] = 10)

3.3 TCM4300 to Microcontroller Interface Timing Requirements (Mitsubishi Write Cycle) (see Figure 3–3 and Note 2)

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write MCRW stable before falling edge of strobe MCDS	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write MCRW stable after rising edge of strobe MCDS	$TRW_{(HO)}$	10		ns
$t_{su(WA)}$	Setup time, write/address MCA stable before falling edge of strobe MCDS	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address MCA stable after rising edge of strobe MCDS	$TWA_{(HO)}$	10		ns
$t_{su(W)}$	Setup time, write data stable MCD before rising edge of strobe MCDS	$TWD_{(SU)}$	14		ns
$t_{h(W)}$	Hold time, write data stable MCD after rising edge of strobe MCDS	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe pulse width low on MCDS	$TWR_{(STB)}$	60		ns
$t_{h(CS)}$	Hold time, chip select MCCSH and MCCSL stable before rising edge of strobe MCDS	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select stable MCCSH and MCCSL before falling edge of strobe MCDS	$TCS_{(SU)}$	0		ns

NOTE 2: Timings based upon Mitsubishi 37732S4 (16 MHz) and Mitsubishi 3772S4L (8 MHz).



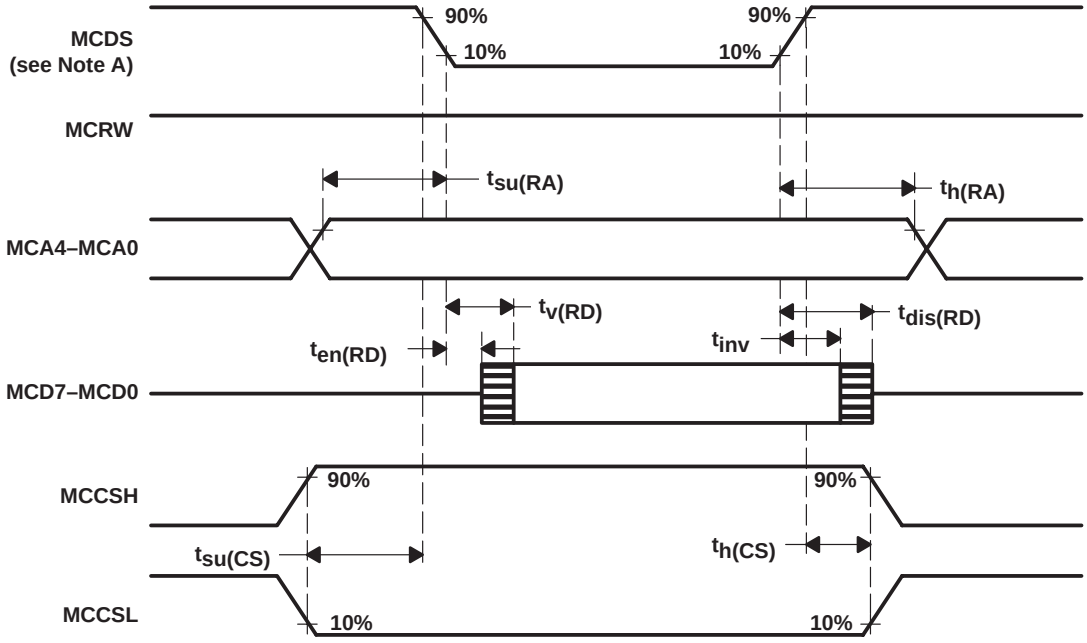
NOTE A: Chip selection is defined as both MCCS and MCDS active.

Figure 3–3. Microcontroller Interface Timing Requirements (Mitsubishi Configuration Write Cycle, MTS [1:0] = 10)

3.4 TCM4300 to Microcontroller Interface Timing Requirements (Intel Read Cycle) (see Figure 3–4 and Note 3)

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(RA)}$	Setup time, read address MCA stable before falling edge of strobe MCDS	$TRA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address MCA stable after rising edge of strobe MCDS	$TRA_{(HO)}$	10		ns
$t_{en(RD)}$	Enable time, read data on falling edge of strobe MCDS to TCM4300 driving data bus MCD	$TRD_{(EN)}$	10		ns
$t_{v(RD)}$	Valid time, read data on falling edge of strobe MCDS to valid data MCD	$TRD_{(DV)}$		50	ns
t_{inv}	Data MCD invalid after rising edge of strobe MCDS	$TRD_{(INV)}$		10	ns
$t_{dis(RD)}$	Disable time, read data. TCM4300 releases MCD data bus after rising edge of strobe MCDS	$TRD_{(DIS)}$		28	ns
$t_{su(CS)}$	Setup time, chip select MCCSH and MCCSL stable before falling edge of strobe MCDS	$TCS_{(SU)}$	0		ns
$t_{h(CS)}$	Hold time, chip select MCCSH and MCCSL stable before rising edge of strobe MCDS	$TCS_{(HO)}$	0		ns

NOTE 3: Timings are based upon Intel 80C186 (16 MHz).



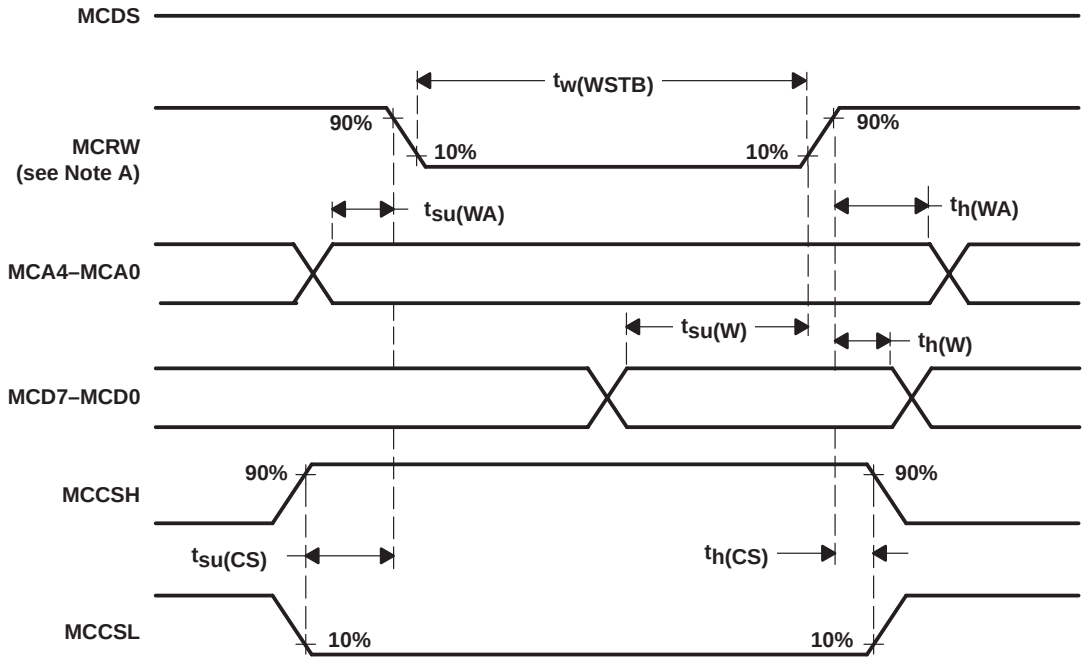
NOTE A: Chip selection is defined as both MCCS and MCDS active.

Figure 3–4. Microcontroller Interface Timing Requirements (Intel Configuration Read Cycle, MTS [1:0] = 00)

3.5 TCM4300 to Microcontroller Interface Timing Requirements (Intel Write Cycle) (see Figure 3–5 and Note 3)

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(WA)}$	Setup time, write address MCA stable before falling edge of strobe MCRW	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address MCA stable after rising edge of strobe MCRW	$TWA_{(HO)}$	10		ns
$t_{su(W)}$	Setup time, write data stable MCD before rising edge of strobe MCRW	$TWD_{(SU)}$	14		ns
$t_{h(W)}$	Hold time, write data stable MCD after rising edge of strobe MCRW	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe pulse width low on MCRW	$TWR_{(STB)}$	60		ns
$t_{su(CS)}$	Setup time, chip select MCCSH and MCCSL stable before falling edge of strobe MCRW	$TCS_{(SU)}$	0		ns
$t_{h(CS)}$	Hold time, chip select MCCSH and MCCSL stable before rising edge of strobe MCRW	$TCS_{(HO)}$	0		ns

NOTE 3: Timings are based upon Intel 8C186 (16 MHz).



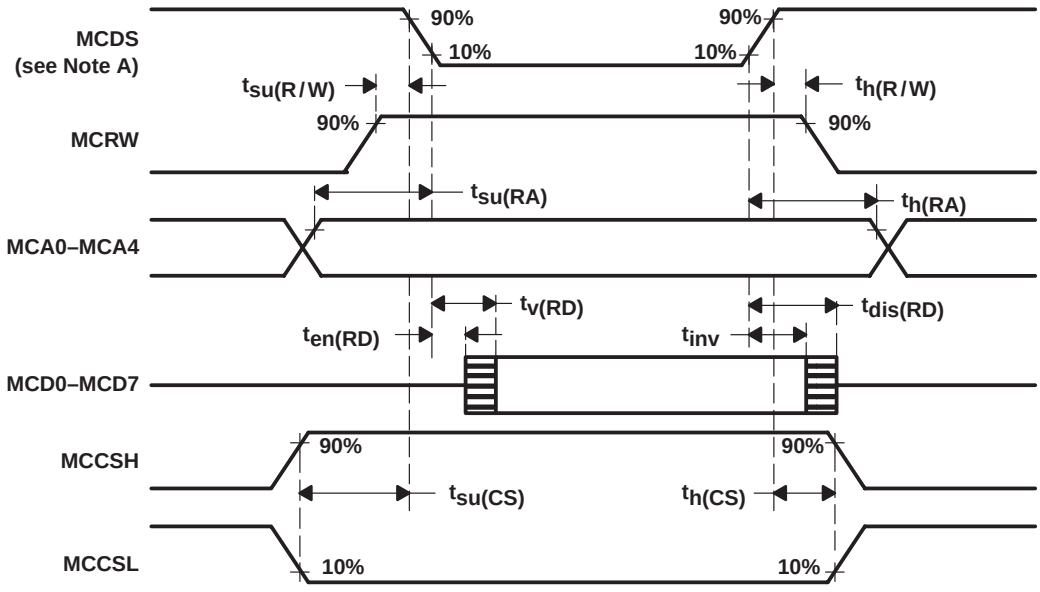
NOTE A: Chip selection is defined as both MCCS and MCRW active.

Figure 3–5. Microcontroller Interface Timing Requirements (Intel Configuration Write Cycle, MTS [1:0] = 00)

3.6 TCM4300 to Microcontroller Interface Timing Requirements (Motorola 16-Bit Read Cycle) (see Figure 3–6 and Note 4)

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write MCRW stable before falling edge of strobe MCDS	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write MCRW stable after rising edge of strobe MCDS	$TRW_{(HO)}$	10		ns
$t_{su(RA)}$	Setup time, read address MCA stable before falling edge of strobe MCDS	$TRA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address MCA stable after rising edge of strobe MCDS	$TRA_{(HO)}$	10		ns
$t_{en(RD)}$	Enable time, read data on falling edge of strobe MCDS to TCM4300 driving data bus MCD	$TRD_{(EN)}$	10		ns
$t_{v(RD)}$	Valid time, read data on falling edge of strobe MCDS to valid data MCD	$TRD_{(DV)}$		50	ns
t_{inv}	Data (MCD) invalid after rising edge of strobe MCDS	$TRD_{(INV)}$		10	ns
$t_{dis(RD)}$	Disable time, read data. TCM4300 releases MCD data bus after rising edge of strobe MCDS	$TRD_{(DIS)}$		28	ns
$t_{h(CS)}$	Hold time, chip select MCCSH and MCCSL stable before falling edge of strobe MCDS	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select stable MCCSH and MCCSL before rising edge of strobe MCDS	$TCS_{(SU)}$	0		ns

NOTE 4: Timings are based upon Motorola 68HC000 (16.67 MHz) and Motorola 68302 (16 MHz).



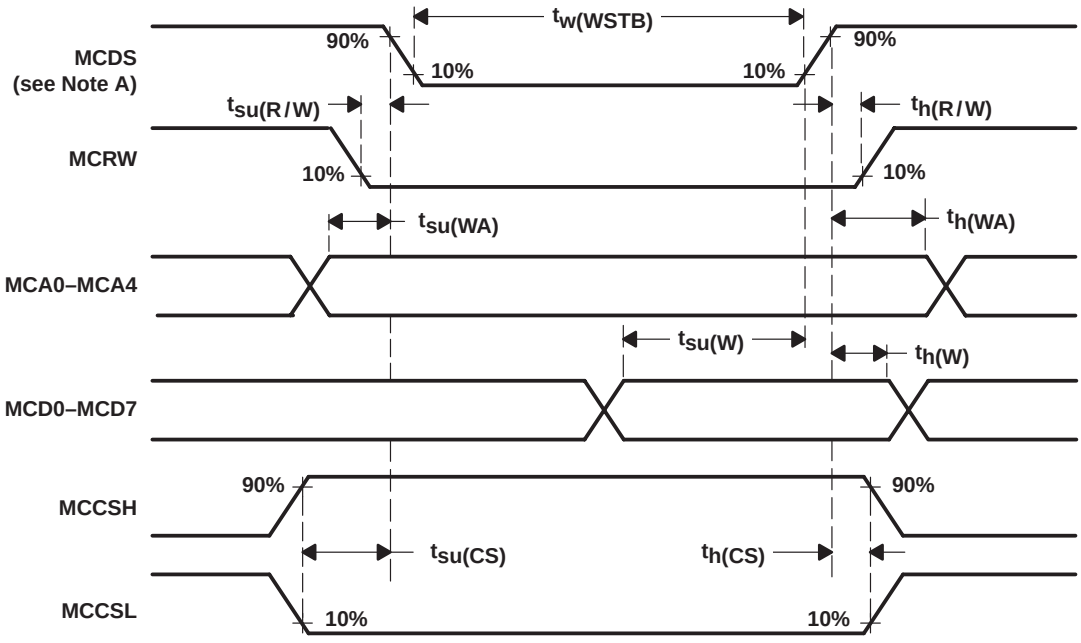
NOTE A: Chip selection is defined as both MCCS and MCDS active.

Figure 3–6. Microcontroller Interface Timing Requirements (Motorola 16-Bit Read Cycle, MTS [1:0] = 10)

3.7 TCM4300 to Microcontroller Interface Timing Requirements (Motorola 16-Bit Write Cycle) (see Figure 3–7 and Note 4)

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write MCRW stable before falling edge of strobe MCDS	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write MCRW stable after rising edge of strobe MCDS	$TRW_{(HO)}$	10		ns
$t_{su(WA)}$	Setup time, write address MCA stable before falling edge of strobe MCDS	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address MCA stable after rising edge of strobe MCDS	$TWA_{(HO)}$	10		ns
$t_{su(W)}$	Setup time, write data stable MCD before rising edge of strobe MCDS	$TWD_{(SU)}$	14		ns
$t_{h(W)}$	Hold time, write data stable MCD after rising edge of strobe MCDS	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe pulse width low on MCDS	$TWR_{(STB)}$	60		ns
$t_{h(CS)}$	Hold time, chip select MCCSH and MCCSL stable before falling edge of strobe MCDS	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select MCCSH and MCCSL stable before rising edge of strobe MCDS	$TCS_{(SU)}$	0		ns

NOTE 4: Timings are based upon Motorola 68HC000 (16.67 MHz) and Motorola 68302 (16 MHz).



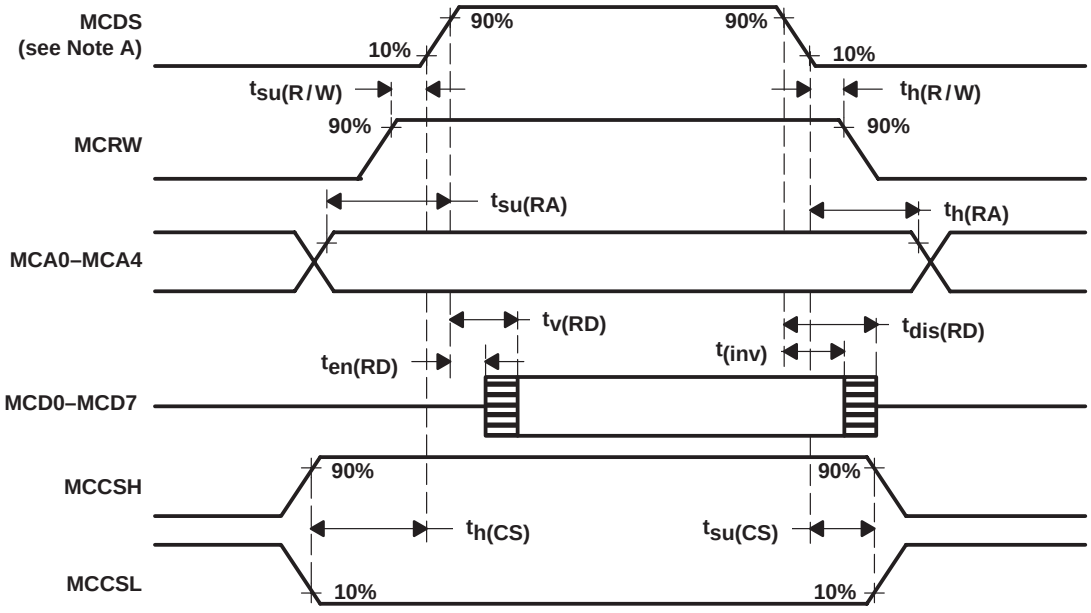
NOTE A: Chip selection is defined as both MCCS and MCDS active.

Figure 3–7. Microcontroller Interface Timing Requirements (Motorola 16-Bit Write Cycle, MTS [1:0] = 10)

3.8 TCM4300 to Microcontroller Interface Timing Requirements (Motorola 8-Bit Read Cycle) (see Figure 3–8 and Note 5)

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write MCRW stable before rising edge of strobe MCDS	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write MCRW stable after falling edge of strobe MCDS	$TRW_{(HO)}$	10		ns
$t_{su(RA)}$	Setup time, read address MCA stable before rising edge of strobe MCDS	$TRA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address MCA stable after falling edge of strobe MCDS	$TRA_{(HO)}$	10		ns
$t_{en(RD)}$	Enable time, read data on rising edge of strobe MCDS to TCM4300 driving data bus MCD	$TRD_{(EN)}$	10		ns
$t_{v(RD)}$	Valid time, read data on rising edge of strobe MCDS to valid data MCD	$TRD_{(DV)}$		50	ns
t_{inv}	Data MCD invalid after falling edge of strobe MCDS	$TRD_{(INV)}$		10	ns
$t_{dis(RD)}$	Disable time, read data. TCM4300 releases MDS data bus after falling edge of strobe MCDS	$TRD_{(DIS)}$		28	ns
$t_{h(CS)}$	Hold time, chip select MCCSH and MCCSL stable before falling edge of strobe MCDS	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select MCCSH and MCCSL stable before rising edge of strobe MCDS	$TCS_{(SU)}$	0		ns

NOTE 5: Timings are based upon Motorola 68HC11D3 (3 MHz) and Motorola 68HC11G5 (2.1 MHz).



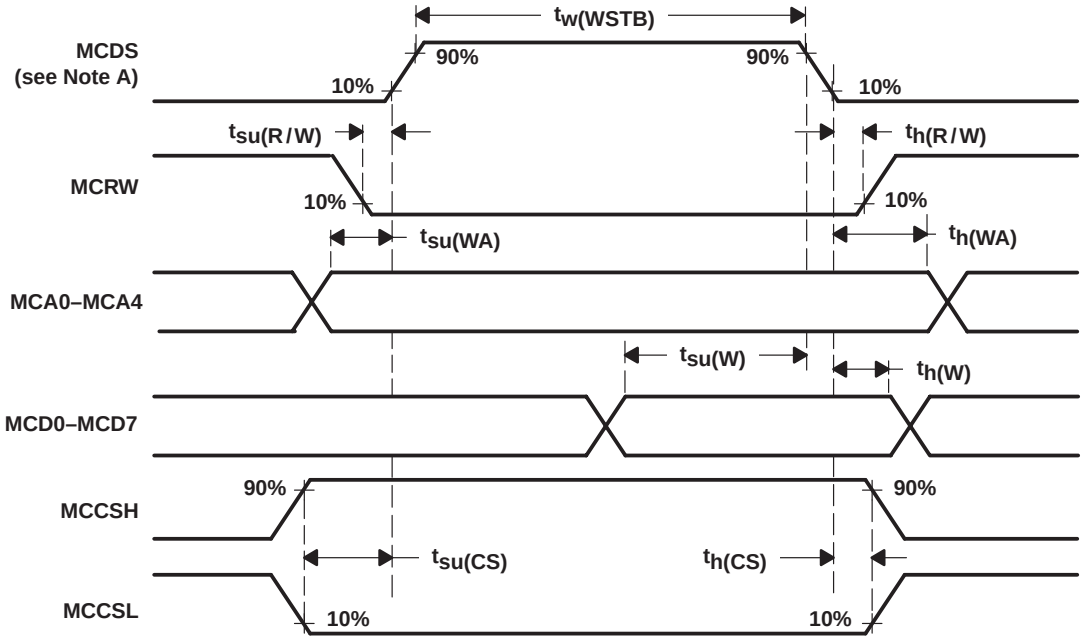
NOTE A: Chip selection is defined as both MCCS and MCDS active.

Figure 3–8. Microcontroller Interface Timing Requirements (Motorola 8-Bit Read Cycle, MTS [1:0] = 01)

3.9 TCM4300 to Microcontroller Interface Timing Requirements (Motorola 8-Bit Write Cycle) (see Figure 3–9 and Note 5)

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write MCRW stable before rising edge of strobe MCDS	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write MCRW stable after falling edge of strobe MCDS	$TRW_{(HO)}$	10		ns
$t_{su(WA)}$	Setup time, write address MCA stable before rising edge of strobe MCDS	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address MCA stable after falling edge of strobe MCDS	$TWA_{(HO)}$	10		ns
$t_{su(W)}$	Setup time, write data stable MCD before falling edge of strobe MCDS	$TWD_{(SU)}$	14		ns
$t_{h(W)}$	Hold time, write data stable MCD after falling edge of strobe MCDS	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe pulse width high on MCDS	$TWR_{(STB)}$	60		ns
$t_{h(CS)}$	Hold time, chip select MCCSH and MCCSL stable before rising edge of strobe MCDS	$TCS_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select MCCSH and MCCSL stable before falling edge of strobe MCDS	$TCS_{(SU)}$	0		ns

NOTE 5: Timings are based upon Motorola 68HC11D3 (3 MHz) and Motorola 68HC11G5 (2.1 MHz).



NOTE A: Chip selection is defined as both MCCS and MCDS active.

Figure 3–9. Microcontroller Interface Timing Requirements (Motorola 8-Bit Write Cycle, MTS [1:0] = 01)

3.10 Switching Characteristics, TCM4300 to DSP Interface (Read Cycle) (see Figure 3–10)

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write DSPRW stable before falling edge of strobe DSPSTRBL	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write DSPRW stable after rising edge of strobe DSPSTRBL	$TRW_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select stable DSPCSL before falling edge of strobe DSPSTRBL	$TCS_{(SU)}$	0		ns
$t_{h(CS)}$	Hold time, chip select DSPCSL stable after rising edge of strobe DSPSTRBL	$TCS_{(HO)}$	0		ns
$t_{su(RA)}$	Setup time, read address DSPA stable before strobe DSPSTRBL goes low	$TWA_{(SU)}$	0		ns
$t_{h(RA)}$	Hold time, read address DSPA stable after strobe DSPSTRBL goes high	$TWA_{(HO)}$	0		ns
$t_{en(R)}$	Enable time, read data on falling edge of strobe DSPSTRBL to TCM4300 driving data bus DSPD	$TRD_{(EN)}$	0		ns
$t_{d(DV)}$	Delay read data valid time on falling edge of strobe DSPSTRBL to valid data DSPD	$TRD_{(DV)}$		50	ns
$t_{h(R)}$	Hold time, read data DSPD invalid after rising edge of strobe DSPSTRBL	$TRD_{(INV)}$	5		ns
$t_{dis(R)}$	Disable time, read data. TCM4300 releases data bus after rising edge of strobe DSPSTRBL	$TRD_{(DIS)}$		12	ns

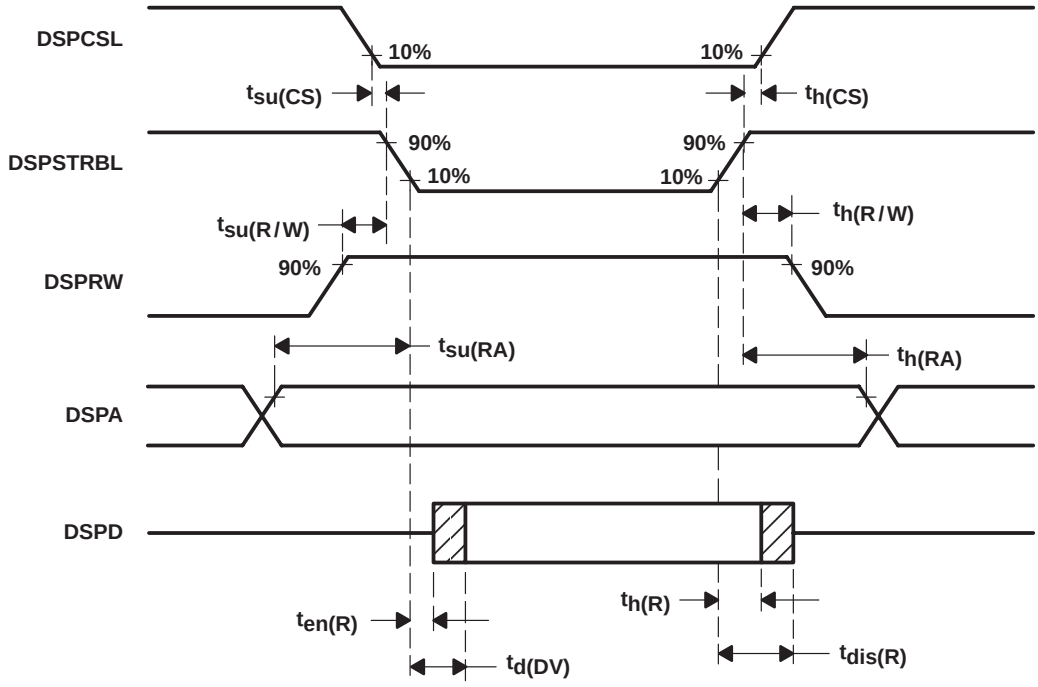


Figure 3–10. TCM4300 to DSP Interface (Read Cycle)

3.11 Switching Characteristics, TCM4300 to DSP Interface (Write Cycle) (see Figure 3–11)

PARAMETER		ALTERNATE SYMBOL	MIN	MAX	UNIT
$t_{su(R/W)}$	Setup time, read/write DSPRW stable before falling edge of strobe DSPSTRBL	$TRW_{(SU)}$	0		ns
$t_{h(R/W)}$	Hold time, read/write DSPRW stable after rising edge of strobe DSPSTRBL	$TRW_{(HO)}$	0		ns
$t_{su(CS)}$	Setup time, chip select stable DSPCSL before falling edge of strobe DSPSTRBL	$TCS_{(SU)}$	0		ns
$t_{h(CS)}$	Hold time, chip select DSPCSL stable after rising edge of strobe DSPSTRBL	$TCS_{(HO)}$	0		ns
$t_{su(WA)}$	Setup time, write address DSPA stable before falling edge of strobe DSPSTRBL	$TWA_{(SU)}$	0		ns
$t_{h(WA)}$	Hold time, write address DSPA stable after rising edge of strobe DSPSTRBL	$TWA_{(HO)}$	0		ns
$t_{su(W)}$	Setup time, write data stable DSPD before rising edge of strobe DSPSTRBL	$TWD_{(SU)}$	3		ns
$t_{h(W)}$	Hold time, write data stable DSPD after rising edge of strobe DSPSTRBL	$TWD_{(HO)}$	0		ns
$t_{w(WSTB)}$	Pulse duration, write strobe pulse width low on DSPSTRBL	$TWR_{(STB)}$	25		ns

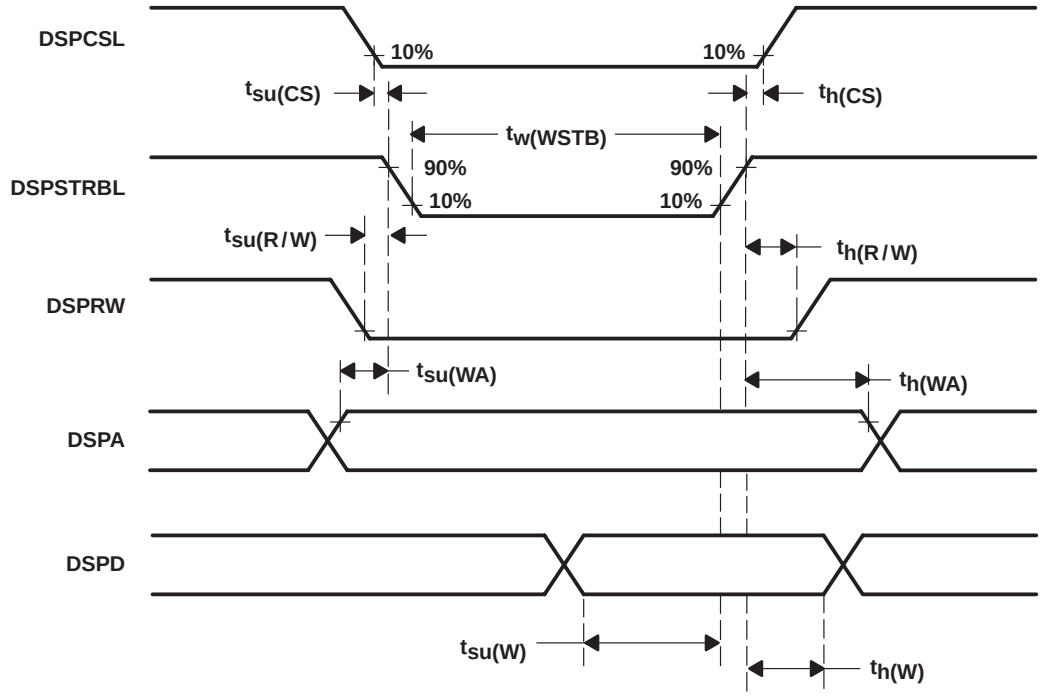


Figure 3–11. TCM4300 to DSP Interface (Write Cycle)

4 Principles of Operation

This section describes the operation of the TCM4300 in detail.

NOTE:

Timing diagrams and associated tables are contained in Section 3 of this data manual.

4.1 Data Transfer

The interface to both the system digital signal processor and microcontroller is in the form of 2s complement.

4.2 Receive Section

The mode of operation is determined by the state of the MODE, FMVOX, IQRXEN, and FMRXEN bits of the DStatCtrl register, as shown in Table 4–1.

Table 4–1. TCM4300 Receive Channel Control Signals

CONTROL SIGNAL	ANALOG MODE	DIGITAL MODE
MODE	0	1
FMVOX	1	0
IQRXEN	0	1
FMRXEN	1	0

In the digital mode (MODE=1), the receive section accepts RXIP, RXIN, RXQP, and RXQN analog inputs. These inputs are passed to continuous-time antialiasing filters (AAF), baseband filtering, and A/D conversion blocks, and then to sample registers where 10-bit registers can be read. The sample rate is 48.6 kilo samples per second (ksps).

In the analog mode (MODE = 0), the FMVOX bit of the DStatCtrl register enables or disables the Q side of the receiver channel, and the FMRXEN bit controls the external functions. In the digital mode, IQRXEN enables both the I and Q receive channels and external functions as well.

To save power, the receive I and Q channels are enabled separately. This operation occurs because in the analog mode, only the Q channel is used. When the FMVOX bit is set to 1, it controls the input multiplexer, connects the FM input to the receiver RXQP signal, and connects the RXQN signal to VHR. When the MODE control bit and the IQRXEN control bit are set to 1, both sides of the receive channel are enabled for use in the digital mode.

The input signals RXIP, RXIN and RXQP, RXQN are differential pair signals (see Table 4–2). Differential signals are used to minimize the pickup of interference, ground, and supply noise, while maintaining a larger signal level. In single-ended applications, the unused RXIN and RXQN terminals must be connected to VHR or to an externally supplied bias voltage equal to the dc value of the input signal, and the input signal level must be adjusted in the RF circuitry to provide the proper signal level so that the digital output codes are properly calibrated (0.5 V peak-to-peak corresponds to full-scale digital output). In the analog mode, the RXQN input is internally referenced to VHR. Alternatively, the unused inputs can be connected to VHR and the used inputs can be capacitively coupled. Note that when the RX and FM inputs are capacitively coupled, it is recommended that the input terminals be connected to VHR using a bias resistor.

Table 4–2. RXIP, RXIN, RXQP, and RXQN Inputs (AV_{DD} = 3 V, 4.5 V, 5 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range			0.3		AV_{DD}–0.3	V
Input voltage for full- scale digital output	Differential			0.5		Vp-p
	Single ended			0.5		
Nominal operating level	Differential			0.125		Vp-p†
	Single ended			0.125		
Input CMRR (RXI, RXQ)			45			dB
Sampling frequency, SINT (digital mode)				48.6		kHz
Sampling frequency, SINT (analog mode)				40		kHz
Receive error vector magnitude (EVM)				5%	6%	
I/Q sample timing skew		Input signal 0 – 15 kHz		50		ns
A/D resolution				10		Bits
Signal-to-noise plus distortion		Input at full scale – 1 dB	54	58		dB
Integral nonlinearity		0 dB to –60 dB input		1		LSB
Gain error (I or Q channel)					±7%	
Gain mismatch between I and Q					±0.3	dB
Differential dc offset voltage					±30	mV
FM input sensitivity, for full scale (±14-kHz deviation)				2.5		Vp-p
FM input dc offset (relative to VHR)					±80	mV
FM input idle channel noise, below full scale input					–50	dB
FM gain error					±6%	
Power supply rejection		f = 0 kHz to 15 kHz		40		dB

† Provides 12-dB headroom for AGC fading conditions.

It is recommended that the single-ended output of an external FM discriminator be capacitively coupled to the FM terminal for analog mode voice and WBD reception. An external bias resistor is needed to bias the FM terminal to VHR. The signal at this terminal is conveyed to the Q side of the receiver using the multiplexer, and the other Q input is connected internally to the VHR reference voltage. The I input of the receive section circuitry is disabled in the analog mode. The FM signal passes through the antialiasing filter, as specified in Table 4–3, before passing through the A/D converter. The signal at the FM terminal is also routed directly to the WBD demodulator through a low-pass filter (LPF) with the –3 dB point at 270 kHz.

Table 4–3. Receive (RX) Channel Frequency Response (FM Input in Analog Mode)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response	2.5 V peak-to-peak	0 kHz to 6 kHz (see Note 1)			±0.5	dB
		20 kHz to 30 kHz (see Note 2)			–18	
		34 kHz to 46 kHz (see Note 3)			–48	
Peak-to-peak group delay distortion	2.5 V peak-to-peak,	0 kHz to 6 kHz			2	µs
Absolute channel delay	2.5 V peak-to-peak,	0 kHz to 6 kHz		400		µs

NOTES: 1. Ripple magnitude
2. Stopband
3. Stopband and multiples of stopband

The VHR can provide a bias voltage for the received inputs when capacitively coupled from the RF section. To meet noise requirements, the VHR output should have an external decoupling capacitor connected to ground. The VHR output buffer is enabled by the OR of TXEN, FMVOX, and IQRXEN. The VHR output is high impedance otherwise.

In the digital mode, both the I and Q receive sides are enabled. Table 4–4 lists the receive channel frequency response.

Table 4–4. Receive (RX) Channel Frequency Response (RXI, RXQ Input in Digital Mode)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Frequency response	0.125 V peak-to-peak	0 kHz to 8 kHz (see Note 4)		±0.5	±0.75	dB
		8 kHz to 15 kHz (see Note 4)			±1	
		16.2 kHz to 18 kHz (see Note 2)			–26	
		18 kHz to 45 kHz (see Note 2)			–30	
		45 kHz to 75 kHz (see Note 2)			–46	
		> 75 kHz			–60	
Peak-to-peak group delay distortion	0.125 V peak-to-peak,	0 kHz to 15 kHz			2	µs
Absolute channel delay, RXI, Q IN to digital OUT	0.125 V peak-to-peak,	0 kHz to 15 kHz		325		µs

NOTES: 2. Stopband
4. Deviation from ideal 0.35 square-root raised-cosine (SQRC) response.

When the I and Q sample conversion is complete and the data is placed in the RXI and RXQ sample registers, the SINT interrupt line is asserted to indicate the presence of that data. This occurs at 48.6-kHz rate in the digital mode and at 40-kHz rate in the analog mode. In the analog mode, only the RXQ conversion path is used, and the RXI path is powered down.

4.3 Transmit Section

The transmit section operates in two distinct modes, digital or analog. The mode of operation is determined by the MODE bit of the DStatCtrl register. In the digital mode, data is input to the transmit section by writing to the TXI register. The resulting output is a $\pi/4$ DQPSK-modulated time division multiplexed (TDM) burst. In the analog mode, the data is in the form of direct I and Q samples which are written to both the TXI and TXQ registers, then D/A converted, filtered, and output through TXIP, TXIN, TXQP, and TXQN. The I and Q outputs are zero-IF FM signals; that is, no baseband connection is necessary for FM transmission.

In the digital mode (MODE = 1), the data is written to the TXI register using the SINT interrupt to synchronize the data transfer. The TCM4300 performs parallel-to-serial conversion of the bits in the TXI register and encodes the resulting bit stream as $\pi/4$ DQPSK data samples. These samples are then filtered by a digital

SQRC shaping filter with a roll-off rate of $\alpha = 0.35$ and converted to sampled analog form by two 9-bit DACs. The output of the DAC is then filtered by a continuous-time resistance-capacitance (RC) filter.

The TCM4300 generates a power amplifier (PA) control signal, PAEN, to enable the power supply for the PA. The start and stop times of the TDM burst are controlled by writing to a single bit, TXGO, in the DSP DStatCtrl register.

In the analog mode (MODE = 0), the DSP writes 8-bit I and Q samples into the TXI and TXQ data registers at a 40-ksps rate. These writes are timed by the SINT interrupt signal. The samples are fed to a low-pass filter before D/A conversion. In the transmit analog mode, PAEN is always set to 1.

The transmit section provides differential I and Q outputs (see Table 4-5) for both analog and digital modes. The differential dc offset for the TXI and TXQ outputs can be independently adjusted using the transmit offset registers.

Table 4–5. Transmit (TX) I and Q Channel Outputs

PARAMETER		MIN	TYP	MAX	UNIT
Peak output voltage full scale, centered at VCM	Differential		2.24		Vp
	Single ended		1.12		
Nominal output-level (constellation radius) centered at VCM	Differential		1.5		V
	Single ended		0.75		
Low-level drift			±200		PPM/°C
Transmit error vector magnitude (EVM)			3%	4%	
Transmit DACs I and Q resolution			8		bits
S/(N+D) ratio at differential outputs		48	52		dB
Gain error (I or Q channel)			±8%	±12%	
Gain mismatch between I and Q				±0.3	dB
Gain sampling mismatch between I and Q			20		ns
Zero code error, I to Q, with respect to other channel (differential or single ended). (See Figure 4–1).				±1.1	LSB
Residual offset error, I or Q, with respect to VCM. (See Note 5 and Figure 4–1).		10			kΩ
Load impedance, between P and N terminals		10			kΩ
Transmit offset DACs I and Q resolution			6		bits
Transmit offset DACs I and Q average step size				5.0	mV
Transmit offset DACs differential nonlinearity				±1.1	LSB
Transmit offset DACs integral nonlinearity				±1.1	LSB

NOTES: 5. The residual (uncorrectable) offset error is the residual offset error I or Q, with respect to VCM, which cannot be eliminated using the transmit offset DACs. The proper correction algorithm must be implemented to minimize the I and Q offset.

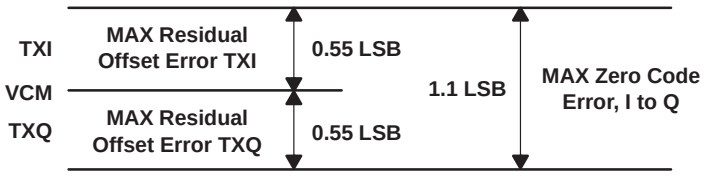


Figure 4–1. Residual (Uncorrectable) Offset Error and Zero Code Error, I to Q

Modulation Error: In the digital mode, during the transmit burst, the complex output of the transmitter circuits consists of an ideal output $s = I_{ideal} + jQ_{ideal}$ + error $e = e_i + je_q$. In Table 4-5, the modulation error vector magnitude (EVM) is defined as the peak value of the magnitude of e relative to the ideal output:

$$\text{Modulation error percentage} = 100 \frac{|e|}{|s|} \%$$

Table 4–6 and Table 4–7 show the frequency response of the transmit section for digital and analog mode, respectively.

Table 4–6. Transmit (TX) Channel Frequency Response (Digital Mode)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response	0 kHz to 8 kHz (see Note 4)			±0.3	dB
	8 kHz to 15 kHz (see Note 4)			±0.5	
	20 kHz to 45 kHz (see Note 2)			–29	
	45 kHz to 75 kHz (see Note 2)			–55	
	> 75 kHz (see Note 2)			–60	
	Any 30 kHz band centered at > 90 kHz (see Note 2)			–60	
Peak-to-peak group delay distortion	0 kHz to 15 kHz			3	µs
Absolute channel delay	0 kHz to 15 kHz		320		µs

NOTES: 2. Stopband
4. Deviation from ideal 0.35 SQRC response

Table 4–7. Transmit (TX) Channel Frequency Response (Analog Mode)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response	0 kHz to 8 kHz (see Note 1)			±0.5	dB
	8 kHz to 15 kHz (see Note 1)			±0.5	
	20 kHz to 45 kHz (see Note 2)			–31	
	45 kHz to 75 kHz (see Note 2)			–70	
	> 75 kHz (see Note 2)			–70	
	Any 30 kHz band centered at > 90 kHz (see Note 2)			–70	
Peak-to-peak group delay distortion	0 kHz to 15 kHz			3	µs
Absolute channel delay	0 kHz to 15 kHz		540		µs

NOTES: 1. Ripple magnitude
2. Stopband

4.4 Transmit Burst Operation (Digital Mode)

In the digital mode, the TCM4300 performs all encoding, signal processing, and power ramping for the burst. Start and stop timing of the variable length bursts are set by means of the TXGO bit in the DStatCtrl register. The SINT interrupt output interrupts the DSP at 48.6 kHz which is T/2 interval (T = 1 symbol period = 1/24.3 kHz). The burst is initiated by the DSP writing 1 to 5 dibits to the TXI register, a small positive-delay offset value d to the base station (BST) register, and a 1 to the TXGO bit in the DStatCtrl register.

The TXGO bit is sampled on the falling edge of SINT. The transmit outputs are held at zero differential voltage (each output terminal is held at the voltage supplied to the VCM input terminal) for 9.5 SINT periods (195.5 µs) plus BST offset delay after SINT has detected TXGO high; then the transmit outputs begin to ramp to the initial $\pi/4$ DQPSK constellation value. The shape of the ramp is the transient resulting from the internal

SQRC filtering. At the same time that the transmit outputs are beginning to ramp, the PAEN digital output goes high. This output can enable the power amplifier of a cellular radio transmitter. The TCM4300 transmit outputs reach the first $\pi/4$ DQPSK constellation value (maximum effect point, MEP) 6 SINT periods (3 symbol periods) after the start of the ramp.

The bit stream to be encoded as $\pi/4$ DQPSK symbols is generated by right shifts on each SINT of the TXI register with bit 0 (LSB) used first.

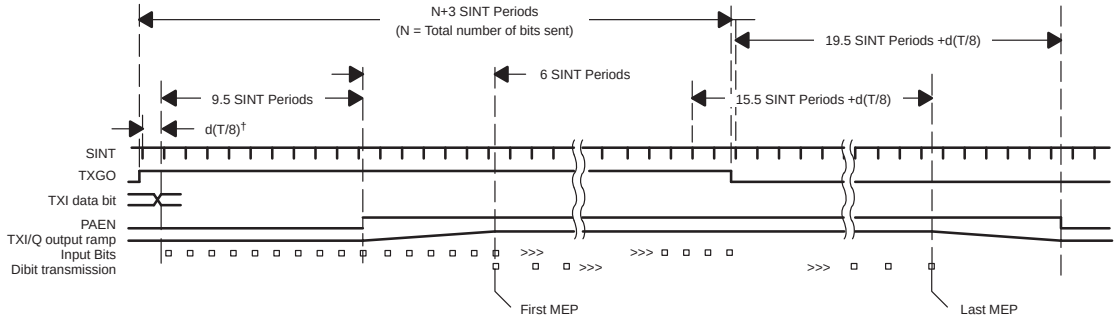
Previously written data continues to propagate through the TCM4300 internal filters until the last $\pi/4$ DQPSK constellation value (last MEP) occurs at the transmit outputs 15.5 SINT periods (318.9 μs) plus BST offset delay after the last symbol occurs (2 SINT periods before TXGO goes low); then the transmit outputs decay to zero differential voltage (each output at the voltage supplied to the VCM input terminal). The shape of the decay is the transient resulting from the internal SQRC filtering. The transmit outputs are held at zero differential voltage 6 SINT periods (3 symbol periods) after the start of the decay. At this time the PAEN digital output is set low (see Figure 4–2 and Figure 4–3).

Nonzero values of the BST offset register increase the delays of both the transmit waveforms and PAEN relative to the edges of TXGO after it is internally sampled by SINT. The delays are increased in increments of 1/4 SINT (1/8 symbol period).

For delays of 1 SINT or greater, the fractional part of the delay can be achieved using the BST offset register with the remaining integer SINT delay implemented externally by delaying the writing to TXGO and TXI.

The relative timing of PAEN and the transmit waveforms is not affected by the BST offset register.

The IS-54 standard describes shortened bursts and normal bursts. The two types differ in duration and number of transmitted bursts, burst length being determined by the TXGO bit.



† Total delay = d (SINT/4 or T/8) where d = integer value (0,1,2,3) written to the BST offset register.

Figure 4–2. Power Ramp-Up/Ramp-Down TIming Diagram

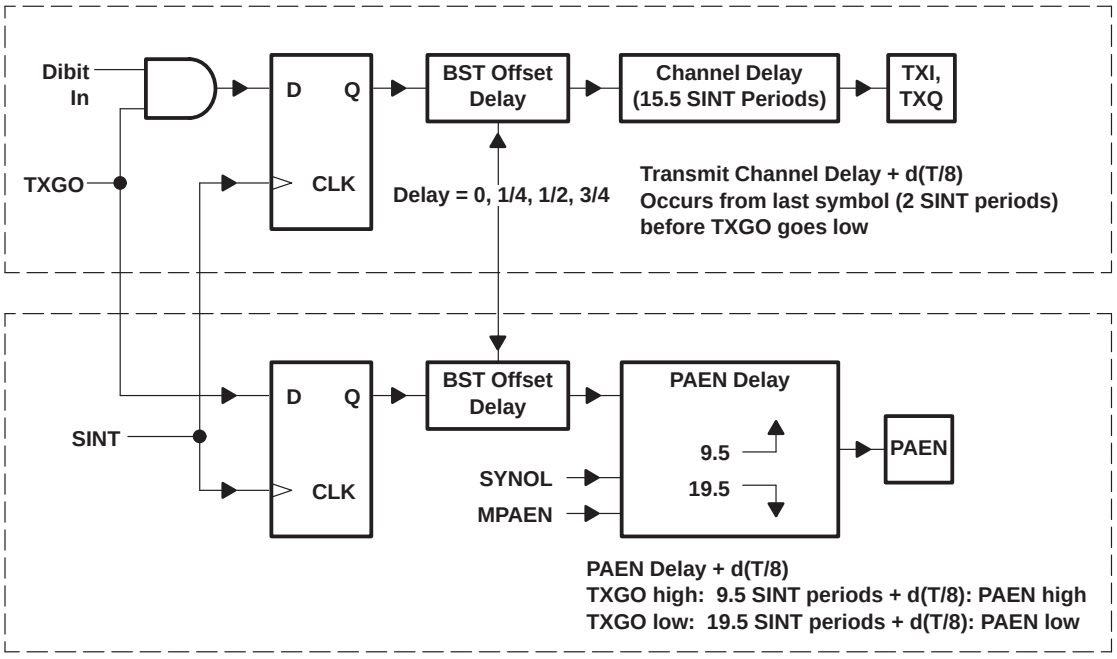


Figure 4–3. Transmit Power Ramp-Up/Ramp-Down Functional Diagram

4.5 Transmit I And Q Output Level

In the digital mode, the output level at TXI and TXQ is controlled by the TCM4300. During the burst, but not including ramp-up or ramp-down periods, the average output level $(I^2 + Q^2)^{1/2}$ should approximate the specified value. There is no variable level control for TXI and TXQ within the TCM4300 other than the fixed ramping. In the analog mode, the output of the TCM4300 depends only on the sample values written to the TXI and TXQ registers.

There are small differences in the average output power levels between the digital and the analog modes. These differences require compensation at the system level by a small attenuation in the sample values of the analog output.

When a change in transmit power is necessary, the microcontroller can change the value sent to the PWRCONT DAC, the output of which can be connected to a voltage-controlled attenuator in the transmit path of the RF section.

4.6 Wide-Band Data Demodulator

The wide-band data demodulator (WBDD) module demodulates the FM signal and outputs a Manchester-decoded data stream. The WBDD is used for receiving the analog control channels of the forward control channel (FOCC) and the forward voice channel (FVC). The bit error rate (BER) performance requirements are listed in Table 4–8.

Table 4–8. Typical Bit-Error-Rate Performance (WBD_BW = 000)

PARAMETER	TEST CONDITIONS MEAN CNR	MIN MAX	UNIT
Bit error rate	–5	0.4	dB
	0	0.279	
	5	0.143	
	10	0.056	
	15	0.0192	
	20	0.00623	
	25	0.00199	

The WBDD is controlled by the bits in the control register WBDCtrl (see Table 4–9).

Table 4–9. Bits in Control Register WBDCtrl

NAME	BIT CODE	FUNCTION
WBD_LCKD	—	Indicates whether edge detector is locked (1) or unlocked (0)
WBD_ON	—	Turns the WBDD module on/off (1/0)
WBD_BW		Sets the appropriate PLL bandwidth
	000	20 Hz
	001	39 Hz
	010	78 Hz
	011	156 Hz
	100	313 Hz
	101	625 Hz
	110	1250 Hz

WBD_LCKD: This bit reduces the effects of signal dropouts due to fading. In the Manchester-coded signal, there are two types of data edges. One type occurs at the midpoint of each data bit, and the other occurs randomly, depending on the transmitted data sequence. Inside the WBDD, an edge detector rapidly synchronizes itself to the midpoint edges when the WBD_LCKD bit clears to 0. However, when a signal dropout occurs, the edge detector may momentarily lock to the wrong edge because it cannot distinguish the midpoint edges from the data edges. A small number of additional bits may be lost in this instance.

When the WBD_LCKD bit is set to 1, the edge detector uses the WBDD internal phase lock loop (PLL) output to distinguish the correct edge. Once acquisition of data has occurred, when this bit is set to 1, the loss of bits due to signal dropouts is restricted to the fade duration only.

When the WBDD PLL is not synchronized, as at power up, the WBD_LCKD bit must be cleared to 0 to allow edge synchronization to the data.

WBD_BW: The variable bandwidth is required for fast acquisition in the beginning using a wide bandwidth for the PLL, and a narrower bandwidth is used afterwards to reduce the likelihood of noise causing loss of synchronization.

The WBDCtrl register is accessible by both the DSP and the microcontroller.

4.7 Wide-band Data Interrupts

The WBDD operates whenever WBD_ON is high, and it does not require the receive channels to be enabled. While WBD_ON is high, every 800 μs, 8 bits are placed in the WBD register, which is accessible by both the DSP and the microcontroller ports. This value should be written at the same time as WBD_ON is initially set high.

At the same time, the interrupts DWBDINT and MWBDFINT are asserted. The interrupt rate is 800 μs (8 bits/10 kHz). These interrupts are individually cleared when the WBD register is read by the corresponding processor. They can also be cleared by their respective processor by writing a 1 to the corresponding clear WBD bit.

There is one WBD control register. It can be written to by either processor port.

4.8 Wide-band Data Demodulator General Information

The WBDD recovers the transmitter clock from the data stream, which is Manchester encoded, and decodes the data bits. Consideration at the system level is required to ensure data integrity.

The WBD stream carries with it a 10-kHz clock. The Manchester-coded data format contains a transition at the middle of every bit-clock period, which aids in clock recovery. The polarity of the transition is data-dependent. In a typical Manchester-coded WBD stream, a positive voltage for the first half of the data sequence bit time followed by a negative voltage for the second half of the data sequence bit time represents the value 0 in the data sequence. Likewise, a negative voltage followed by a transition to a positive voltage represents the value 1 in the data sequence. This is illustrated in Figure 4–4. The WBD stream can also be seen as the exclusive-OR of the clock and data sequence. The data sequence is in nonreturn to zero (NRZ) format.

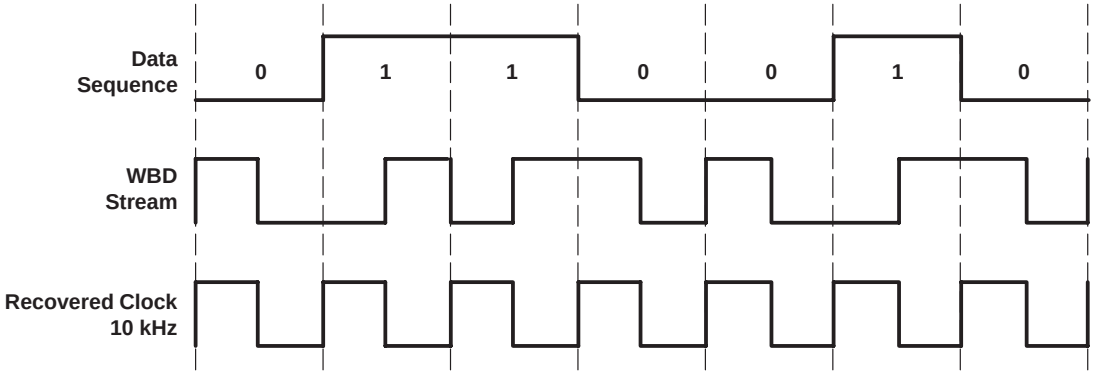


Figure 4–4. WBD Manchester-Coded Data Stream

4.9 Auxiliary DACs, LCD Contrast Converter

Auxiliary DACs generate AFC, AGC and power control signals for the RF system. These three D/A converters are updated when the corresponding data is received from the DSP. In fewer than 5 µs after the corresponding registers are written to, the output has settled to within 1 LSB of its new value (see Table 4–10).

Table 4–10. Auxiliary D/A Converters

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output range	AV_{DD} > 3 V†, AUXFS [1:0] = 00	0.2		2.5	V
	AV_{DD} > 4.5 V†, AUXFS [1:0] = 10	0.2		4	
	AV_{DD} > 5 V†, AUXFS [1:0] = 11	0.2		4.5	
Resolution AGC, AFC, PWRCONT DACs			8		bits
Resolution LCDCONTR DAC			4		bits
Gain + offset error (full scale) AGC, AFC, PWRCONT DAC				±3%	
Gain + offset error (full scale) LCDCONTR DAC				±7%	
Differential nonlinearity			±0.75	±1	LSB
Integral nonlinearity			±0.75	±1	LSB

† Range settings depends only on AUXFS [1:0]. The supply voltage is not detected.

The LCDCONTR output is used by the microcontroller to adjust the contrast of the LCD. This converter is a separate 4-bit DAC.

The auxiliary DACs can be powered down. The AGC and AFC DACs have dedicated bits in the MIntCtrl register to enable the DACs. The PWRCONT DAC is enabled by the TXEN bit in the DStatCtrl register. The LCDCONTR DAC is enabled when the LCDEN bit of the LCD D/A register clears to 0, the four data bits being left justified. The AFC, AGC, and PWRCONT DACs are disabled after powerup or after a reset of the TCM4300. After power up or reset, the default AUXFS[1:0] is 00. When the DACs are powered down, their output terminals go to a high-impedance state and can tolerate any voltage present on the terminal that falls within the supply range.

The slope and the corresponding output values for the auxiliary DACs are listed in Table 4–11 and Table 4–12.

Table 4–11. Auxiliary D/A Converters Slope (AGC, AFC, PWRCONT)

AUXFS[1:0] SETTING	SLOPE	NOMINAL LSB VALUE (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 128 (MIDRANGE) (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 256† (MAX VALUE) (V)
00	2.5/256	0.0098	1.25	2.5
01	Do not use	Do not use	Do not use	Do not use
10	4/256	0.0156	2	4
11	4.5/256	0.0176	2.25	4.5

† The maximum input code is 255. The value shown for 256 is extrapolated.

4.9 Auxiliary DACs, LCD Contrast Converter (continued)

Table 4–12. Auxiliary D/A Converters Slope (LCDCONTR)

AUXFS[1:0] SETTING	SLOPE	NOMINAL LSB VALUE (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 8 (MIDRANGE) (V)	NOMINAL OUTPUT VOLTAGE FOR DIGITAL CODE = 16† (MAX VALUE) (V)
00	2.5/16	0.1563	1.25	2.5
01	Do not use	Do not use	Do not use	Do not use
10	4/16	0.2500	2	4
11	4.5/16	0.2813	2.25	4.5

† The maximum input code is 15. The value shown for 16 is extrapolated.

4.10 RSSI, Battery Monitor

The RSSI and battery (BAT) strength monitor share a common register. The input source is determined by writing any value to the mapped register location for that ADC (see Table 4–13), and the result of the conversion is stored in both register locations. The conversion process is initiated when the register is written to. The CVRDY bit in the MStatCtrl register is set to 1 to show completion of the conversion process. Reading from either of the register locations causes the CVRDY bit to change to 0. The RSSI allows the mobile unit to choose the proper control channels and to report signal levels to the base stations.

When the CVRDY bit in the MStatCtrl register goes to 1, this indicates that the latest RSSI or battery voltage A/D conversion has been completed and can be read from the RSSI or BAT register location. CVRDY clears to 0 when the microcontroller reads either of these locations.

Table 4–13. RSSI/Battery A/D Converter

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input range	AV_{DD} = 3 V, 4.5 V, 5 V	0.2		2	V
Resolution			8		bits
Conversion time	AV_{DD} = 3 V, 4.5 V, 5 V		20		μs
Gain + offset error (full scale)			±3%	±4%	
Differential nonlinearity			±0.75	±1	LSB
Integral nonlinearity			±0.75	±1	LSB
Input resistance		1	2		MΩ

In order to save power, the entire RSSI/battery converter circuit is powered down when no A/D conversions are requested for 40 μs. The microcontroller writes to RSSI or BAT registers, causing power to be applied to the converter circuit. Power is applied to the converter circuit until the data value has been latched into the corresponding register, at which time power to the converter is removed. Data remains in the result registers after the converter is powered down.

4.11 Timing And Clock Generation

The digital timing generation system uses a 38.88-MHz master clock as shown in Figure 4–5. The upper waveform shows the clock generation for clocks that must be phase adjusted in order to synchronize the mobile unit with the received symbol stream in the digital mode. In the analog mode, these clocks operate without phase adjustments. The bottom waveform of Figure 4–5 shows the clocks that are directly derived from the master clock.

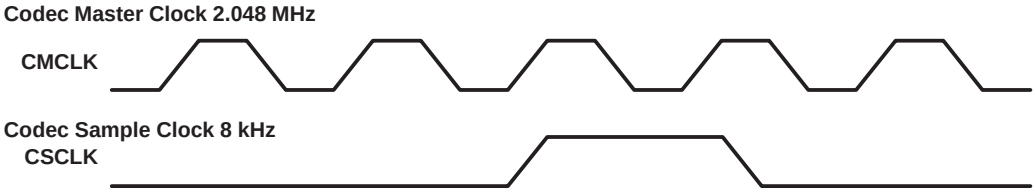


Figure 4–5. Codec Master and Sample Clock Timing

4.11.1 Clock Generation

There are three options for generating the master clock. A fundamental crystal or a third-overtone crystal with a frequency of 38.88 MHz can be connected between the MCLKIN and the XTAL terminals or an external clock source can be connected directly to the MCLKIN terminal. The MCLKOUT is a buffered master clock output at the same frequency as MCLKIN. MCLKOUT can be used as the source clock for other devices in the system. Setting the MCLKEN bit in the MStatCtrl register enables or disables this output. The MCLKOUT enable is synchronous with MCLKIN to eliminate abnormal cycles of the clock output.

All output clocks are derived from the master clock (MCLKIN). The sample clocks for the digital and analog modes, the 8-kHz speech codec sample clock, and the clocks for the A/D and D/A functions are also derived from the master clock.

4.11.2 Speech-Codec Clock Generation

The TCM4300 generates two clock outputs for use with speech codecs: the 2.048-MHz CMCLK and the 8-kHz CSCLK. These clocks are generated so that each CSCLK period contains exactly 256 cycles of CMCLK. Since 2.048 MHz is not an integer division of the 38.88-MHz MCLKIN, one out of every 64 CMCLK cycles is 18 MCLKIN periods long, and the remaining 63 out of 64 are 19 MCLKIN periods long. The average frequency of MCLKIN is therefore

$$\text{MCLKIN} \times \frac{\left(\frac{63}{19} + \frac{1}{18}\right)}{64} = 2.048092 \text{ MHz}$$

CSCLK is exactly CMCLK divided by 256 (see Figure 4–5).

To save power, the codec clocks are only generated by TCM4300 when the SCEN bit of the DStatCtrl register is set high. When SCEN is low, both outputs, CSCLK and CMCLK, are held low. SCEN is also available as an output.

4.11.3 Microcontroller Clock

A variable modulus divider provides a selection of frequencies for use as a microcontroller clock. The master clock is divided by an integer from 32 to 2, giving a wide range of frequencies available to the microcontroller (1.215 MHz to 19.88 MHz). The modulus can be changed by writing to the microcontroller clock register. The output duty cycle is within the requirements of most microcontrollers, that is, from 40% to 60%. At power-on reset, the clock divider defaults to 1.215 MHz.

4.11.4 Sample Interrupt SINT

The SINT interrupt signal is the primary timing signal for the TCM4300 interface. The primary function of the SINT is to indicate the ready condition to receive or transmit data. It also conveys timing marks to allow for the synchronization of system DSP functions. In the digital mode, SINT is used in conjunction with the received sync word to track cellular system timing. The SINT can be disabled by writing a 1 to the SDIS bit of the DIntCtrl register. When enabled, the SINT operates continuously at 48.6 kHz in the digital mode and at 40 kHz in the analog mode. The SINT signal does not require an interrupt acknowledge. The SINT is active low for 5.5 MCLK cycles (141.5 ns) in the analog mode and 6.5 MCLK cycles (167.2 ns) in the digital mode.

4.11.5 Phase-Adjustment Strategy

For an IS-54 system in the digital mode, receiver sample timing must be phase adjusted to synchronize the A/D conversions to optimum sampling points of the received symbols, and to synchronize the mobile unit timing to the base station timing. This is done by temporarily increasing or decreasing the periods of the clocks to be adjusted. To avoid undesirable transients, each cycle of the clock being adjusted is altered by only one period of MCLKIN. A total adjustment equivalent to multiple MCLKIN periods is accomplished by altering multiple cycles of the clock being adjusted. The number of cycles altered is controlled by internal counters.

In the TCM4300 there are two clocks which must be adjusted: CMCLK and an internal 9.72-MHz clock from which SINT is derived. Each of these clocks has an associated counter that counts the number of cycles that have been lengthened or shortened by one MCLKIN period each and thus detects when the total adjustment is complete. These counters are shown in Figure 4–6 as Adjust Counter A and Adjust Counter B.

The magnitude of the 2s complement value written to the timing adjustment register determines the number of cycles of the clocks to be lengthened or shortened by one MCLKIN period each to achieve the total desired timing adjustment in units of MCLKIN periods. If a negative number is written, the clock periods are lengthened for the duration of the timing adjustment, resulting in a timing delay. If a positive number is written, the clock periods are shortened for the duration of the timing adjustment, resulting in a timing advance.

The divider generates CMCLK normally divides MCLKIN by either 19 or 18. When the CMCLK period is being lengthened during a timing adjustment, MCLKIN is divided by either 20 or 19. When the CMCLK period is being shortened, MCLKIN is divided by either 18 or 17 (see *subsection 4.11.2*). The divider used to generate a 9.72-MHz clock divides by 4 during normal operation, by 5 when its period is being lengthened during timing adjustments, and by 3 when its period is being shortened during timing adjustments.

Because CMCLK and the 9.72-MHz internal clock have different periods, and the timing adjustments are limited to one period of MCLKIN per period of the clock, these clocks take different times to complete the entire timing adjustment. Because the total adjustment is the same number of MCLKIN periods for both clocks, the relative phases of the two clocks are the same after the adjustment as they were before.

Both adjust counters reach zero when the adjustment is complete, so there is no need to write to the timing adjustment register until another timing adjustment is required. For each write to the timing adjustment register, a single timing adjustment of the direction and magnitude requested is performed.

The output of each adjustment counter is fed to a variable modulus divider. For counter A, there are three possible moduli, 3, 4, and 5. For counter B there are four possible moduli, 17, 18, 19, and 20.

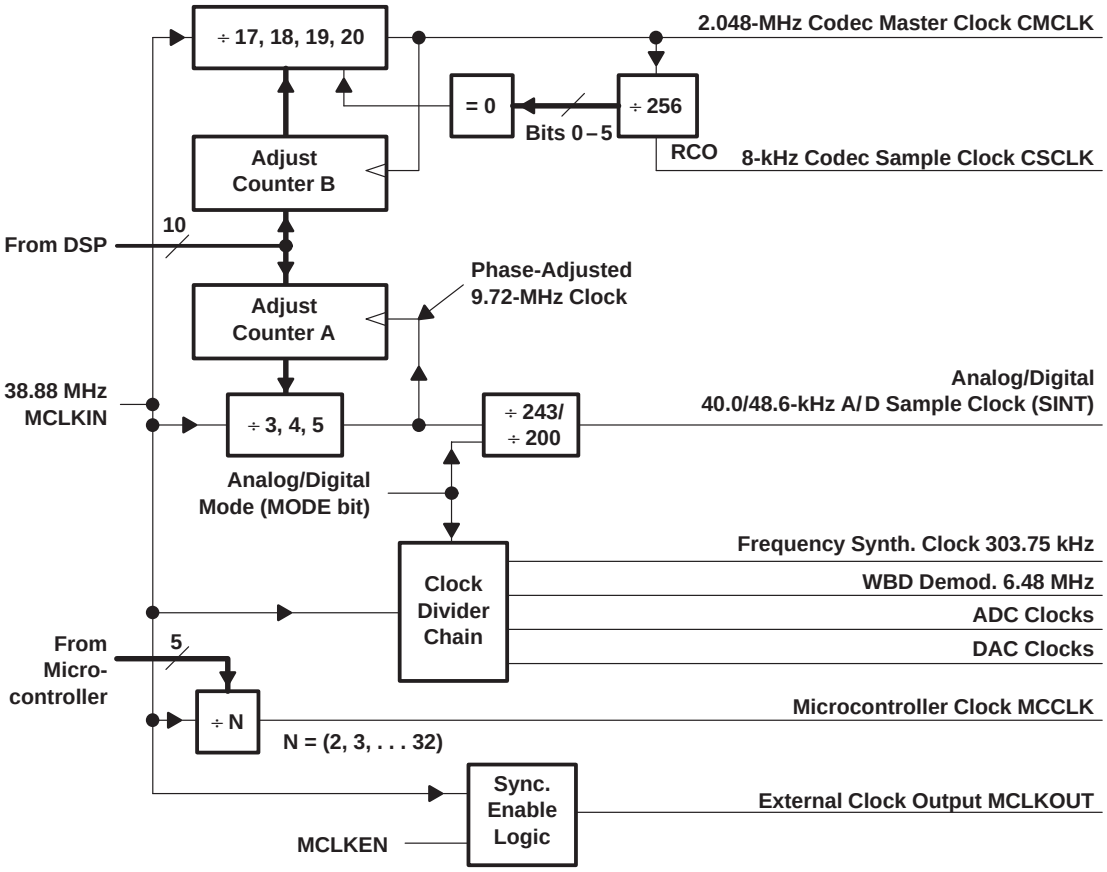


Figure 4–6. Timing and Clock Generation for 38.88-MHz Clock

4.12 Frequency Synthesizer Interface

The synthesizer interface provides a means of programming three synthesizers. The synthesizer-side outputs are a data line, a clock line, and three latch enable lines that separately strobe data into each synthesizer. The control inputs are registers mapped into the microcontroller address space. The status of the interface can be monitored to determine when the programming operation has been completed.

The synthesizer interface is designed to be general purpose. Most of the currently available synthesizers can be accommodated by programming the interface according to the required synthesizer data and logic level formats.

The output of the synthesizer interface consists of five signals. SYNCLK is the common data clock for all attached synthesizer chips. The clock rate is MCLK/128 (≈304 kHz). The clock pulse has a 50% duty factor. The serial data output SYNDTA is common to all synthesizers. Three strobe signals, SYNLE0, SYNLE1, and SYNLE2, are provided. There is one for each synthesizer chip. The attributes of this interface are controlled by means of the synthesizer control registers, SynCtrl0, SynCtrl1, and SynCtrl2. These attributes determine:

- The polarity of the clock (rising or falling edge)
- Whether data is shifted left or right
- The number of bits sent to the synthesizer
- The timing and polarity of the latch enable bits
- The selection of which synthesizer to program

Programming of the synthesizers is accomplished by writing to four microcontroller-mapped data registers. These registers are chained to form a 32-bit data shift register that can be operated in either shift left or shift right mode. This register set can accommodate various formats of synthesizer control data. When fewer than 32 bits of data are to be transmitted, the significant data bits must be justified such that the first bit to be transferred is either the LSB or the MSB of the register set, as defined by the control register for LSB or MSB first operation. All 32 bits of the data register are transmitted each time (see Section 4.15 for register location and Figure 4–7 for a representative block diagram of the frequency synthesizer interface).

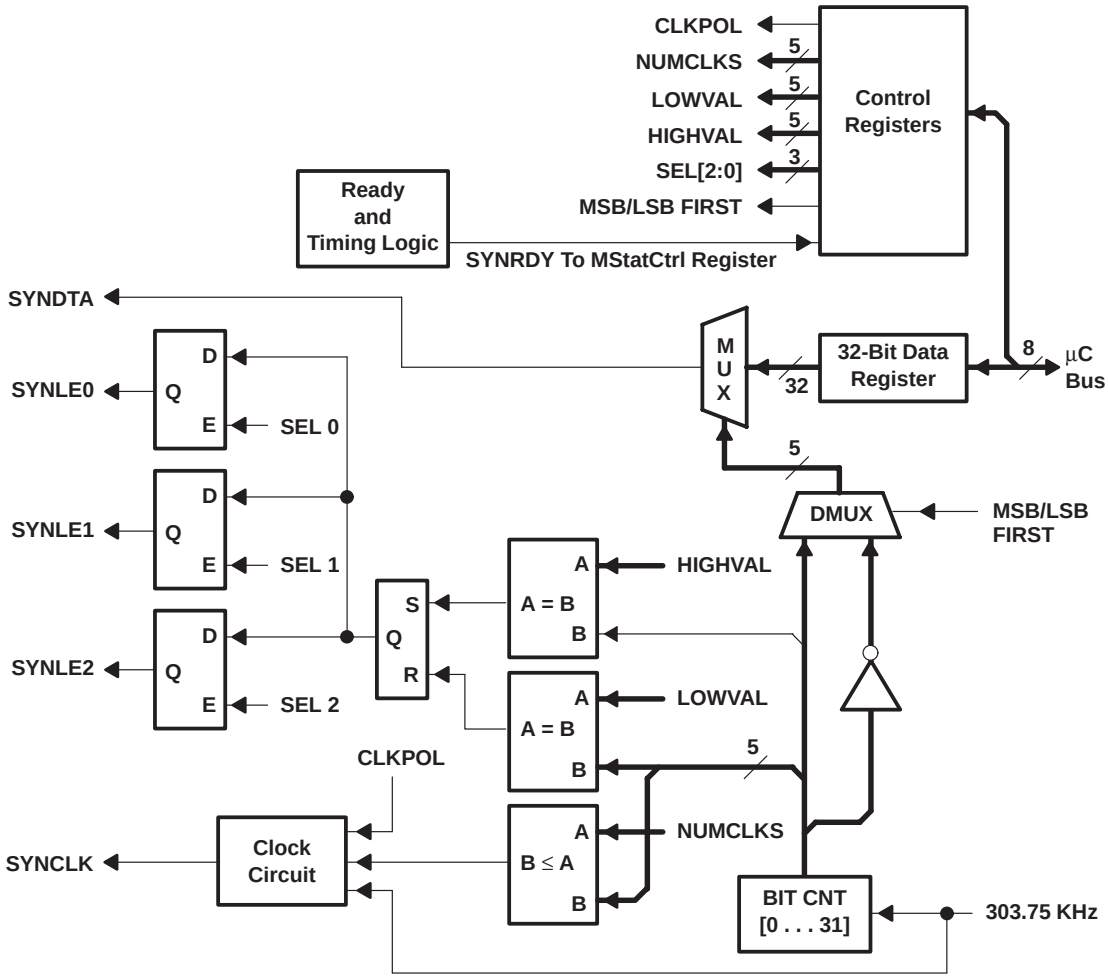


Figure 4–7. Synthesizer Interface Circuit Block Diagram

The SynData0 register contains the least significant bits of the 32-bit data register. SynData3 contains the most significant bits. The bits in the SynCtrl0, SynCtrl1, and SynCtrl2 registers are allocated as shown in Figure 4–8.

SynCtrl0	7–5	4–0
	SEL[2:0]	LOWVAL

SynCtrl1	7–6	5	4–0
	Reserved	MSB/LSB FIRST	HIGHVAL

SynCtrl2	7–6	5	4–0
	Reserved	CLKPOL	NUMCLKS

Figure 4–8. Contents of SynData Registers

Table 4–14 identifies the meaning of each of the bit fields in SynCtrl[2:0].

Table 4–14. Synthesizer Control Fields

NAME	DESCRIPTION
CLKPOL	This is a 1-bit field. When CLKPOL = 1, the SYNCLK signal is a positive-going, 50% duty cycle pulse. CLKPOL = 0 reverses the polarity of SYNCLK.
NUMCLKS	This 5-bit field defines the total number of clock pulses that are to be produced on SYNCLK. The value written into NUMCLKS is the desired number of output clock pulses, with one exception: When 32 clock pulses are desired, all zeroes are written into NUMCLKS.
HIGHVAL	This 5-bit field defines when the strobe signal for the selected synthesizer is driven high. HIGHVAL is the bit number at which the signal changes state. Bits being transferred on SYNDTA are sequentially designated 0, 1, . . . 31, independent of any MSB/LSB selection.
LOWVAL	The value written into this 5-bit field affects the strobe signal for the selected synthesizer. LOWVAL is the bit number at which the strobe signal is driven low. The first bit transferred out of the serial interface is defined to occur at bit-time 0, independent of any MSB/LSB selection.
MSB/LSB FIRST	Writing a 0 to MSB/LSB FIRST causes the LSB (SynData0[0]) to be the first bit sent to SYNDTA of the serial synthesizer interface. Writing a 1 to this bit programs the block for MSB first operation, SynData3[7].
SEL[2:0]	This is a 3 bit field that selects which synthesizer strobe line is active. A 1 in any of the SELx bits activates the corresponding latch enable.

In the status register MStatCtrl, two bits, SYNOL and SYNRDY, are dedicated to the synthesizers. The first is an out-of-lock indicator that comes from the SYNOL input terminal. When the SYNOL input terminal is connected to the OR of the out-of-lock signals from the external synthesizers, the lock condition of the synthesizers can be monitored by reading the MStatCtrl register. A high on SYNOL also prevents the PAEN output from being asserted and forces the TXI and TXQ outputs to zero. The SYNRDY bit, active high, indicates when the synthesizer interface is idle and ready for programming. When SYNRDY is low, the synthesizer interface is busy.

Controlling the synthesizer interface is straightforward. The microcontroller checks to see if the SYNRDY bit is low. When it is low, the synthesizer interface is not ready. When SYNRDY goes high, the microcontroller programs the desired information into the four registers. When the microcontroller write to the SynCtrl2 register is complete, the synthesizer interface sets the SYNRDY bit low and begins to send data, clock, and latch enable according to the format established in the registers. SYNRDY returns high when the entire operation is complete.

Up to 31 data bits plus a latch enable (SYNLE0,1,2) can be programmed in one programming cycle. When data greater than or equal to 32 bits must be programmed, TI recommends using two or more programming cycles with data in each cycle and a latch enable in the final programming cycle. Two or more programming cycles are recommended because all programming cycles must contain at least one SYNCLK pulse, whereas the latch enable can be suppressed in any programming cycle.

Figure 4–9 shows an example of the synthesizer output signals. In this case, an 18-bit pattern, 0x10664, was chosen to write into synthesizer 1 with a positive-going latch enable pulse at the eighteenth bit. In order to do so, the microcontroller writes the values 00h into SynData0, 00h into SynData1, 99h into SynData2, 41h into SynData3, 52h into SynCtrl0, 31h into SynCtrl1, and 32h into SynCtrl2.

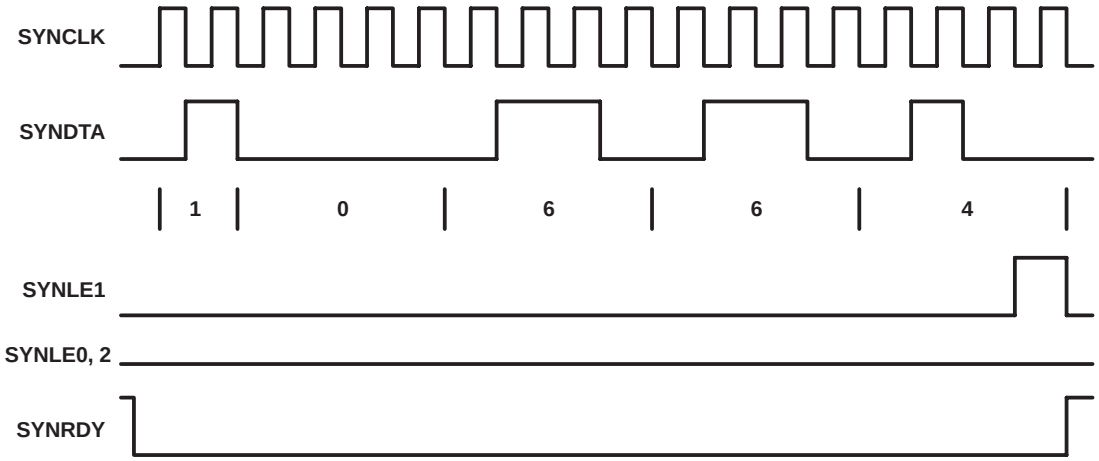


Figure 4–9. Example Synthesizer Output

4.13 Power Control Port

For systems requiring minimum system current consumption, power can be provided to each functional part of the TCM4300 only when that function is required for proper system operation. To accomplish this, the TCM4300 provides six external power control signals accessible through the DStatCtrl and MStatCtrl registers. These signals can be used to minimize the on time of the functional units. These power control signals are SCEN, FMRXEN, IQRXEN, TXEN, PAEN, and OUT1 (see Table 4–15). The polarity of each of these signals is high enable, low disable.

Table 4-15. External Power Control Signals

NAME	SUGGESTED EXTERNAL APPLICATION	RESET VALUE
SCEN	Speech codec (microphone/speaker interface circuit) enable	0
FMRXEN	FM demodulator enable	0
IQRXEN	I and Q receive enable. IQRXEN enables the QPSK demodulator and the AGC amplifier	0
TXEN	Transmit enable. TXEN enables power to the transmitter signal processing circuits: QPSK modulator, voltage-controlled amplifier, driver amplifier, PA negative bias. This signal can be used to enable these subsystems only during the transmit burst in digital mode.	0
OUT1	User defined	0
PAEN	Power amplifier enable. PAEN enables power to PA.	0

In addition to allowing control of power to external functional modules, these power control bits combined with other control bits are used to control internal TCM4300 functions. This control system is shown in Figure 4–10.

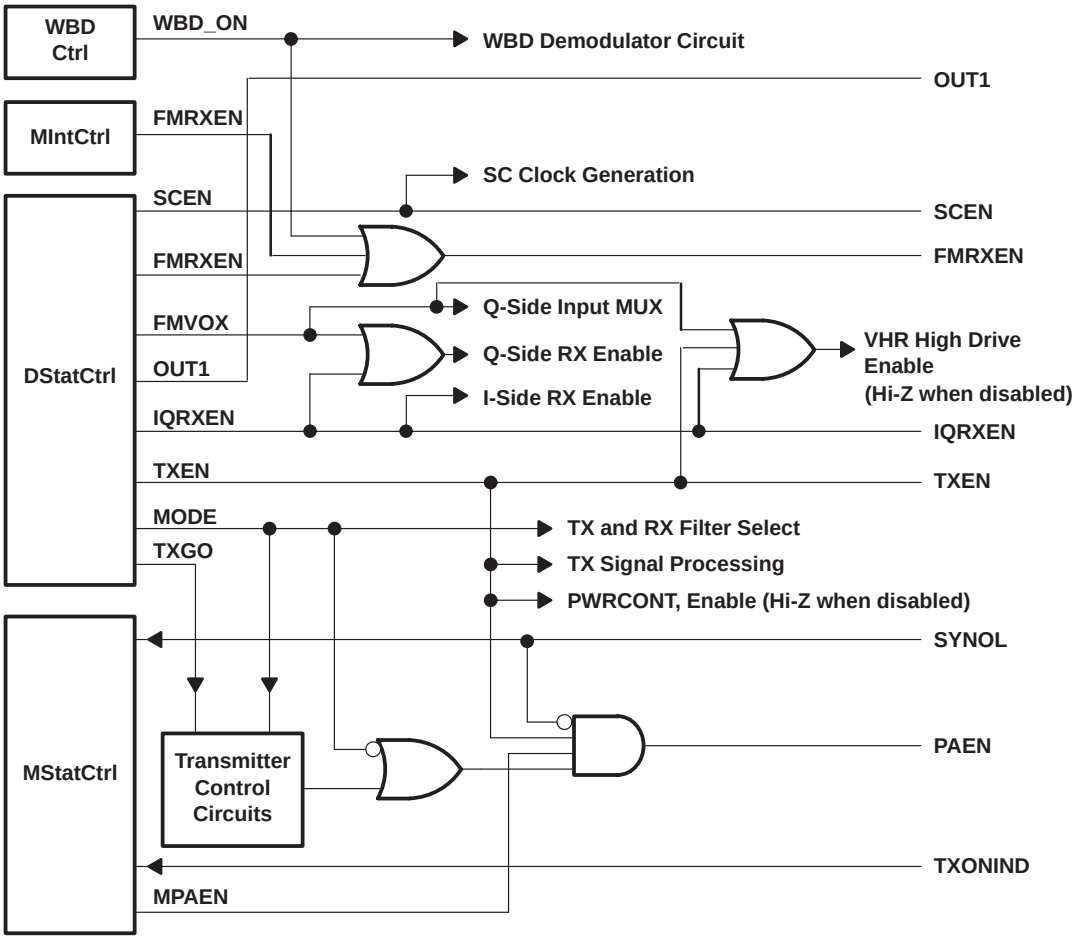


Figure 4–10. Internal and External Power Control Logic

To allow for further system power savings, the TCM4300 receive I and Q channels are enabled separately because only the Q side is used in analog mode. The FMVOX bit controls the Q-side input multiplexer. When FMVOX is high, the QP side of the receiver is connected to the FM input terminal, the QN input is connected to the VHR reference voltage, and the Q side of the receiver is powered up. The MODE bit controls the Q-side filter characteristics for digital or analog mode. The IQRXEN bit enables both the I and Q receiver sides. The bit IQRXEN can be set high while still in analog mode (FMVOX high or MODE low) to allow sufficient power-up settling time for the external receiver I and Q circuits.

Setting the MODE bit low connects RXQP to the FM input and RXQN to VHR.

In the digital mode (MODE bit set high), setting IQRXEN high turns on both sides of the receiver. The TXEN enables the internal transmit functions. When the TXEN bit is set low, the PWRCONT output goes to a high-impedance state and the PAEN output is set low. The TXEN signal can be used to power down most of the external transmit circuits between transmit bursts.

In the analog mode, (MODE bit set low), PAEN is high whenever TXEN is active and SYNOL is low. The SYNOL input can be used as an indication to the TCM4300 that the external synthesizers are out of lock. The PAEN signal is gated by SYNOL to prevent off-channel transmissions.

The TXEN, IQRXEN, FMVOX, and MODE signals are generated by sampling the corresponding bits of the DStatCtrl register with the internal SINT. The effect of a write to the DStatCtrl register on these signals does not appear until the next SINT after the write.

4.14 Microcontroller-DSP Communications

The microcontroller and the DSP communicate by means of two separate 32-byte first-in first-out (FIFO) buffers. Figure 4–11 illustrates this scheme. The microcontroller writes to FIFO A, but data read from the same address comes from FIFO B. On the DSP side, the situation is reversed.

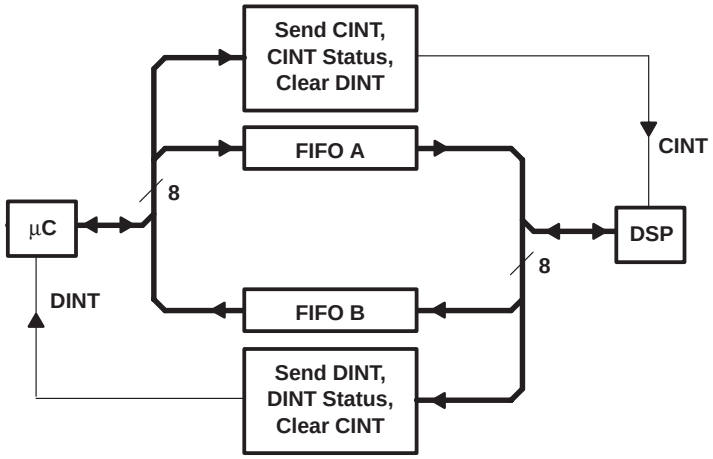


Figure 4–11. Microcontroller-DSP Data Buffers

To send data to the DSP, the microcontroller writes data to FIFO A. To indicate to the DSP that FIFO A is ready to be read, the microcontroller writes a 1 to the Send-C bit of the microcontroller interrupt control register MIntCtrl. When this happens, the DSP interrupt line CINT goes active, signaling to the DSP that data is waiting. At the same time, the value that can be read from the Clear-C bit in the DIntCtrl register goes from 0 to 1, indicating that the interrupt is pending. When the DSP writes a 1 to the Clear-C bit, the CINT line returns to the inactive state and the value that can be read from Clear-C is 0. The microcontroller cannot deassert the CINT line.

The microcontroller-DSP communications interface is symmetric. Data sent from the DSP to the microcontroller is handled as described above, with the roles of A and B FIFOs and C and D bits and interrupts reversed. When the number of reads exceeds the number of writes from the other side, the values read are undefined.

4.15 Microcontroller Register Map

The microcontroller can access 17 locations within the TCM4300. The register locations are 8 bits wide as shown in Table 4–16 and Table 4–17.

Table 4–16. Microcontroller Register Map

ADDR	NAME	D7	D6	D5	D4	D3	D2	D1	D0
00h	WBDCtrl	WBD_LCKD	WBD_ON	WBD_BW			Reserved		
00h	WBD	MSB							LSB
01h	FIFO	MSB	FIFO A(B) Microcontroller to DSP (DSP to microcontroller)						LSB
02h	MIntCtrl	Clear WBD	Clear-F	Clear-D	Send-C	AGCEN	AFCEN	FMRXEN	Reserved
03h	SynData0	MSB							LSB
04h	SynData1	MSB							LSB
05h	SynData2	MSB							LSB
06h	SynData3	MSB							LSB
07h	SynCtrl0	SEL[2:0]			LOWVAL				
08h	SynCtrl1	Reserved		MSB/LSB FIRST	HIGHVAL				
09h	SynCtrl2	Reserved		CLKPOL	NUMCLKS				
0Ah	MCClock	Reserved		MSB					LSB
0Bh	RSSI A/D	MSB							LSB
0Ch	BAT A/D	MSB							LSB
0Dh	LCD D/A	MSB			LSD	Reserved			LCDEN
0Eh	MStatCtrl	SYNOL	TXONIND	SYNRDY	MCLKEN	CVRDY	AuxFS1	AuxFS0	MPAEN
0Fh	TXI Offset	Reserved		Sign	MSB				LSB
10h	TXQ Offset	Reserved		Sign	MSB				LSB

Table 4–17. Microcontroller Register Definitions

ADDR	NAME	CATEGORY	R/W
00h	WBDCtrl	Wide-band data	W
00h	WBD		R
01h	FIFO	FIFO A(B) microcontroller to DSP (DSP to microcontroller)	W/(R)
02h	MIntCtrl	Interrupt/control status	R/W
03h	SynData0	Synthesizer interface	W
04h	SynData1		W
05h	SynData2		W
06h	SynData3		W
07h	SynCtrl0		W
08h	SynCtrl1		W
09h	SynCtrl2		W
0Ah	MCClock	Microcontroller clock speed	W
0Bh	RSSI A/D	RSSI level	R
0Ch	BAT A/D	Battery level monitor	R
0Dh	LCD D/A	LCD contrast control	W
0Eh	MStatCtrl	Miscellaneous status/control	R/W
0Fh	TXI Offset	Transmit dc offset compensation	W
10h	TXQ Offset		W

4.16 Wide-Band Data/Control Register

This register is used for two functions, depending on whether it is being read from or written to. When read from, the register provides the latest 8 bits of received and demodulated data according to the microcontroller register map to the microcontroller. When it is written to, the bits are placed into the WBDCtrl register (see Table 4–16) as shown here:

	7	6	5–3	2–0
WBDCtrl	WBD_LCKD	WBD_ON	WBD_BW[2:0]	Reserved
	W	W	W	

When the WBDCtrl register is read, bit 7 (MSB) is the last received data bit.

The definition of the WBDCtrl register, according to the DSP register map, is shown in Table 4–18.

Table 4–18. WBDCtrl Register

BIT	R/W	NAME	FUNCTION	RESET VALUE
9	R/W	WBD_LCKD	Wide-band data lock data. WBD_LCKD determines whether edge detector is locked (1) or unlocked (0).	0
8	R/W	WBD_ON	Wide-band data on. WBD_ON turns the WBDD module on/off (1/0).	0
7–5	R/W	WBD_BW[2:0]	Wide-band data bandwidth. WBD_BW[2:0] sets the appropriate PLL bandwidth. 000 : 20 Hz 001 : 39 Hz 010 : 78 Hz 011 : 156 Hz 100 : 313 Hz 101 : 625 Hz 110 : 1250 Hz	110
4–0	—	—	Reserved	—

4.17 Microcontroller Status and Control Registers

MCClock: This location is used by the microcontroller to change the speed of its own clock. The division modulus is equal to a binary coded value written into this register. Only bits [5:0] are significant. After reset, MCClock is equal to MCLKIN/32. Division moduli 2 through 32 are valid (0-1 moduli are prohibited). The clock speed change occurs after the write is complete.

MIntCtrl Bits [7:4]: The bit names in this field indicate the resulting action when the bit is set to 1. When these bits are being read, a 1 indicates that the corresponding interrupt is pending. A 0 indicates that the interrupt is clear. Writing a 0 into any bit location has no effect.

MIntCtrl Bits [3:1]: These bits enable power to the AGC and AFC DACs and their corresponding outputs as shown below. FMRXEN can assert (set to 1) the FMRXEN external function. The reset value is 0 (off).

	7	6	5	4	3	2	1	0
MIntCtrl	Clear WBD	Clear-F	Clear-D	Send-C	AGCEN	AFCEN	FMRXEN	Reserved
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

MStatCtrl: This register contains various signals needed for system monitoring and control as shown here (also see Table 4–19).

	7	6	5	4	3	2	1	0
MStatCtrl	SYNOL	TXONIND	SYNRDY	MCLKEN	CVRDY	AuxFS1	AuxFS0	MPAEN
	R	R	R	R/W	R	R/W	R/W	R/W

Table 4–19. MStatCtrl Register Bits

BIT	R/W	NAME	FUNCTION	RESET VALUE
7	R	SYNOL	Synthesizer out of lock. SYNOL is equal to the level applied to SYNOL input pin. SYNOL can be used as an input for an externally generated status signal to prevent transmission when external synthesizers are out of lock. In digital mode, when SYNOL is high, PAEN is not asserted and no signal can be transmitted from TXIP, TXIN, TXQP, and TXQN.	Level on SYNOL input terminals
6	R	TXONIND	Transmitter on indicator. TXONIND is equal to the level applied to TXONIND, and it can indicate that power is applied to the power amplifier.	Level for TXONIND input terminals
5	R	SYNRDY	Synthesizer interface ready. SYNRDY indicates that frequency synthesizer is ready to be programmed by the microcontroller. When SYNRDY is 1, the microcontroller can program the frequency synthesizer interface; a 0 indicates the interface circuit is busy.	1
4	R/W	MCLKEN	MCLKOUT enable. When MCLKEN is set to 1 by the microcontroller, the 38.88-MHz master clock is output at MCLKOUT. Writing 0 to MCLKEN disables MCLKOUT.	1
3	R	CVRDY	Conversion ready. A 1 indicates that the latest RSSI or battery voltage A/D conversion is complete and can be read from the RSSI or battery register location. CVRDY goes to 0 when the microcontroller reads from either of these locations.	1
2	R/W	AuxFS[1]	Auxiliary DACs full-scale select. The auxiliary DACs are AGC, AFC, PWRCONT and also LCD CONTR DAC. The microcontroller selects the full-scale output ranges with these bits (see Table 4–11 and Table 4–12 for bit-to-output range mapping).	0
1		AuxFS[0]		0
0	R/W	MPAEN	Microcontroller PA enable. A 0 indicates that the external PA enable line PAEN is prevented from going active (see Figure 4–9).	0

TXI Offset and TXQ Offset: These registers allow the differential offset voltages TXIP – TXIN and TXQP – TXQN to be adjusted to compensate for internal and/or external offsets. The magnitude of adjustment is D × step size, where D is a 6-bit, 2s-complement integer written into bits 5–0 of these registers, as shown here:

	7–6	5–0
TXI(Q) Offset	Reserved	TXI(Q) Offset Value
		W

4.18 LCD Contrast

The LCD contrast register allows for 16 levels of control of terminal LCD contrast. The register is input to the LCD contrast D/A converter allowing control of the level of intensity of the LCD display as shown here:

	7–4	3–1	0
LDC D/A	LCD Contrast	Reserved	LCDEN (active low)
	W		W

4.19 DSP Register Map

The register map accessible to the DSP port is shown in Table 4–20 and Table 4–21. There are 14 system addressable locations. Note that the write address of FIFO B is the same as the read address of FIFO A. Figure 4-12 details the connection of TCM4300 to an example DSP.

Table 4–20. DSP Register Map

ADDR	NAME	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	WBD	MSB							LSB	Reserved	
01h	WBDCtrl	WBD_LCKD	WBD_ON	WBD_BW			Reserved				
02h	RXI	Sign	MSB								LSB
03h	RXQ	Sign	MSB								LSB
04h	TXI	Sign	MSB								LSB
05h	TXQ	Sign	MSB								LSB
06h	FIFO	MSB	FIFO A(B) microcontroller to DSP (DSP to microcontroller)						LSB	Reserved	
07h	DIntCtrl	Clear WBD	SDIS	Clear-C	Send-D	Send-F	Reserved				
08h	Timing Adj	MSB									LSB
09h	AGC DAC	MSB							LSB	Reserved	
0Ah	AFC DAC	MSB							LSB	Reserved	
0Bh	PWR DAC	MSB							LSB	Reserved	
0Ch	DStatCtrl	TXGO	MODE	SCEN	FMVOX	FMRXEN	IQRXEN	TXEN	OUT1	RXOF	ALB
0Dh	BST Offset	Reserved								MSB	LSB

Table 4–21. DSP Register Definitions

ADDR	NAME	CATEGORY	R/W
00h	WBD	Wide-band data	R
01h	WBDCtrl	Wide-band data control	R/W
02h	RXI	RX channel A/D results	R
03h	RXQ		
04h	TXI	Analog mode: TXI D/A data	W
		Digital mode: $\pi/4$ DQPSK modulator input data	
05h	TXQ	Analog mode: TXQ D/A data	W
		Digital mode: Not used	
06h	FIFO	FIFO A(B) microcontroller to DSP (DSP to microcontroller)	R/(W)
07h	DIntCtrl	Interrupt control/status	R/W
08h	Timing Adj	Symbol timing adjust	W
09h	AGC DAC	AGC	W
0Ah	AFC DAC	AFC	W
0Bh	PWR DAC	Power control	W
0Ch	DStatCtrl	Miscellaneous status/control	R/W
0Dh	BST Offset	TDM burst offset	W

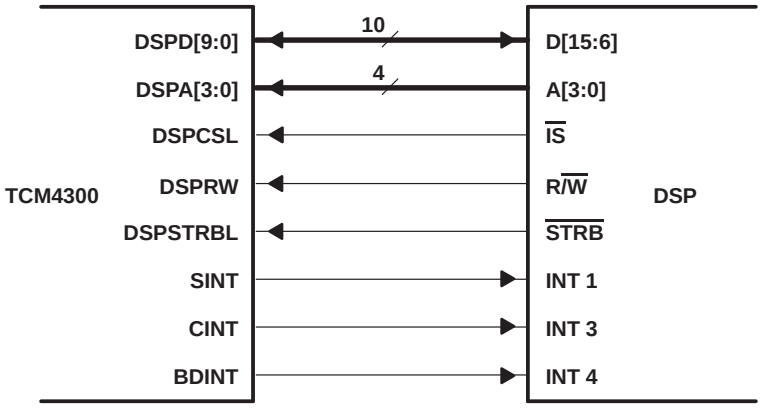


Figure 4–12. DSP Interface

4.20 Wide-Band Data Registers

Bit 9 of the wide-band data register is the most recently received bit as shown below.

WBD	9–2	1–0
	WB Data	Reserved
	R	

WBDCtrl	9	8	7–5	4–0
	WBD_LCKD	WBD_ON	WBD_BW	Reserved
	R/W			

4.21 Base Station Offset Register

BST OFFSET values are 00, 01, 10, and 11, which correspond to an offset value d of 0, 1, 2, and 3 respectively as shown below.

BST OFFSET	9–2	1–0
	Reserved	Offset[1:0]
		W

The delay in the TCM4300 TX channels is increased by the amount:

$$\text{BST OFFSET} = d \times \frac{T_{SINT}}{4}$$

4.22 DSP Status and Control Registers

DIntCtrl, Clear and Send Bits: The bit names in the DIntCtrl register indicate the action to be taken when a 1 is written to the respective bit. When these bits are being read, a 1 indicates that the corresponding interrupt is pending. A 0 indicates that the interrupt is not pending. Writing a 0 to any bit has no effect. Writing a 1 to the clear bits clears the corresponding interrupt, and the interrupt terminal returns to its inactive level. Writing a 1 to the send bits causes the corresponding interrupt to go active.

DIntCtrl, SDIS: When a 1 is written to the SDIS bit, the SINT interrupt going to the DSP is disabled. The disabling and re-enabling function is buffered to prevent the SINT signal from having shortened periods of output active. The SDIS bit is active (1) upon reset.

	9	8	7	6	5	4–0
DIntCtrl	Clear WBD	SDIS	Clear-C	Send-D	Send-F	Reserved
	R/W					

The DStatCtrl register contains various signals needed for system monitoring and control. These are described in Table 4–22.

	9	8	7	6	5	4	3	2	1	0
DStatCtrl	TXGO	MODE	SCEN	FMVOX	FMRXEN	IQRXEN	TXEN	OUT1	RXOF	ALB
	R/W									

Table 4–22. DStatCtrl Register Bits

BIT	R/W	NAME	FUNCTION	RESET VALUE
9	R/W	TXGO	Transmitter go. TXGO is used in digital mode to initiate (1) and terminate (0) a transmit burst.	0
8	R/W	MODE	Digital (1) – Analog (0) mode select. MODE affects the clock dividers and the transmitter modes of operation and the Q side filter.	0
7	R/W	SCEN	Speech codec enable (microphone/speaker interface chip). SCEN is connected to bits. SCEN also enables (1) or disables (0) the internal speech codec clock generation circuits (2.048 MHz – 8 kHz outputs).	0
6	R/W	FMVOX	FM voice enable. When FMVOX is 1 it enables the Q side of the internal receiver circuits and connects the receivers Q channel input to FM (see Figure 4–9).	0
5	R/W	FMRXEN	FM receiver enable. FMRXEN is connected to bit 5 (see Figure 4–9).	0
4	R/W	IQRXEN	I and Q receiver enable. The IQRXEN is connected to bit 4. When IQRXEN is 1, it enables (1) power to the I and Q sides of the internal receiver circuits, and when IQRXEN is 0, it disables (0) power to the I and Q sides of the internal receiver circuits (see Figure 4–9).	0
3	R/W	TXEN	Transmitter enable. TXEN is connected to bit 3. When TXEN is 1, it enables (1) power to the internal transmitter circuits and when TXEN is 0, it disables (0) power to the internal transmitter circuits (see Figure 4–9).	0
2	W	OUT1	Output 1. OUT1 is a user-defined general purpose data or control signal.	0
1	R/W	RXOF	Receive channel offset. When RXOF = 1, it disconnects the RXIP, RXIN, RXQP, and RXQN terminals from receive channel, and shorts internal RXIP to RXIN and RXQP to RXQN. It provides the capability of measuring the dc offset of the receive channel.	0
0	R/W	ALB	Analog loop-back. When ALB = 1, it disconnects the RXIP, RXIN, RXQP, and RXQN terminals from the internal receive channels and connects the corresponding internal signals to attenuated copies of the TXIP, TXIN, TXQP, and TXQN signals. The attenuation factor is 8.	0

4.23 Reset

A low on RSINL causes the TCM4300 internal registers to assume their reset values. The power-on reset circuit also causes internal reset. However, the logic level at RSINL has no effect on reset outputs RSOUTH and RSOUTL. The effects of resetting the TCM4300 are described in the following paragraphs.

4.23.1 Power-On Reset

The power-on reset (POR) is digitally implemented and provides a timed POR signal at RSOUTL and RSOUTH. The POR pulse duration is equal to 388,800 cycles of MCLKIN (10 ms). There are two outputs to provide a high reset and a low reset in order to accommodate the reset polarity requirements of any external device. The TCM4300 internal registers are reset when the POR outputs are activated. See Figure 4–13.

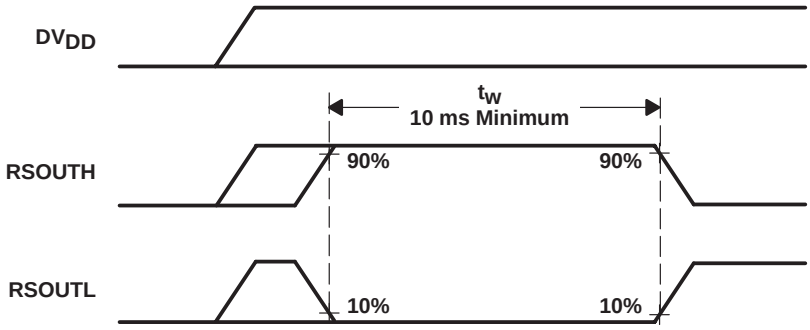


Figure 4–13. Power-On Reset Timing

4.23.2 Internal Reset State

After power-on reset, the TCM4300 register bits are initialized to the values shown in Table 4–23. The synthesizer control terminals SYNCLK, SYNLE0, SYNLE1, SYNLE2, and SYNDTA are high after reset, and the synthesizer interface circuit is in the stable idle state with no SYNCLK outputs.

Table 4–23. Power-On Reset Register Initialization

REGISTER NAME	BIT 9	8	7	6	5	4	3	2	1	0
DIntCtrl	0	1	0	0	0	r	r	r	r	r
DStatCtrl	0	0	0	0	0	0	0	0	0	0
MIntCtrl			0	0	0	0	0	0	0	r
MStatCtrl			ext	ext	1	1	0	0	0	0
MCClock					0	0	0	0	0	0

NOTE 6: r= reserved; ext= bit value from external terminal

4.24 Microcontroller Interface

The microcontroller interface of the TCM4300 is a general purpose bus interface (see Table 4–24) which ensures compatibility with a wide range of microcontrollers, including the Mitsubshi M37700 series and most Intel and Motorola series. The interface consists of a pair of microcontroller type select inputs MTS1 and MTS0, address and data buses, as well as several input and output control signals that are designed to operate in a manner compatible with the microcontroller selected by the user. See Sections 3.2 to 3.11 for Interface timing requirements.

Table 4–24. Microcontroller Interface Configuration

MTS1	MTS0	MODE	POLARITY	
			DATA STROBE (DS) ACTIVE	INTERRUPT/OUTPUT ACTIVE
0	0	Intel	Low (separate read and write)	High
1	0	Motorola 16-bit and Mitsubishi	Low	Low
0	1	Motorola 8-bit	High	Low
1	1	Reserved	N/A	N/A

The microcontroller interface of the TCM4300 is designed to allow direct connection to many microcontrollers. Except for the interrupt terminals, it is designed to connect to microcontrollers in the same manner as a memory device.

The internal chip select is asserted when MCCSH = 1 and MCCSL = 0.

4.24.1 Intel Microcontroller Mode Of Operation

When the microcontroller type select inputs MTS1 and MTS0 are both held low, the TCM4300 microcontroller interface is configured into Intel mode (see Table 4-25). In this mode, the interface uses separate read and write control strobes and active-high interrupt signals. The processor $\overline{RD}$ and $\overline{WR}$ strobe signals should be connected to the TCM4300 MCDS signal and MCRW signal, respectively. The multiplexed address and data buses of the microcontroller must be demultiplexed by external hardware. Table 4–25 lists the microcontroller interface connections for Intel mode.

Table 4–25. Microcontroller Interface Connections for Intel Mode

TCM4300 TERMINAL	MICROCONTROLLER TERMINAL
MTS1, MTS0	Tie to logic level low
MCCSH	Not on microcontroller; can be used for address decoding
MCCSL	Not on microcontroller; can be used for address decoding
MCD7–MCD0	AD[7:0] data bus on microcontroller
MCA4–MCA0	Demultiplexed address bits not on microcontroller
MCRW	$\overline{WR}$ (Active-low write data strobe)
MCDS	$\overline{RD}$ (Active-low read data strobe) MCDS configured to active-low operation by MTS1 and MTS0. The microcontroller bus must be demultiplexed by external hardware.
MWBDFINT	Either one of INT3 through INT0 as appropriate
DINT	Either one of INT3 through INT0 as appropriate

4.24.2 Mitsubishi Microcontroller Mode of Operation

When the microcontroller type select MTS1 and MTS0 inputs are held high and low, respectively, the TCM4300 microcontroller interface is configured in Mitsubishi mode. In this mode, the interface has a single read/write control (R/$\overline{W}$) signal, an active-low data strobe (MCDS) signal, and active-low interrupt request signals. The processor $\overline{E}$ and R/($\overline{W}$) signals should be connected to the TCM4300 MCDS signal and the MCRW signal, respectively. Table 4–26 lists the microcontroller interface connections for Mitsubishi mode.

Table 4–26. Microcontroller Interface Connections for Mitsubishi Mode

TCM4300 TERMINAL	MICROCONTROLLER TERMINAL
MTS1, MTS0	Tie to logic levels: high and low, respectively
MCCSH	Not on microcontroller; can be used for address decoding
MCCSL	Not on microcontroller; can be used for address decoding
MCD7–MCD0	D[7:0] data bus on microcontroller
MCA4–MCA0	A[4:0]
MCRW	R/$\overline{W}$
MCDS	$\overline{E}$ (Active-low read data strobe) MCDS configured to active-low operation by MTS1 and MTS0.
MWBDFINT	Either one of INT3 through INT0 as appropriate
DINT	Either one of INT3 through INT0 as appropriate

4.24.3 Motorola Microcontroller Mode of Operation

When the microcontroller selects MTS0 = high and MTS1 = low, the TCM4300 microcontroller interface is configured for 8-bit family (6800 family derivatives, e.g., 68HC11D3 and 68HC11G5) bus characteristics, and when the microcontroller selects MTS0 = low and MTS1 = high, the microcontroller interface is configured for 16-bit family (680$\times$0 family derivatives, e.g., 68008 and 68302) characteristics. The Motorola mode makes use of a single read/write control (R/$\overline{W}$) signal and active-low interrupt request signals. The processor E (8-bit) or $\overline{DS}$ (16-bit) and (R/$\overline{W}$) control signals should be connected to the TCM4300 MCDS signal and the MCRW signal, respectively. Table 4–27 illustrates the connections between the TCM4300 and an 8-bit Motorola processor. Table 4–28 illustrates the connections between the TCM4300 and a 16-bit Motorola processor.

Table 4–27. Microcontroller Interface Connections for Motorola Mode (8 bits)

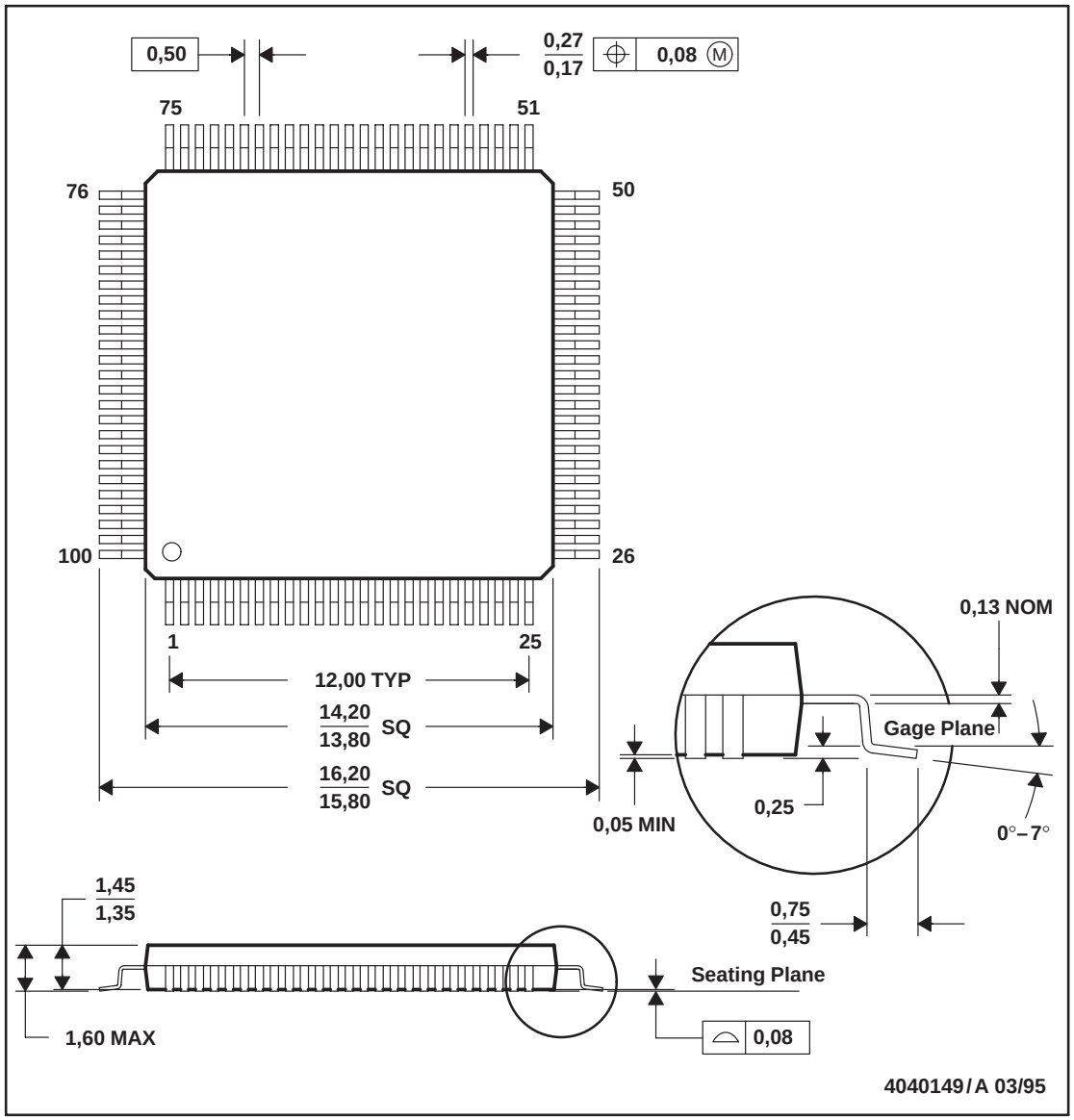
TCM4300 TERMINAL	MICROCONTROLLER TERMINAL
MTS1, MTS0	Tie to logic levels: low and high, respectively
MCCSH	Not on microcontroller; can be used for address decoding
MCCSL	Not on microcontroller; can be used for address decoding
MCD7–MCD0	PC[7:0] data bus on microcontroller
MCA4–MCA0	Demultiplexed address output. PF[4:0] on microcontroller for nonmultiplexed machines (e.g., 68CH11G5) and not on micro for multiplexed bus machines (e.g., 68HC11D3).
MCRW	R/$\overline{W}$
MCDS	E (Active-high data strobe) MCDS configured to active-high operation by MTS1 and MTS0.
MWBDFINT	$\overline{IRQ}$ and/or $\overline{NMI}$ as appropriate
DINT	$\overline{IRQ}$ and/or $\overline{NMI}$ as appropriate

Table 4–28. Microcontroller Interface Connections for Motorola Mode (16 bits)

TCM4300 TERMINAL	MICROCONTROLLER TERMINAL
MTS1, MTS0	Tie to logic levels: high and low, respectively
MCCSH	Not on microcontroller; can be used for address decoding
MCCSL	Not on microcontroller (68000, 68008) $\overline{CS1}$, $\overline{CS2}$, or $\overline{CS3}$ (68302)
MCD7–MCD0	D[7:0] data bus on microcontroller
MCA4–MCA0	A[4:0] (68008) A[5:1] (68000, 68302)
MCRW	R/$\overline{W}$
MCDS	$\overline{DS}$ active-low data strobe (68008) $\overline{LDS}$ (active-low data strobe) (68000, 68302) MCDS configured to active-low operation by MTS1 and MTS0.
MWBDFINT	IACK7, IACK6, or IACK1 (68302) Not on microcontroller (68000, 68008)
DINT	Either one of INT3 through INT0 as appropriate

5 Mechanical Data

5.1 PZ (S-PQFP-G100) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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