TCM8030
Analog Baseband Processor
User's Guide

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Preface

Read This First

About This Manual

This manual provides design information for the TCM8030 analog cellular telephone baseband processor. The manual is written for senior engineers, junior engineers, and support staff who design and develop analog cellular telephone baseband processors and applications.

You should be familiar with basic telecommunications concepts, analog theory, and cellular applications.

How to Use This Manual

This document contains generic and specific information about the TCM8030 baseband processor.

Chapter 1 Provides an overview of TCM8030 analog cellular telephone baseband processing

Chapter 2 Describes the principles that apply during operation of the TCM8030 analog cellular telephone processor

Chapter 3 Describes the receive processing procedure for the forward control channel (FOCC) and the forward voice channel (FVC)

Chapter 4 Provides AMPS wideband data reverse channel transmission processing procedures for both the reverse control channel (RECC) and reverse voice channel (RVC)

Chapter 5 Describes TCM8030 wideband data transmissions and provides wideband data transmission examples

Chapter 6 Describes the process and methods used during reverse control channel arbitration

Chapter 7 Defines automatic frequency control and its system cycle

Chapter 8 Provides basic information regarding the programmable expansion input/output ports, special function port keys, and read and write register definitions

Chapter 9 Describes the baseband processing techniques to apply necessary external circuitry to the TCM8030

Notational Conventions

- An overscored $\overline{\text{word}}$ indicates a signal that is active low.
- Words that serve to emphasize an important element, notation, or imperative in a procedure are emphasized in **bold .**

Related Documentation From Texas Instruments

The following books describe the TCM8030 and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924. When ordering, please identify the book by its title and literature number.

- ***TCM8030 Analog Baseband Processor Data Manual*** (literature number SLW033A) describes the component and electrical specifications for the TCM8030.
- ***TPS72xx Micropower Low-Dropout (LDO) Voltage Regulators*** (literature number SLVS102E) describes the components and electrical specifications for the TPS72xx family.

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Chapter 1

Introduction

This chapter provides an overview of TCM8030 analog cellular telephone baseband processing. It describes TCM8030 features and the power modes used in generic and specific processing applications, as detailed in later chapters.

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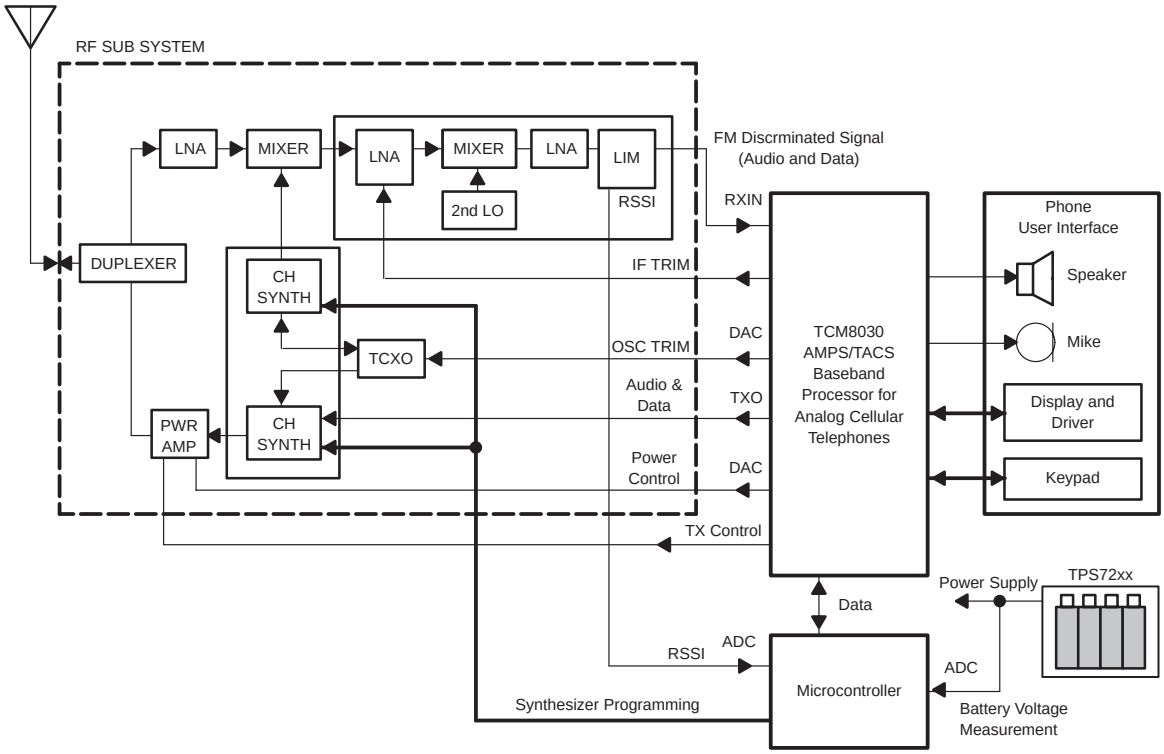
1.1 Analog Cellular Telephone Baseband Processing

The TCM8030 baseband processor provides a unique low-power solution for advanced mobile phone services (AMPS), narrowband advanced mobile phone services (NAMPS), total access communication systems (TACS), extended total access communication systems (ETACS), narrowband total access communication systems (NTACS), and Japanese total access communication systems (JTACS) baseband processing.

Figure 1–1 shows the TCM8030 in a typical telecommunications application.

Figure 1–1. TCM8030 Typical Analog Cellular Processing



Note: The TPS72xx family of the micropower low-dropout (LDO) voltage regulators provides the necessary power supply management for a typical analog cellular application using the TCM8030.

1.2 TCM8030 Features

The TCM8030 provides all data and audio processing functions for AMPS, NAMPS, TACS, ETACS, NTACS, and JTACS in a compact, low-power, baseband processor enclosed in an 80-pin TQFP package.

1.2.1 Data Processing Features

The TCM8030 provides data transceiver, data processing, and supervisory audio tone (SAT) functions, and includes the following data processing features:

- ❑ Single-chip processing for AMPS, NAMPS, TACS, ETACS, NTACS, JTACS, SAT, and digital supervisory audio tone (DSAT)
- ❑ 2.7-V to 5.5-V operation
- ❑ Serial interface
- ❑ User-configurable interrupt structure
- ❑ Transmit (TX) and receive (RX) data buffers
- ❑ Integrated RX and TX data filters
- ❑ TX wideband (WB) SAT filter
- ❑ RX WB and narrowband (NB) SAT filters
- ❑ RX WB and NB data comparator
- ❑ Programmable timer
- ❑ Independent watchdog timer
- ❑ RX/TX automatic mute functions
- ❑ Arbitration processing
- ❑ Twenty programmable expansion I/O ports
- ❑ WB and NB-RX recovery
- ❑ Automatic frequency control (AFC)
- ❑ Multiple power-saving mode implementation
- ❑ Separate encoder for WB-TX and NB-TX

1.2.2 Audio Processing Features

The TCM8030 provides the following audio processing features:

- ❑ AMPS, NAMPS, TACS, ETACS, NTACS, and JTACS operation
- ❑ Integrated RX and TX voice filters
- ❑ Microphone amplifiers and loud speaker drivers
- ❑ Pre-emphasis and de-emphasis filtering
- ❑ Digitally-controlled gains and signal selection or muting
- ❑ Adjustable TX limiter
- ❑ Three 8-bit digital-to-analog converters (DAC) with output buffers
- ❑ Dual-tone multifrequency (DTMF) generator
- ❑ On-chip compandor
- ❑ Flexible clock and oscillator operation

1.3 Power Modes

The TCM8030 power mode structure provides independent powering of various on-chip circuits, thereby enabling the creation of low-power designs that are ideal for frequency modulation (FM) analog cellular telephones. The power modes are as follows:

- Total power-down mode
- Shutdown mode
- Idle mode
- Tonemode
- Full operation (DTMF TX off) mode
- Full operation (DTMF TX on) mode

Chapter 2

Principles of Operation

This chapter describes the principles that apply during operation of the TCM8030 analog cellular telephone processor.

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2.1 Principles of Operation Overview

The TCM8030 provides a complete, low-power, integrated solution for FM analog cellular telephones by integrating the analog processing and digital data processing functions onto one chip.

The TCM8030 contains transmit (TX) and receive (RX) analog paths, a digital data processor with filters, a compressor and expandor, routing switches, data input/output (I/O), an audio power amplifier, an uncommitted operational amplifier, and a DTMF generator. With these circuits, the TCM8030 applies appropriate signal levels for AMPS, NAMPS, TACS, ETACS, JTACS, and NTACS standards. In addition, both analog paths are software configurable such that all audio trimming functions can be achieved without manual intervention.

The TCM8030 data processor has several functional features: it performs transmit encoding and receive decoding, as well as majority voting and data recovery; it generates supervisory audio tone (SAT) and digital supervisory audio tone (DSAT); and it implements a number of independent circuits for arbitration logic, timers, and power logic. These features, along with a simple serial peripheral interface (SPI™) that interfaces with an external microcontroller, make the TCM8030 data processor extremely effective for all of the analog standards.

The TCM8030 provides greater integration than typical analog cellular baseband systems; thus, it reduces power consumption and increases talk and standby time. This integration, along with the other TCM8030 features, offers an efficient and effective cost solution for FM analog telephones and related applications.

Figure 2–1 shows a simplified block diagram of the device, and Figure 2–2 shows a detailed functional block diagram of the device.

Figure 2–1. TCM8030 Simplified Block Diagram

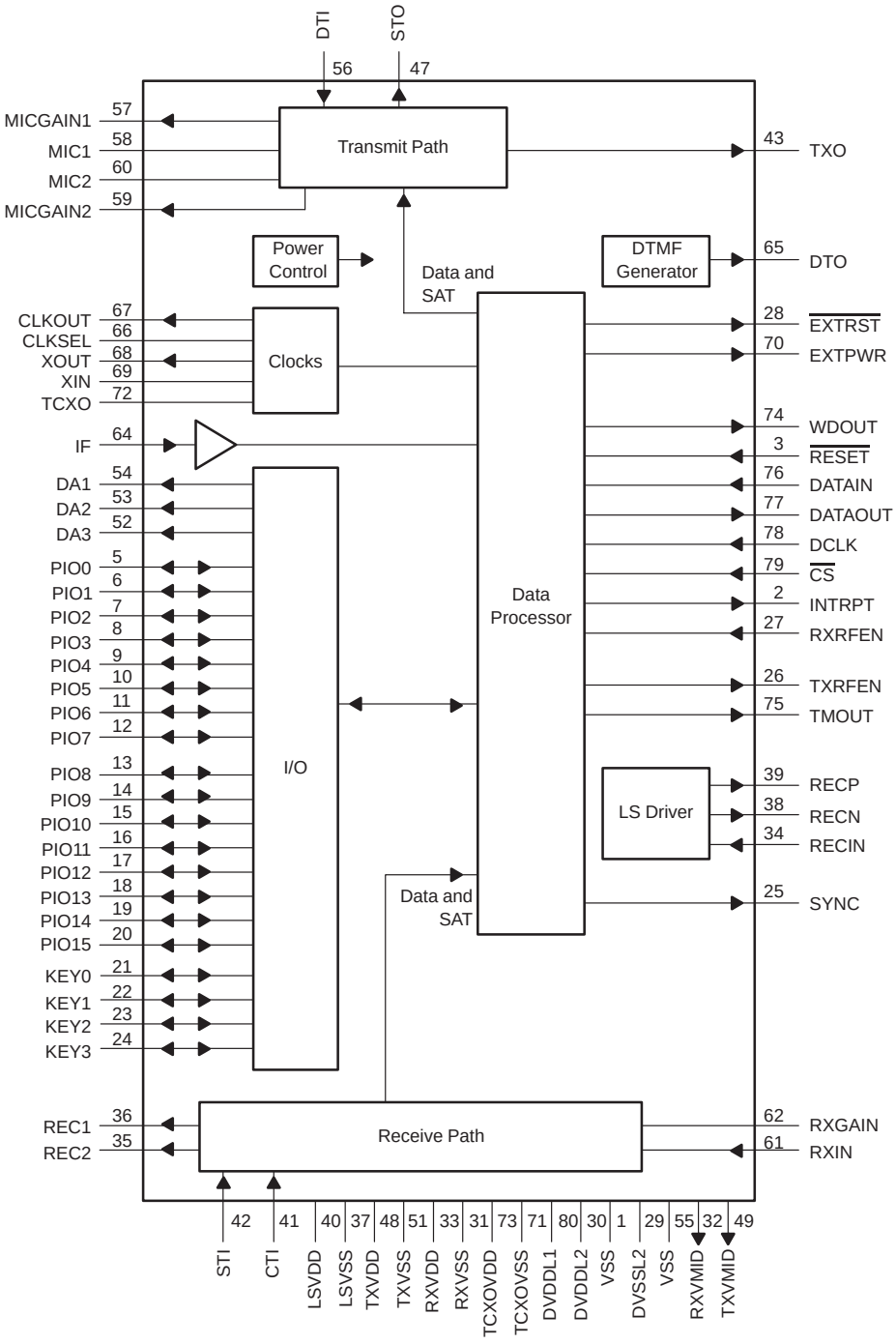


Figure 2–2. TCM8030 Detailed Functional Block Diagram

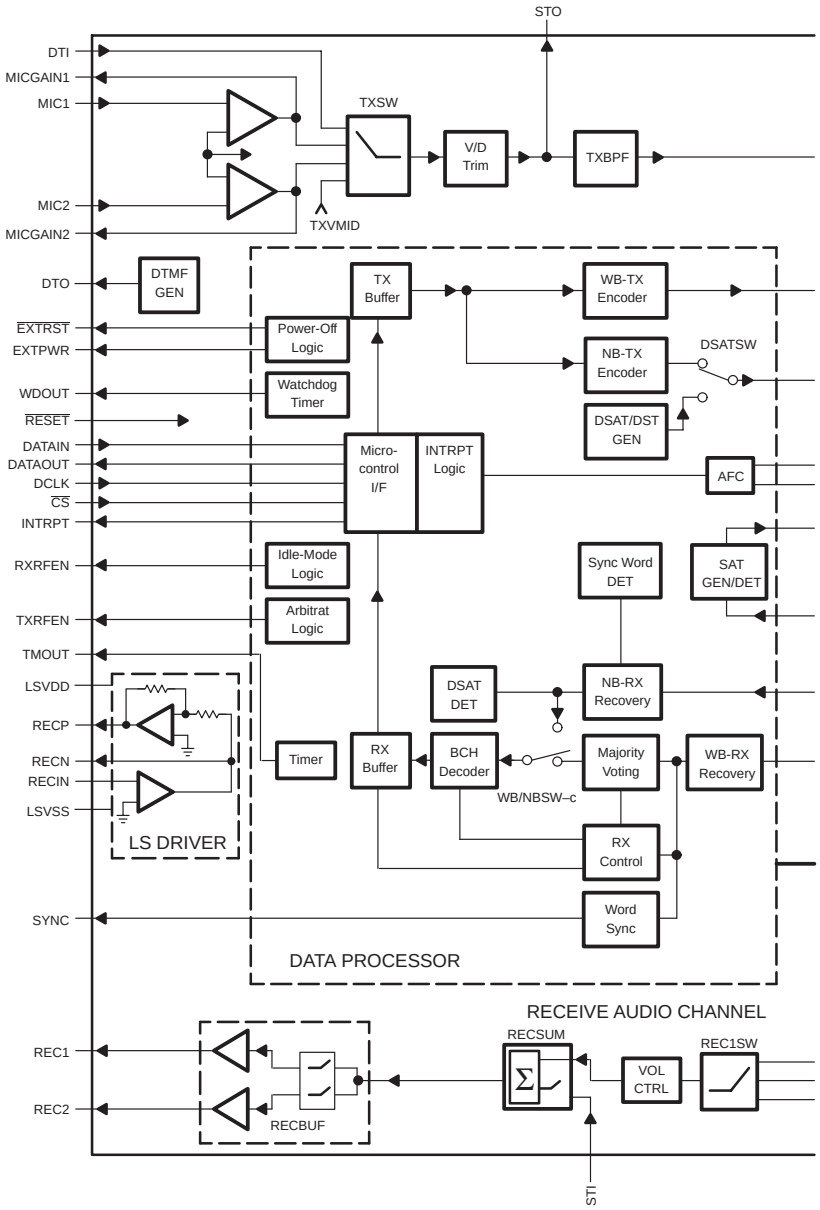
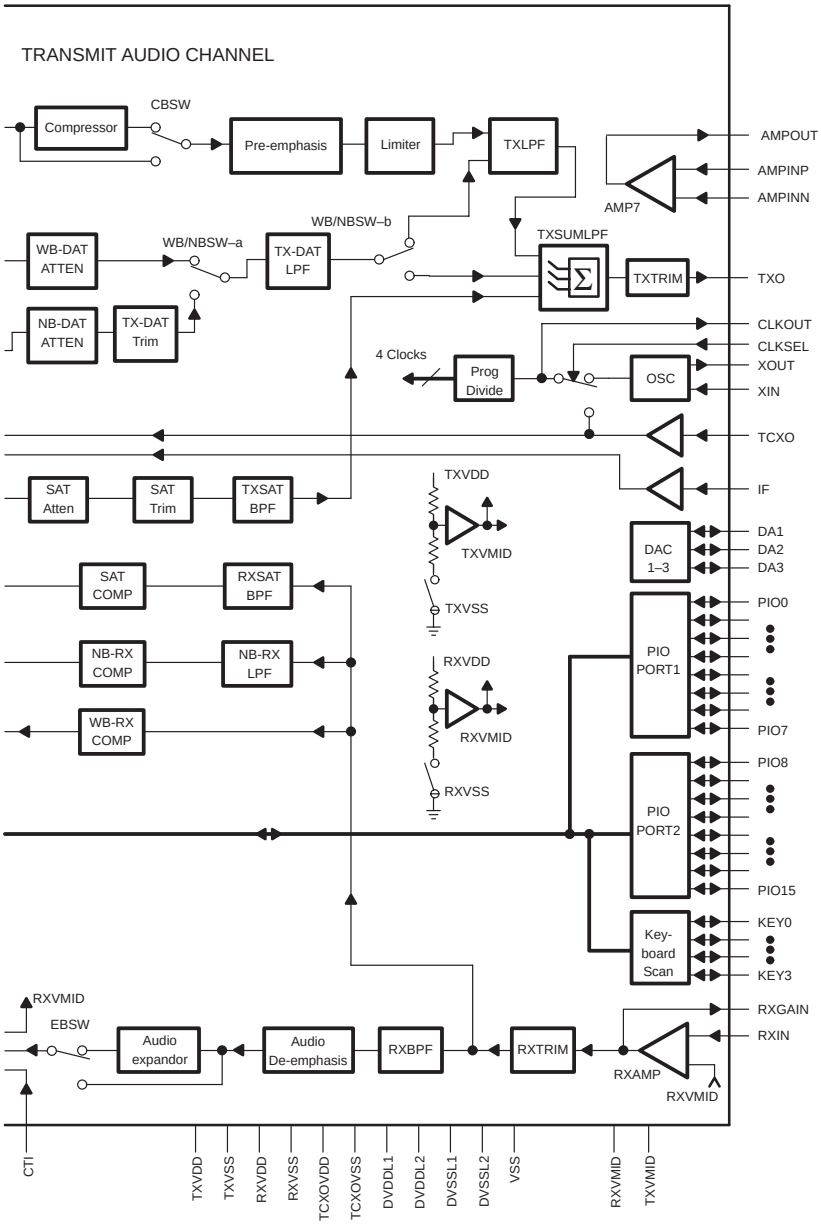


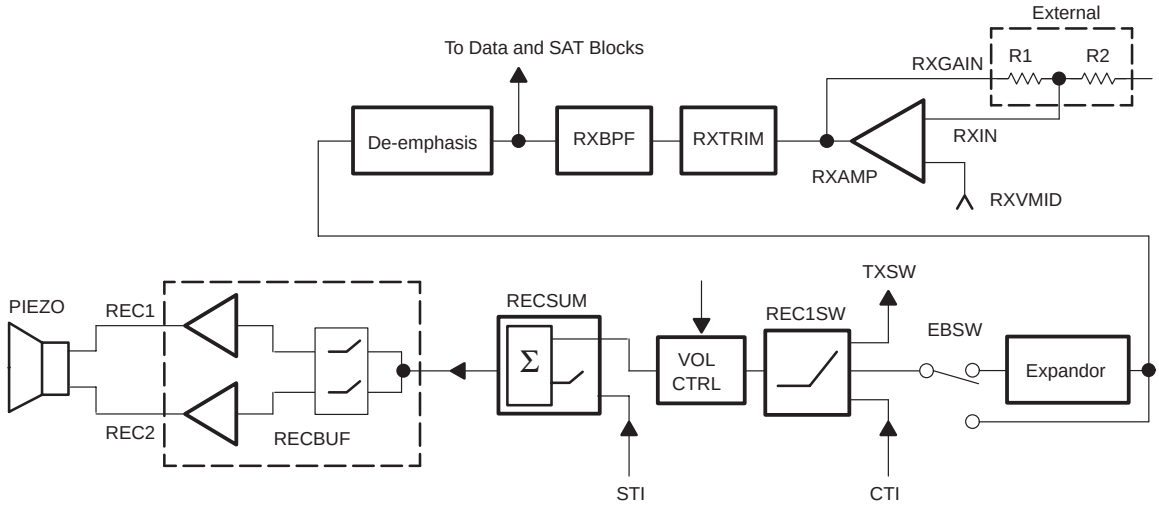
Figure 2–2. TCM8030 Detailed Functional Block Diagram (Continued)



2.2 Receive Audio Path

Figure 2–3 shows the receive audio path. A pair of external gain-setting resistors (R1 and R2) adjusts the input sensitivity to system requirements. A second digitally programmable gain trim is provided in RXTRIM, followed by a band-pass filter (BPF). The filter output drives the data/SAT blocks and the de-emphasis block.

Figure 2–3. Receive Audio Path



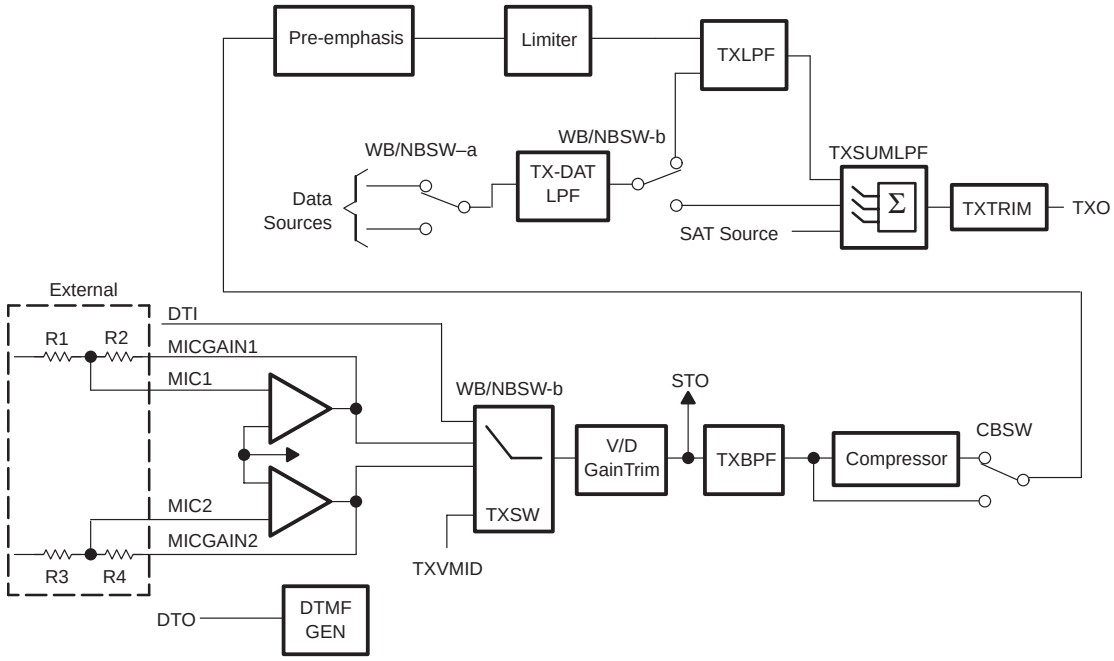
You can bypass the expandor for testing purposes or for applying linear functions. The switch REC1SW allows you to select either the transmit loop-back, the expandor output, or the call tone input (CTI) to feed into the digitally programmable volume control (VOL CTRL).

The receive summing block (RECSUM) sums (or does not sum) the sidetone input (STI) with the audio signal, based on a software command. The final stage consists of a pair of configurable receive buffers (RECBUF) that drives a piezospeaker or other light load. A separate loudspeaker driver block (LS DRIVER) is discussed later.

2.3 Transmit Audio Path

Figure 2–4 shows the block diagram for the transmit path. Here, you can select transmit inputs by using software control for the transmit switch (TXSW). The MIC1 and MIC2 inputs have operational amplifiers that you can configure with external gain-setting resistors R2/R1 and R4/R3. A selectable DTMF signaling input (DTI) is provided. You can use this with a programmable DTMF generator that has an independent output (DTO).

Figure 2–4. Transmit Audio Path



A programmable voice/DTMF gain trim stage (V/D TRIM) outputs to the sidetone output (STO) and drives the transmit band-pass filter (TXBPF). The signal from the TXBPF goes to the audio compressor. A bypass switch (CBSW) allows you to bypass the compressor for DTMF tones, as well as other uncompressed functions that might require testing.

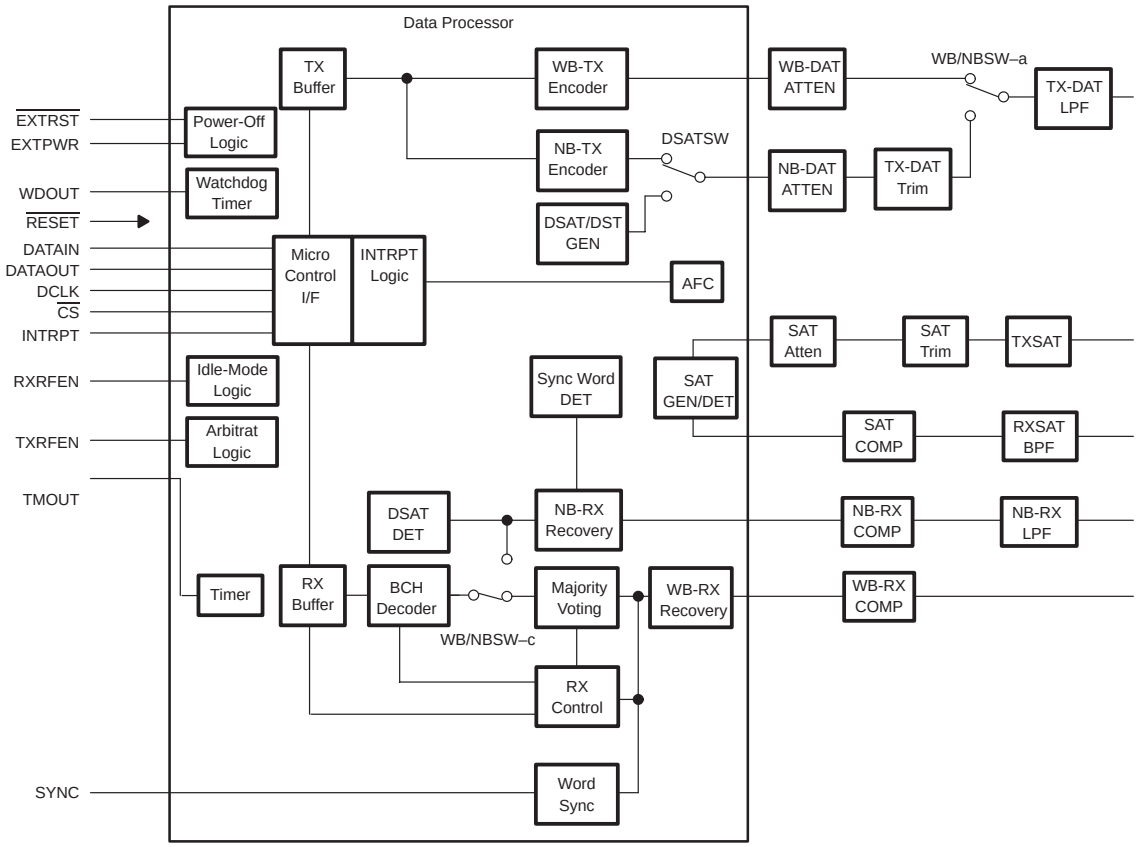
The pre-emphasis and (deviation) limiter blocks then drive the transmit low-pass filter (TXLPF). This attenuates the harmonics caused by limiting the signal. Some data transmission modes use the TXLPF route, which inverts the signal. This requires reinversion of the data signal polarity using either inversion set/reset bits or external means.

The transmit summer and low-pass filter block (TXSUMLPF) selects voice, data, or SAT signals and sums them together. It also provides a continuous-time smoothing filter that removes high-frequency products. The transmit gain-trim (TXTRIM) is the final stage that drives the output terminal (TXO).

2.4 Data Processor

The data processor, shown in Figure 2–5, provides a large number of functions for processing cellular data streams and controlling other functions of the TCM8030. The microcontroller interface is a simple serial-shift register function that uses DATAIN, DATAOUT, DCLK, and $\overline{CS}$ (active-low chip select), and has an interrupt output (INTRPT). This interface allows the TCM8030 to communicate with the microcontroller that is operating the telephone.

Figure 2–5. Data Processor Block Diagram



Power-off and idle-mode logic are provided, together with both standard and watchdog timers. The data processor selects incoming receive (RX) data according to standard (for example, WB/NB). The filters/comparators process the data to comply with the standard. After majority voting and/or BCH decoding, the data processor buffers the data and applies it to the microcontroller interface. On the transmit side, data moves to the TX buffer after the data processor selects the appropriate encoder. The encoded data

goes through the attenuator and/or trim stage to the transmit data low-pass filter (TX-DAT LPF) and switches to the transmit (TX) audio path.

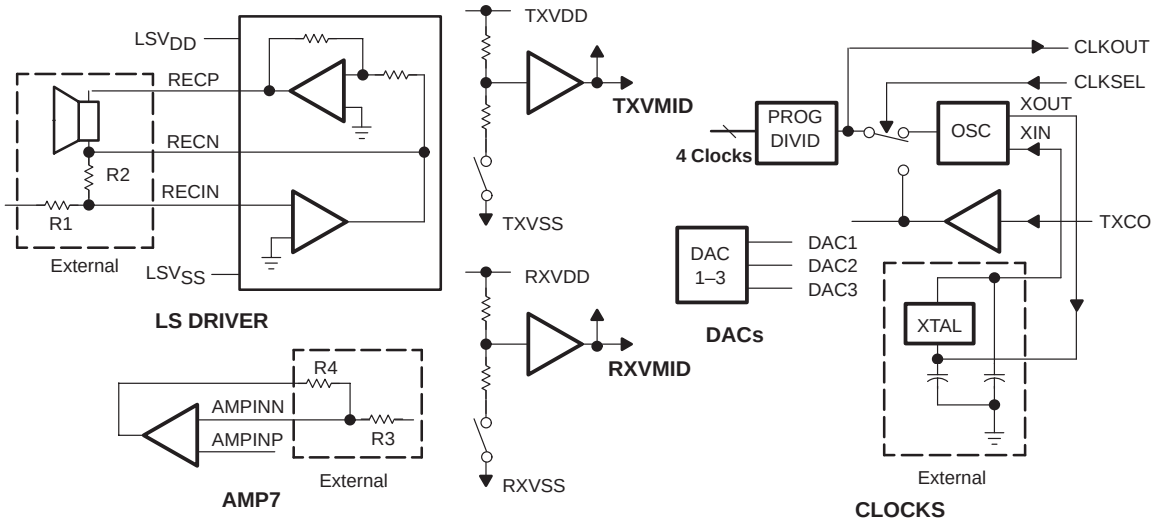
The RXSAT filter and SAT comparator recover the SAT (supervisory audio tone) from the receive audio path and feed it to the data processor detector/ generator. The SAT GEN/DET block generates TXSAT and applies it through programmable attenuator/trim stages to the band-pass filter that feeds the transmit path.

The NB data recovery block detects a DSAT (digital supervisory audio tone) signal. The DSAT/DST GEN regenerates the DSAT signal and sends it through the normal NB-DAT path to the transmit path.

2.5 Miscellaneous Circuits

Figure 2–6 shows miscellaneous circuit block diagrams. The LS DRIVER block provides the capability to drive loudspeakers. The external resistor pair R2/R1 sets the gain. An uncommitted operational amplifier (AMP7) is provided, and the external resistor pair R4/R3 sets the gain.

Figure 2–6. Miscellaneous Circuit Block Diagrams



A separate mid-rail voltage source is provided for both the receive and transmit paths (RXVMID and TXVMID). Each is deselected when its part of the circuit powers down.

You may program the TCM8030 clocking source (oscillator signal or external clock) that applies to a programmable divide (PROG DIVID). PROG DIVID divides the clocking source into four separate internal clocking signals. The oscillator block requires only a crystal oscillator (XTAL) and a pair of capacitors for operation. Alternatively, you can connect an external clock at XIN, or you may select a TCXO, as required. A triple DAC is also provided for oscillator trim functions. When used in conjunction with the AFC control in the data processor block, the triple DAC allows you to use lower stability oscillators successfully, to save system costs.

2.6 Clocks

The TCM8030 oscillator and programmable divider (OSC and PROG DIVID) circuits generate internal clocks and an external clock output on the CLKOUT terminal. The circuits are shown in Figure 2–2.

The TCM8030 CLKSEL terminal selects the clocking source, as shown in Table 2–1.

Table 2–1. Clock Sources

TCM8030 Clocking Scheme	CLKSEL	Description
XTALOSC	LOW	Clock Source is the internal crystal oscillator (XTALOSC). An external crystal oscillator is required and is connected between XIN and XOUT (terminals 69 and 68). Any frequency in Table 2–2 is allowed. In addition, TCXOAMP can be enabled by selecting IFAMPEN in register AUXPE (write address 30H, bit 4).
External square wave	LOW	Clock source is an external square wave frequency with a standard CMOS logic level input applied to XIN (terminal 69). Any frequency in Table 2–2 is allowed. In addition, TCXOAMP can be enabled by selecting IFAMPEN in register AUXPE (write address 30H, bit 4).
External TCXO (temperature-compensated crystal oscillator)	HIGH	Clock source is an external TCXO with a minimum amplitude of 0.5-Vp-p applied to TCXO (terminal 72). Any frequency in Table 2–2 is allowed. In this mode, the XTALOSC block is powered down and TCXOAMP is enabled independent of the settings of register AUXPE (write address 30H).

The TCM8030 has an automatic frequency control (AFC)circuit that maintains the accuracy of an external temperature-compensated crystal oscillator (TCXO). For the first two clock sources (XTALOSC or external square wave), the AFC circuit operates with any TCXO operating at a frequency less than 20 MHz. However, for the third clock source (external TCXO), the AFC operates with a TCXO at a frequency associated with CKRT (write address 31H, bits 0–2), as shown in Table 2–2.

Table 2–2. Master Clock Input Frequency and CLKOUT Select

Bit 2 CKRT2	Bit 1 CKRT1	Bit 0 CKRT0	Bit 3 CLKOUTSEL	Frequency Selected	Terminal CLKOUT
0	0	0	X	5.12 MHz	X
0	0	1	X	7.68 MHz	X
0	1	0	X	10.24 MHz	X
0	1	1	X	12.8 MHz	X
1	0	0	X	15.36 MHz	X
1	0	1	X	17.92 MHz	X
1	1	0	X	†	X
1	1	1	X	†	X
X	X	X	0	X	Active
X	X	X	1	X	Hi-Z

† CKRT(bits 0–2) = 110 and 111 are not allowed.

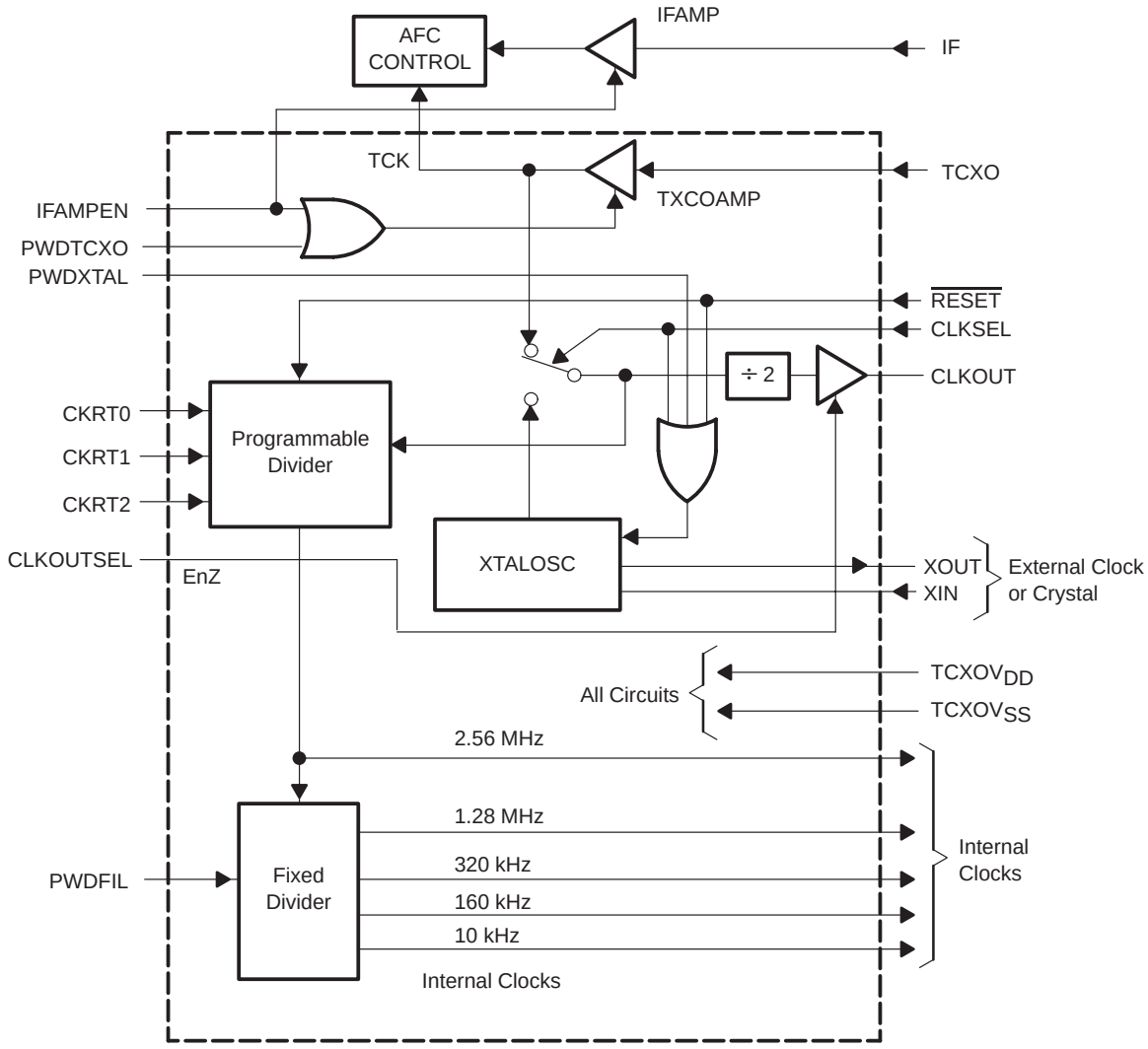
The TCM8030 also provides an external divide-by-two counter clock (CLKOUT). If CLKSEL is high, the internal XTALOSC or external square wave-frequency signal source routes through a divide-by-two counter to CLKOUT. If CLKSEL is low, the external TCXO frequency routes through the divide-by-two counter to CLKOUT. CLKOUTSEL is low after reset. CLKOUT is active.

The TCM8030 also possesses a frequency divider circuit that derives the internal and external reference clocks (2.56 MHz to the data processor and 1.28 MHz, 320 kHz, 160 kHz, and 10 kHz to the audio processor).

The internal crystal oscillator (XTALOSC), TCXO input recovery circuit (TCXOAMP), and internal dividers (PROG DIVID) share their own dedicated power supply terminals. This minimizes crosstalk from the rest of the circuit, therefore reducing the amount of clock jitter.

All the clock circuits power down in the TCM8030 power-down mode. In all other modes, the clock circuits stay active. Program the appropriate external clock or crystal frequencies using the clock source frequency-select, write address 31H, CLKSRC. Use CKRT0 – CKRT2 (CLKSRC bits 0 – 2) to program the frequency, and CLKOUTSEL (CLKSCR bit 3) to enable or disable CLKOUT. A reset will select, by default, a 5.12-MHz frequency (CKRT0 – CKRT2 = 000) and CLKOUT will become active (CLKOUTSEL = 0) (see Table 2–2). Figure 2–7 illustrates the TCM8030 clocking scheme.

Figure 2–7. Clocking Scheme Functional Block Diagram



2.7 Power Modes

The TCM8030 contains power-off logic circuitry that implements six modes of operation, as shown in Table 2–3 and Figure 2–8. These modes are selected by control word 4. In total power-down mode, all internal circuits, including the crystal oscillator (XTALOSC), are disabled.

Table 2–3. Power Modes Block Diagram Legend

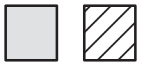
Power Modes	Description	Coding
1. Total power-down mode	Power is applied to the TCM8030, but all circuits are powered down. EXTPWR is low to disable power supply to the rest of the phone. Only a static power-up using one of the keyboard interrupt ports allows the TCM8030 to exit total power-down mode. When this happens, the TCM8030 enters shutdown mode.	
2. Shutdown mode	Power is applied to the TCM8030, but the phone is unable to receive calls. The microcontroller may access internal registers, but it may not issue commands. Only the circuits with the following coding are on.	
3. Idle mode	Power is applied to the TCM8030, and the phone is monitoring the forward control channel (FOCC) from the base station. Only the circuits with the following coding are on.	
4. Tone mode	Power is applied to the TCM8030, but the phone is not in communication with the base station. The user interface (via the I/O ports) is enabled. Only the circuits with the following coding are on.	
5. Full operation mode, DTMF off	Power is applied to the TCM8030. The phone is in conversation mode, but the DTMF generator is not enabled. All circuits except the circuit with the following coding are on.	
6. Full operation mode, DTMF on	Power is applied to the TCM8030. The phone is in conversation mode, but the DTMF generator is enabled. All circuits are on.	
Auxiliary Circuits *Power enabled independently*	Independent enabling can be applied to IFAMP, DAC1–3, and AMP7. Only the circuits with the following coding have this feature. In total power-down mode, this feature and these circuits are disabled.	

Figure 2–8. Power Modes Block Diagram

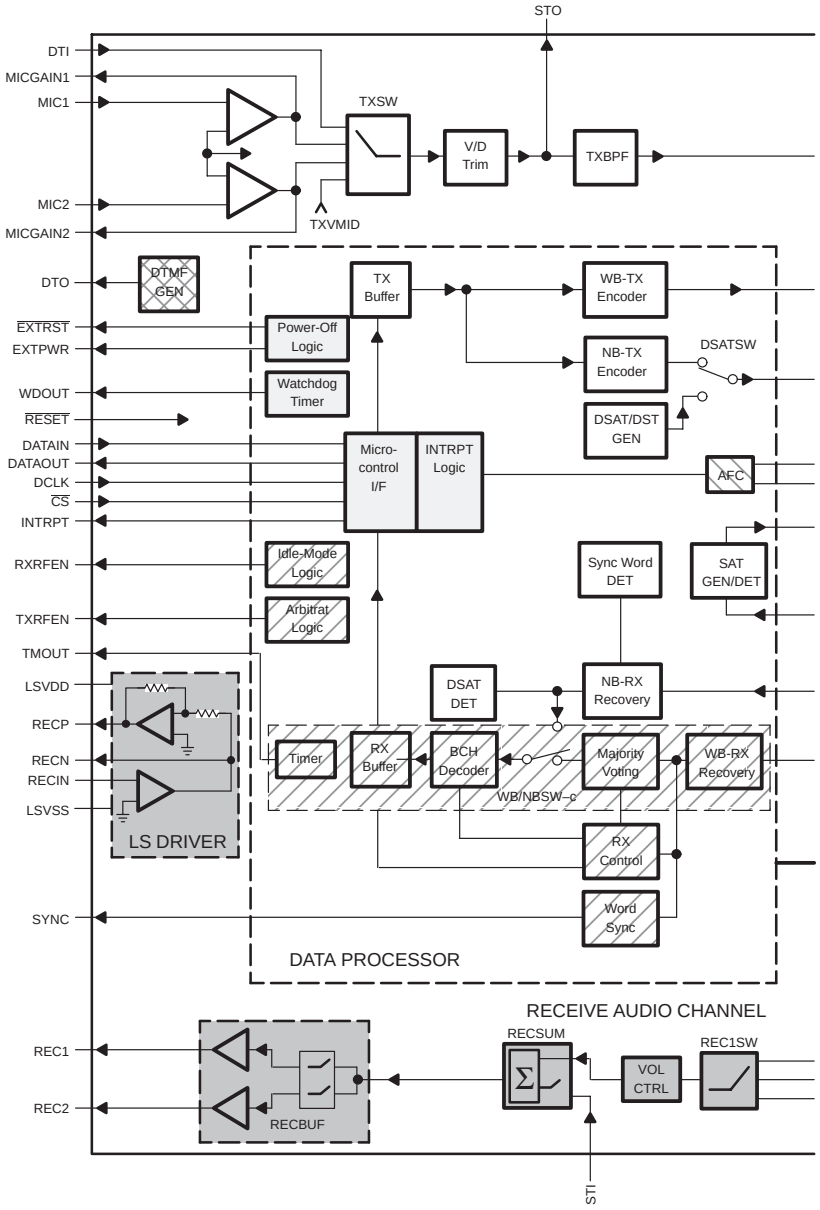
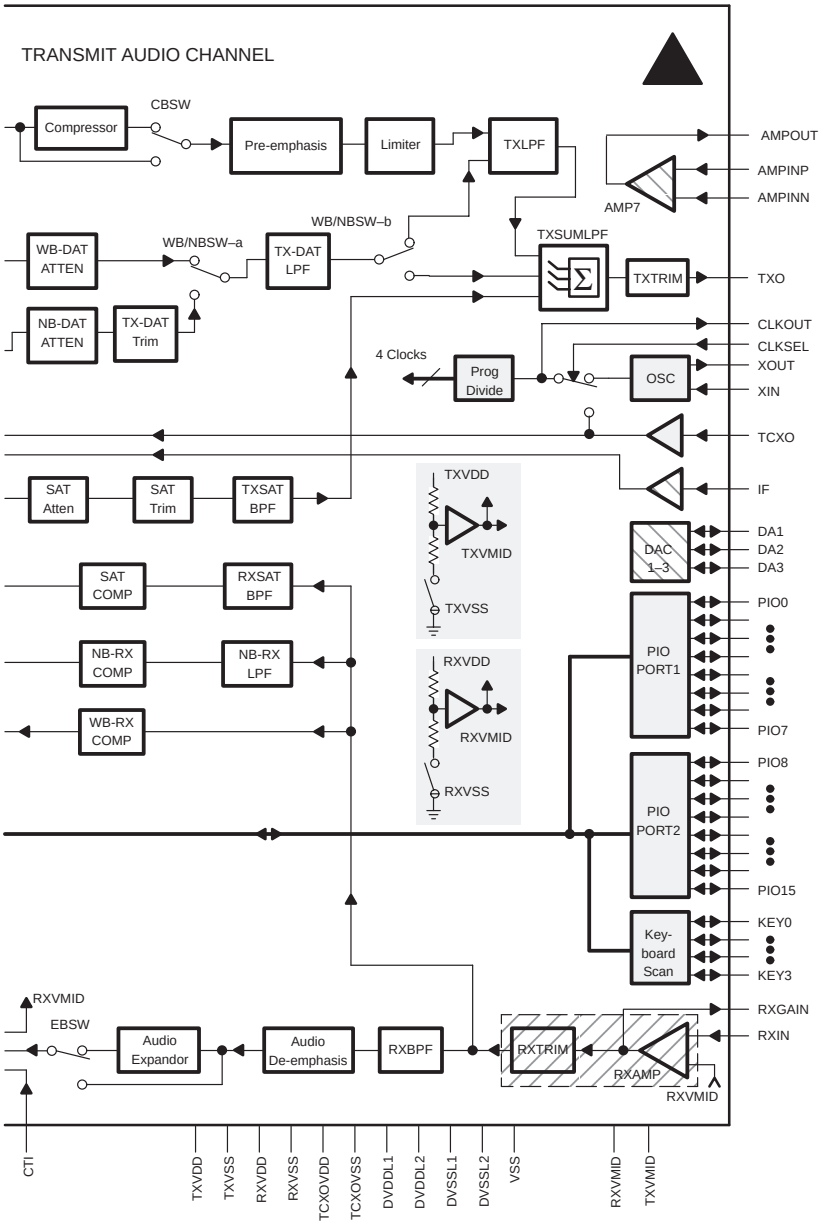


Figure 2–8. Power Modes Block Diagram (Continued)



2.7.1 Total Power-Down Mode

In this mode, power is still applied to the TCM8030, but the device is in total power-down mode. All circuits, including CLOCK, bias circuits, PIOs, and the watchdog timer, power down. The TCM8030 stops so it draws minimal leakage current, as illustrated in Figure 2–8. The EXTPWR output terminal is low to disable the power supply to the rest of the telephone (including the MCU). The $\overline{\text{EXTRST}}$ terminal is also low, and the TCM8030 microcontroller interface is disabled.

The TCM8030 is the only device in the telephone with its power supply enabled in total power-down mode. Static power-up logic, implemented using one of the keyboard interrupt ports, waits for the power-on key to be pressed. After the key is pressed, the TCM8030 exits the total power-down mode, reactivates the oscillator, enables the regulators to the rest of the telephone (using the EXTPWR enable signal), and holds the $\overline{\text{EXTRST}}$ terminal low for 0.1 to 0.2 second, to allow the rest of the telephone to go to power-up reset mode when the system is stable.

The TCM8030 goes into total power-down mode by writing to control word 4, (write address 03H, C4 bits 4–0). You must toggle both control word 4 (C4) bits 1–0, with this write transaction. The security bit, C4 bit 1, reduces the probability that the total power-down mode is entered erroneously, for example, by RFI (radio frequency interference).

The independent analog circuits IFAMP, AMP7, and DAC1–3 also power down in total power-down mode, independent of the status of their own power-down control bits in register AUXPE (write address 30H).

The cellular telephone uses the total power-down mode from the first connection of the battery as follows:

1) The telephone receives power for the first time when the battery is connected. Only TCM8030 initially connects to its power supply, powering up in shutdown mode. In this mode, CLKSEL sets the TCM8030 master clock source (see Section 2.6, *Clocks*), and it immediately sets EXTPWR high.

2) The power-up $\overline{\text{RESET}}$ input to the TCM8030 is held low during the operation of the external power-on-reset (RC) circuit. This also holds $\overline{\text{EXTRST}}$ at low.

3) When the external power-on reset mode finishes, $\overline{\text{EXTRST}}$ transitions to high, the TCM8030 microcontroller interface enables, and the MCU starts its boot routine. Because the TCM8030 INTRPT terminal is not set to one, the MCU knows that it was reset by a battery connect power up. (In this

situation the telephone should appear to be off until the power-on key is pressed). The MCU then writes to the TCM8030 to:

- Enable a keypad interrupt on the appropriate KEY pin. This requires four write transactions to TCM8030 registers:
  - PI3INT (write address 1CH) to enable the pin interrupt
  - PI3PULL (write address 1BH) to enable or disable the pullup as required
  - PIOC3 (write address 19H) to set direction as input
  - IE2 (write address 06H) to enable interrupts from the PIO3, keypad port
- Set the C4 bits 4–0 to 02H to enter total power-down mode.

The MCU must first enable the keypad port terminal connected to the power-on key before entering total power-down mode. If the MCU does not, only a $\overline{\text{RESET}}$ to the TCM8030 will re-enable it.

4) At this point the clock stops, EXTPWR transitions to low, $\overline{\text{EXTRST}}$ transitions to low, and the MCU and other parts of the system power off, waiting for the power-on key to be pressed.

5) When you press the power-on key, it is sensed on one of the KEY inputs. Asynchronous logic, which does not need the clock, reads the power-on key, forces TCM8030 back into shutdown mode, and turns EXTPWR back on. The TCM8030 event register also records the fact that a keypad interrupt was received.

6) EXTPWR transitions to high and powers up the microcontroller, and after a timed interval of between 0.1 and 0.2 second, including the XTALOSC warm-up time, TCM8030 releases $\overline{\text{EXTRST}}$, allowing the rest of the system to power up and reset when the system is stable. The MCU then executes its boot routine.

7) At this time, the INTRPT terminal from the TCM8030 is in active mode, and the microcontroller checks the TCM8030 event register and determines it was awakened by a keypad event, such as a pressed power-on key. When the MCU is awakened, the microcontroller starts to initialize the entire system, as appropriate.

2.7.2 Shutdown Mode

The microcontroller interface, clock, bias circuits, watchdog timer blocks, and all three PIOs remain operational in the shutdown mode, as illustrated in

Figure 2–8. The shutdown mode can be used when the telephone is switched on but cannot receive calls, for example, while the battery is recharging. The microcontroller interface may access all internal registers during shutdown mode, but may not issue commands (addresses 08H to 0EH).

2.7.3 Idle Mode

In addition to the circuits that are operational in shutdown mode, the wideband receive data path is enabled, as illustrated in Figure 2–8. This corresponds to the telephone being in idle mode, on a forward-control channel (FOCC). Two submodes also activate within the idle mode to further minimize power consumption in the telephone. First, the MCU idle submode (see the *TCM8030 Analog Baseband Data Manual* description for register E2 in read address map – read address 06H) enables the MCU to go to sleep when it does not receive any new messages, and the RXRF idle submode (see the *TCM8030 Analog Baseband Data Manual* description for register RXRFTIM in write address map – write address 20H) powers down the RF receiver when it is not needed.

2.7.4 Tone Mode

In addition to the circuits in shutdown mode, the DTMF generator and the section of the RX audio path that follows the call tone input (CTI) power up in tone mode, as illustrated in Figure 2–8. This mode is used when the telephone powers up, and when the user interface, such as the keypad and user memories, is enabled but the telephone does not communicate with the base station.

2.7.5 Full Operation Mode, DTMF TX Off

This mode corresponds to a telephone conversation in progress. All circuits are on, except the DTMF generator, as illustrated in Figure 2–8.

2.7.6 Full Operation Mode, DTMF TX On

This mode is enabled so that a DTMF tone can be transmitted during a telephone conversation. All circuits are on, as illustrated in Figure 2–8.

2.7.7 Independent Circuits

The IFAMP, DAC1–3, and AMP7 blocks can be individually powered down as described in the AUXPE register (write address 30H). These bits are overridden, and all circuits power down in total power-down mode, as illustrated in Figure 2–8.

2.8 Circuit Definitions

Within the TCM8030, certain circuits control specific analog baseband processor operations. Below is a list of these circuits and a description of their function.

2.8.1 Transmit Path Audio Processing Functions

The TCM8030 audio transmit path is composed of the following circuits, as shown in Figure 2–2. A brief functional description is given for each circuit.

- MIC1 and MIC2 amplifier

A pair of single-ended microphone amplifiers accept two input signals (MIC1 and MIC2). Gains for MIC1 and MIC2 are set using external resistors. Output from each amplifier is fed back through terminals MICGAIN1 and MICGAIN2.

- TXSW

The transmit switch (TXSW) selects one of four transmit audio sources. It selects either the voice signal from MICAMP1 or MICAMP2; the input pin DTI, which connects externally to the DTMF generator; or connects to TXVMID to mute the transmit path.

- V/D Trim

The voice or DTMF trim (V/D TRIM) circuit uses an antialiasing filter to process the audio signal before it is applied to the transmit band-pass filter. This circuit block also provides a means to trim the voice and DTMF signal levels.

- TXBPF

The transmit band-pass filter (TXBPF) is a switched capacitor band-pass filter that passes only the transmit audio frequencies from 300 Hz to 3 kHz.

- Compressor

The compressor circuit compresses the audio signal and outputs a signal with a change of 1 dB for an input signal change of 2 dB.

- CBSW

The compressor bypass switch (CBSW) permits the routing of the audio signal around the audio compressor circuit when testing the audio channel or passing DTMF signals.

❑ Pre-emphasis

As audio frequencies increase, the pre-emphasis circuit increases the signal gain at a rate of 6 dB per octave across the 300-Hz to 3-kHz audio passband.

❑ Limiter

The limiter circuit limits the transmit signal deviation within an acceptable range. The limiter has a set gain of +6.0 dB. The limiter also maintains a software programmable trim with a trim range from –10.97 dB to 7.5 dB.

❑ TXLPF

The transmit low-pass filter (TXLPF) is a switched-capacitor filter that removes harmonics caused by the (deviation) limiter. Linear-phase design prevents overshoots. This circuit is also used in narrowband mode to filter switched-capacitor output noise from TX-DAT LPF.

❑ TXSUMLPF

The transmit-summing and low-pass filter (TXSUMLPF) is a switched-capacitor filter that selectively sums voice, data, or SAT into the audio output. It also includes a low-pass switched-capacitor filter to reduce spurious output emissions above 10 kHz.

❑ TXTRIM

The transmit trim stage (TXTRIM) trims the FM deviation by transmitting either ST or wideband data prior to its output on the TXO terminal. This stage has a continuous second-order smoothing filter that removes noise.

2.8.2 Receive Path Audio Processing Functions

The TCM8030 audio receive path is composed of the following circuits, as shown in Figure 2–2. A brief functional description is given for each circuit.

❑ RXAMP

The receive amplifier circuit (RXAMP) receives its input from the RXIN terminal. A portion of the RXAMP output is applied, through the RXGAIN terminal, to a pair of external resistors that set the stage gain. The RXAMP noninverting input internally connects to the RXVMID reference level.

❑ RXTRIM

The receive trim (RXTRIM) stage compensates for FM discriminator variations. This block also contains a switched-capacitor filter to perform antialiasing.

❑ RXBPF

The receive band-pass filter (RXBPF) is a switched-capacitor filter with a pass-band from 300 Hz to 3 kHz.

❑ DE-EMPHASIS

As audio frequencies increase, the de-emphasis circuit decreases the signal gain at a rate of 6 dB per octave across the 300-Hz to 3-kHz audio pass-band.

❑ EXPANDOR

The audio expandor circuit expands the audio signal and outputs the signal with a change of 2 dB for an input signal change of 1 dB.

❑ EBSW

The expandor bypass switch (EBSW) permits the routing of the received audio signal around the expandor during testing.

❑ REC1SW

The receive 1 switch (REC1SW) selects one of three receive sources. REC1SW selects either the output from the expandor circuit (expanded or bypassed), the call tone (CTI) input, or selects and connects REC1SW to RXVMID to mute the receive path.

❑ VOL CTRL

The volume control (VOL CTRL) circuit can be programmed to provide a nominal gain of –20 dB to 17.5 dB for the outputs REC1 and REC2.

❑ RECSUM

The receiver summing circuit and switch (RECSUM) provide the means for adding sidetone (STI) input into the receive audio path.

❑ RECBUF

The receiver buffer (RECBUF) switches or mutes two output buffers independently, or it connects these buffers in differential mode so that a piezo-speaker can be connected to REC1 and REC2 terminals. Independent control of the two audio outputs allows one to be used for external hands-free operation.

❑ LS DRIVER

The loudspeaker driver (LS DRIVER) circuit is a selectable differential or single-ended output earpiece amplifier. It drives a 32 Ω dynamic earpiece (or a piezoearpiece).

2.8.3 Transmit Path Data Processing Functions

The TCM8030 data processing functions associated with the transmit path are performed by the following circuits as shown in Figure 2–2. A brief functional description is given for each circuit.

- TX BUFFER

The transmit buffer (TX BUFFER) buffers both narrowband and wideband data that is loaded from the five transmit-data word registers (TXD0 – TXD4, write addresses 10H–14H).

- WB-TX ENCODER

The wideband transmit data encoder circuit (WB-TX ENCODER) receives the data from the transmit buffer and performs all the necessary operations for both the reverse control channel (RECC) and reverse voice channel (RVC) data transmission. It calculates and adds BCH parity bits to the data, along with word sync and dotting. The data is repeated as specified for analog cellular. The wideband signaling tone (ST) is generated when required.

- NB-TX ENCODER

The narrowband transmit data encoder circuit (NB-TX ENCODER) calculates the BCH encoding parity bits from the data in the transmit buffer and adds the 30-bit synch word to synchronize the transmission of RVC data to the DSAT.

- DSATSW

The digital supervisory audio tone switch (DSATSW) selects either narrowband data or the output from the DSAT/DST GEN stage for application to the NB-DAT ATTEN stage. The fifth and sixth bits of the operational control word C1 (write address 00H) control the operation of the DSATSW. When bits 5 and 6 are set to zero, the switch connects to the NB-TX encoder input.

- WS/NBSW-a, -b, and -c

The wideband and narrowband switches (WB/NBSW -a through -c), grouped together, select either narrowband or wideband transmission operation. The switch position is controlled by the value in bit one of the operational control word C1 (write address 00H).

- DSAT/DST GEN

The digital supervisory audio tone/digital signaling tone generator (DSAT/DST GEN) circuit generates the narrowband DSAT and DST signals.

- NB-DAT ATTEN and WB-DAT ATTEN

These two circuits are fixed narrowband and wideband data attenuators (NB-DAT ATTEN AND WB-DAT ATTEN) that set a fixed attenuation to provide the correct data signal levels.

- TX-DAT TRIM

The transmit data trim circuit (TX-DAT TRIM) trims the DSAT, DST, and narrowband data levels.

- TX-DAT LPF

The transmit data low-pass filter circuit (TX-DAT LPF) provides low-pass switched-capacitor filtering of the DSAT and DST. It also transmits narrowband and wideband data to minimize output harmonics and correct narrowband transmitted data eye patterns.

2.8.4 Receive Path Data Processing Functions

The TCM8030 data processing functions associated with the receive path are performed by the following circuits as shown in Figure 2–2. A brief functional description is given for each circuit.

- WB-RX COMP

This wideband receive comparator circuit (WB-RX COMP) features built-in hysteresis to reject noise.

- WB-RX RECOVERY

This circuit performs the wideband data recovery function (WB-RX RECOVERY), including dotting.

- WORD SYNC

This circuit performs frame synchronization (WORD SYNC) recovery for the wideband data channel.

- NB-RX LPF

The narrowband receive data and low-pass filter circuit (NB-RX LPF) contains a low-pass switched-capacitor filter for filtering DSAT and audio signals. This circuit also includes a decimating antialiasing stage at the input.

- NB-RX COMP

The narrowband receive and DSAT comparator circuit (NB-RX COMP) features built-in hysteresis to reject noise.

❑ NB-RX RECOVERY

The narrowband data and DSAT recovery circuit (NB-RX RECOVERY) recovers the narrow-band data and DSAT components for application to the BCH decoder circuit.

❑ SYNC WORD DET

The sync word detect circuit (SYNC WORD DET) detects the narrowband data sync word.

❑ DSAT DET

The digital supervisory audio tone detector circuit (DSAT DET) monitors the narrowband receive recovery data for the DSAT signal.

❑ Majority voting

In wideband mode, each of the 40 receive data bits is majority voted. The number of repeats is read using the microcontroller interface.

❑ BCH decoder

The wideband and narrowband BCH decoder stage can correct up to two errors in the received signal and give a 4-bit error correction status report.

❑ RX BUFFER

The receive buffer (RX BUFFER) stage provides a buffer for both wideband and narrowband received data.

❑ RX CONTROL

The receive control (RX CONTROL) functional block controls the wideband/ narrowband receive data recovery and decoding stages. It splits the time-multiplexed busy/idle bits, chooses word A or B, and starts the majority vote and error correction processes, when required.

❑ ARBITRAT LOGIC

The arbitration logic circuit (ARBITRAT LOGIC) arbitrates wideband data busy/idle bits majority voting and outputs the results to the TXRFEN terminal.

❑ IDLE MODE LOGIC

The idle-mode logic circuit senses the microcontroller unit (MCU) idle mode and receive RF (RXRF) idle-mode functions, and applies an enable signal to the output terminal RXRFEN to control the internal power mode.

2.8.5 Transmit Path SAT Processing Functions

The TCM8030 supervisory audio tone (SAT) transmit-path processing functions are performed by the following circuits, as shown in Figure 2–2. A brief functional description is given for each circuit.

- SAT GEN/DET

The supervisory audio tone generator and detector (SAT GEN/DET) circuit is primarily a transponding digital phased-locked loop (PLL) circuit. It is used in wideband mode only. The circuit is an enhanced design that improves SAT sensitivity. SAT outputs can also be programmed without a SAT input to facilitate phone testing.

- SAT ATTEN

The supervisory audio tone attenuator (SAT ATTEN) circuit is a fixed attenuator used to set the correct TX SAT signal level.

- SAT TRIM

The supervisory audio tone trim (SAT TRIM) circuit sets the wide-band SAT level trim. Output from this circuit is applied to the TXSAT BPF antialiasing filter.

- TXSAT BPF

The transmit band-pass filter (TXSAT BPF) circuit is a switched-capacitor band-pass filter that performs antialiasing.

2.8.6 Receive Path SAT Processing Functions

The TCM8030 supervisory audio tone (SAT) receive-path processing functions are performed by the following circuits, as shown in Figure 2–2. A brief functional description is given for each circuit.

- RXSAT BPF

The receive band-pass filter (RXSAT BPF) circuit for the supervisory audio tone is a switched-capacitor band-pass filter.

- SAT COMP

The supervisory audio tone comparator (SAT COMP) circuit slices the received SAT signal before sending it to the SAT GEN/DET circuit. This circuit also contains built-in hysteresis to aid in noise rejection.

2.9 Miscellaneous Functions

The TCM8030 contains several circuits that perform specific functions as previously shown in Figure 2–2. A brief functional description is given for each circuit.

❑ Power-Off Logic

This function implements total power-down mode logic. In this mode, all internal circuits, including the XTALOSC, are disabled. The TCM8030 is the only device in the phone with its power supply enabled in this mode. Static power- up logic, implemented via one of the keyboard interrupt ports, waits for a pressed power-on key. Then TCM8030 exits total power-down mode, reactivates the oscillator, enables the regulators to the rest of the phone via EXTPWR, and holds $\overline{\text{EXTRST}}$ low for 0.1 to 0.2 second, to allow the rest of the phone to power up cleanly.

❑ TXVMID and RXVMID

The TXVMID and RXVMID functional blocks are separate transmit and receive analog-reference voltage generators. The circuits contain resistive dividers fed from analog voltage supplies. The outputs are buffered and then decoupled externally, to provide accurate, quiet, mid-rail reference to internal audio circuits.

❑ AFC

The AFC (automatic frequency control) circuit receives one input from an external TCXO (temperature-compensated crystal oscillator) and another input from the receiver IF (intermediate frequency) stage. The counters in this block then process the inputs and provide a count that can be read using the microcontroller interface.

❑ DAC 1–3

DACs 1–3 are each 8-bit linear digital-to-analog converters.

❑ AMP7

AMP7 is an uncommitted operational amplifier.

❑ DTMF GEN

The dual-tone multifrequency generator (DTMF GEN) circuit generates the tones for push-button dialing and provides the user-alert tone.

❑ Timer

The timer circuit is a programmable 8-bit counter. The timer can either count down once or cycle continuously. When the counter reaches zero, the output changes state.

- Watchdog timer

The watchdog timer circuit starts by writing to a location in the microcontroller interface. If the location is not written to again within the time-out period, the watchdog timer times out and the output changes state. This change in output resets the telephone microcontroller.

- PIO Port 1 and PIO Port 2

PIO Port 1 and PIO Port 2 are two 8-bit wide programmable ports. Each line of each port can be individually programmed as either an input or an output.

- Keyboard scan

The keyboard scan port is a 4-bit port that accepts inputs from a keyboard and generates interrupts to the microcontroller. The port can also be reconfigured as a general purpose I/O (input/output) port. One I/O terminal connected to the telephone ON/OFF key supplies a wake-up signal that terminates the total power-down mode.

- MICRO CONTRL I/F and INTRPT LOGIC

All wideband and narrowband data communications are transmitted to and received from the telephone microcontroller using the microcontroller interface (MICRO CONTRL I/F) circuitry. Internal data, command, and interrupt registers are programmed using the write operation. Other internal data, status, and interrupt registers are monitored using read operations.

Chapter 3

Receive Processing

This chapter describes the receive processing procedure for the forward control channel (FOCC) and the forward voice channel (FVC). In addition to a description of each mode, it includes examples that describe and illustrate the processing methodology.

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3.1 Receive Processing Overview

FOCC synchronization or FVC frame timing, and majority voting and data decoding occur during receive processing in the forward control channel (FOCC) and/or the forward voice channel (FVC), as noted above. Several read and write address registers control these processes, as illustrated in Table 3–1.

Table 3–1. Read/Write Address Information for Receive Processing

Name	Read/Write	Address	Bit	Description
FRAMESYNC	Write	0CH	N/A	Restart FRAMESYNC (data written not important) – resets the data recovery circuit to achieve bit synchronization to the received data
E2	Read	06H	3	Change in FOCC FRAME-SYNC status
E2	Read	06H	2	FVC FRAMESYNC achieved
S2	Read	01H	3	In FOCC FRAMESYNC
S2	Read	01H	2	FVC message being received
RXRPT	Read	22H	3–0	Number of word repeats used for majority voting – wideband
FRAMEMIS	Write	22H	2–0	Frame mismatch coefficient-wide-band

Note: E2 (bit 3) in FOCC mode and S2 (bit 2) in FVC mode can be monitored from device pin 25-SYNC.

FRAMESYNC (write address 0CH: data not significant) resets the data recovery circuit, which bit-synchronizes the received data. When the telephone switches to FOCC, FRAMESYNC reduces the wait time to acquire bit synchronization. As a result, the data recovery circuit does not have to wait until it detects loss of bit synchronization to change to fast-lock mode (coarse mode).

Device pin 25-SYNC monitors different events for FOCC and FVC modes.

- For the FOCC, event register 2 (read address 06H, bit 3) monitors changes in FRAMESYNC and applies them to device pin 25-SYNC.
- For the FOCC, when the *WS Expected* occurs a second time after the *WS Expected* reference, the FOCC is in FRAMESYNC. This is monitored in status word 2 (read address 01H, bit 3).
- For the FVC, event register 2 (read address 06H, bit 2) monitors FVCMSG and applies it to device pin 25-SYNC. FRAMESYNC is not externally accessible from the TCM8030.

- For the FVC, after the FVC dotting pattern is detected, when the first *WS Expected* occurs, the FVC message is being received. This is monitored in status word 2 (read address 01H, bit 2).
- RXRPT (read address 22H, bits 3–0) reports the number of repeats that were actually used during bit-wise majority voting.

Along with SYNC monitoring, there is also a FRAMEMIS write register that controls the number of allowable, missed word syncs before FRAMESYNC transitions from high back to low. The TCM8030 has a default value of FRAMEMIS = 5. Therefore, if five word synchronizations are missed, the FRAMESYNC is lost, and the resynchronization process reoccurs.

Note:

The default value for FRAMEMIS (FRAMEMIS = 5) is used as the reference in the following FOCC and FVC receive-processing examples. Also, E2 (bit 3) and S2 (bit 2) can be monitored from device pin 25-SYNC.

3.2 Forward Control Channel (FOCC) Receive Processing

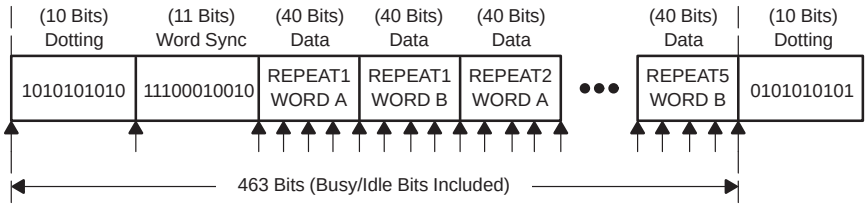
This section describes the algorithm used by the data processor to synchronize to a received message stream on the control channel in wideband mode.

3.2.1 Frame Description

Each data frame consists of several components. The frame begins with a dotting sequence (alternating 1s and 0s), continues with a word-sync pattern, and is followed by five repeats of word-A and word-B data. The base station forms each word by encoding 28 content bits into a (40, 28) BCH code. Figure 3–1 shows the detailed FOCC frame format, and Figure 3–2 shows the simplified FOCC frame format.

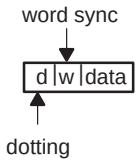
Busy/idle bits are also inserted into the FOCC frame format. The first is inserted at the beginning of the dotting sequence. The second is inserted at the beginning of the word sync, and the third is inserted at the end of the word sync. After the third busy/idle bit, a busy/idle bit is inserted every 10 bits through the five repeats of word-A and word-B data (Figure 3–1). The busy/idle bits indicate the control channel availability with the base station. An idle-to-busy transition coordinates messages sent on the control channel. This is monitored when the mobile station is attempting to transmit data over the RECC.

Figure 3–1. FOCC Frame Format



Note: Busy/idle bits are inserted in the bit stream at each arrow.

Figure 3–2. Simplified FOCC Frame Format



3.2.2 Synchronization

When the data processor switches into FOCC mode, it attempts to synchronize to the received data stream in the following manner:

1) The microcontroller places the data recovery PLL into coarse mode. This allows the PLL to shift by 180 degrees within five data edges. In this mode, the PLL attempts to lock onto any distinct data arriving at the AMPS/TACS data rate.

2) The RX controller evaluates the recovered data. When the controller recognizes the dotting pattern, the microcontroller places the PLL into fine mode where it can only shift a few degrees per cycle. FCCDOT (write address 23H) sets the number of dotting bits required before recognition occurs. The default value for this address is 07H.

3) The RX controller recognizes a word sync. With this recognition, the controller sets a timer that generates a *WS Expected* pulse exactly one frame later. If the next word sync arrives at the same time as *WS Expected*, then FOCC FRAMESYNC (status word 2: read address 01H bit 3) is raised to indicate the achieved synchronization. For the remainder of the frame, the PLL is frozen. When the dotting at the beginning of the next frame is expected, the PLL returns to fine mode, but only until the end of the dotting, where it freezes again.

FOCC FRAMESYNC enables evaluation of the received data. When FOCC FRAMESYNC is high, the RX controller decodes and reports on the frame data even if the dotting pattern or word sync is corrupted (corruption in the preamble does not mean that the data is bad). If word syncs do not occur for a specific number of frames indicated from the value in FRAMEMIS, FOCC FRAMESYNC transitions to low (no data is decoded) and the synchronization process, in steps 1–3 above, repeats.

3.2.3 Majority Voting

Majority voting occurs on all available data repeats in wideband mode. A 40×4 register contains a summation of all repeats of the 40 bits. When the register receives bit n of the current repeat, load the n^{th} slice of the register into a counter. If the received bit is 1, the counter increments. If the received bit is 0, the counter decrements. The counter can count from 0 to 7 or –7.

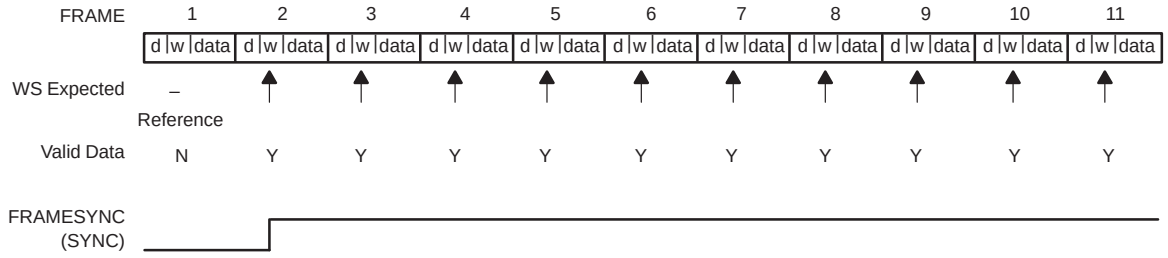
There are five data repeats in FOCC mode. A majority vote of three out of five words determines whether to eliminate the recognition of corrupted data. All five repeats are always loaded into the majority vote logic so there is always a positive or negative number assigned to the register and never zero.

3.2.4 Normal Operation

During a normal operation in FOCC mode (see Figure 3–3), FRAMESYNC (SYNC pin 25) transitions from low to high when *WS Expected* occurs during the second frame. With this transition, RX controller decodes the data from the second frame.

By checking that the first two word syncs occur at the correct time interval, you can eliminate false word syncs produced by noise. You can ignore the first frame of data because the data will be repeated or is for another user. Because *WS Expected* occurs in every additional frame, FRAMESYNC remains high, and RX controller decodes every frame of data.

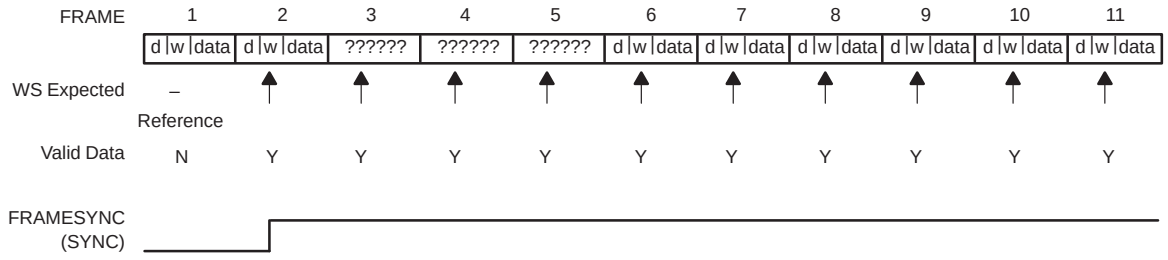
Figure 3–3. FOCC Normal Operation



3.2.5 Less Than Five Word Syncs Missing

In this FOCC case (see Figure 3–4), when the word sync occurs with *WS Expected* during the second frame, FRAMESYNC (SYNC pin 25) transitions from low to high. With this transition, RX controller decodes the second frame's data. It also decodes the third frame's data, but *WS Expected* does not occur. It continues to decode data through additional frames even though the word sync is corrupted. However, because there are not more than five word syncs missing, FRAMESYNC remains high.

Figure 3–4. FOCC Less Than Five Word Syncs Missing

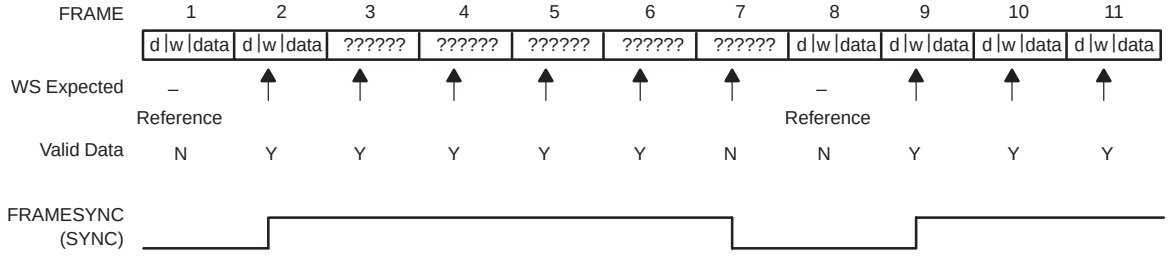


3.2.6 More Than Five Word Syncs Missing

Unlike the less than five word syncs missing case, in the more than five word syncs missing case (see Figure 3–5), FRAMESYNC transitions from high to

low. This transition follows the fifth case, where word sync does not occur with *WS Expected* (frame 7 for this case). At this point, the data is not valid and the process to find a new reference for *WS Expected* begins. FRAMESYNC transitions back to high when the word sync again corresponds to the *WS Expected*. In Figure 3–5, this occurs in frame 9.

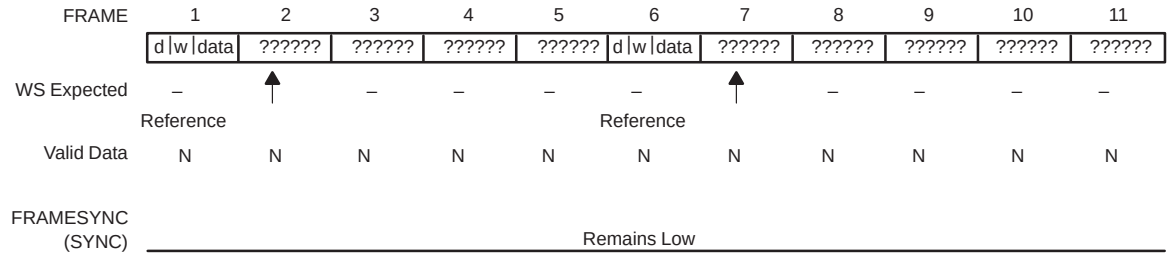
Figure 3–5. FOCC More Than Five Word Syncs Missing



3.2.7 Single Word Sync Detected

The final FOCC case (see Figure 3–6) occurs when FRAMESYNC detects only a single word sync. The reference for *WS Expected* occurs in frame 1, but word sync and *WS Expected* do not correspond in frame 2. As a result, the RX controller looks for a new reference for *WS Expected*. This occurs in frame 6, but word sync and *WS Expected* do not correspond in frame 7. Thus, for these two instances, FRAMESYNC does not transition from low to high, and the data, throughout the stream, is not valid.

Figure 3–6. FOCC Single Word Sync Detected



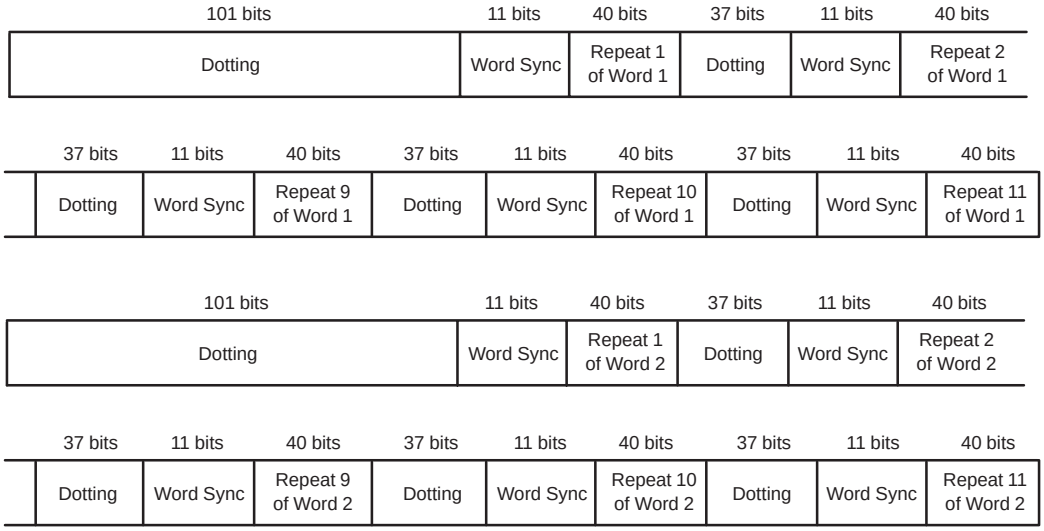
3.3 Forward Voice Channel (FVC) Receive Processing

This section describes the algorithm used by the data processor to synchronize to a received message stream on the voice channel in wideband mode.

3.3.1 Message Stream

The FVC message stream consists of components that synchronize incoming data and encode 28 bits of data into (40, 28) BCH code. Each word contains 40 bits (28 content bits and 12 parity bits) and is repeated 11 times, along with 37 bits of dotting and 11 bits of word sync. With the 40 BCH encoded bits, the left-most bit (earliest in time) of each word is the most significant bit (see Figure 3–7).

Figure 3–7. FVC Message Stream



3.3.2 Frame Timer

When the data processor switches into FVC mode, it attempts to identify the start of the frame in the following manner:

1) The microcontroller places the data recovery PLL into coarse mode. This allows the PLL to shift by 180 degrees within 5 data edges. In this mode, the PLL tries to lock onto any distinct data arriving at the AMPS/TACS data rate.

2) The RX controller evaluates the recovered data. When the controller recognizes the dotting pattern, the microcontroller places the PLL into fine

mode where it can only shift a few degrees per cycle. FVCDOT (write address 24H) sets the number of dotting bits required before recognition occurs. The default is 10H.

3) The RX controller recognizes the first word sync. Then it sets a timer that generates a *WS Expected* pulse exactly one frame later. If the next word sync arrives at the same time as *WS Expected*, then the FVC message being received (status word 2: read address 01H, bit 2) is raised (set high) to indicate the start of the frame. For the remainder of the frame, unless the RX controller requires frame resynchronization, the PLL is frozen.

Status word 2 bit 2 enables evaluation of the incoming repeats as described in the following sections. Status word 2 bit 2 transitions to low, again, after a fixed time interval equal to 11 frame repeats. The timer provides a master supervisory function and ensures that the circuit does not wait indefinitely.

3.3.3 Majority Voting

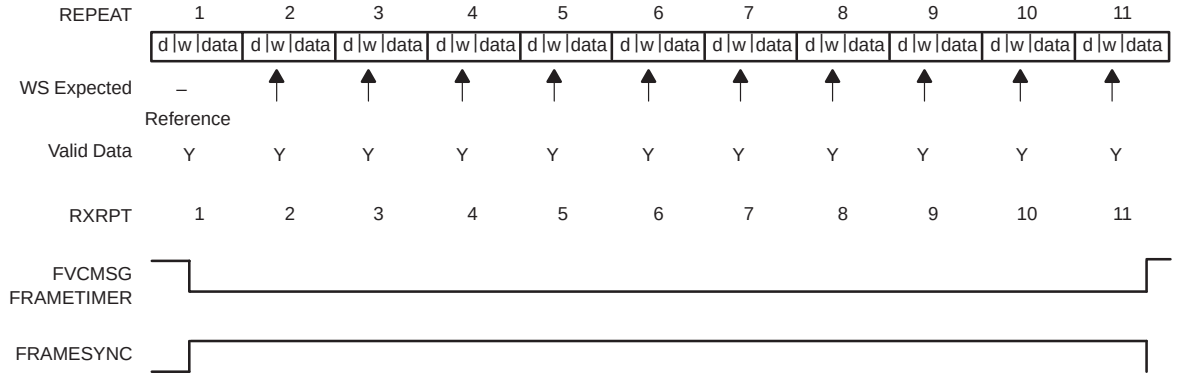
Majority voting occurs on all available data repeats in wideband mode. A 40×4 register contains a summation of all repeats of the 40 bits. When the register receives bit n of the current repeat, load the n^{th} slice of the register into a counter. If the received bit is 1, increment. If the received bit is 0, decrement. The counter can count from 0 to +7 or –7. When the counter reaches +/–7, it saturates.

After only one repeat, the sign bit of the 40×4 register indicates whether the received bit is a 0 or 1. After two or more repeats, the register contains a majority-voted value. Therefore, this design is totally flexible in the number of repeats it uses. If there is an even number of repeats and any one bit has an equal number of ones to zeros, the count in the 40×4 register is 0000. This is called an erasure. The number of erasures is reported in the BCH error correction status register (read address 13H, bits 0–3).

3.3.4 Normal Operation

During a normal operation in FVC mode (see Figure 3–8), status word 2, bit 2 is raised (set low), FRAMESYNC transitions from low to high when the RX controller encounters the first word sync, and the RXRPT value is subsequently incremented. With status word 2, bit set, the circuit sets the frame timer for a fixed time interval equal to 11 repeats. For every repeat, during the fixed time interval when FRAMESYNC is high, RXRPT (RX repeat count) is incremented and used for majority voting.

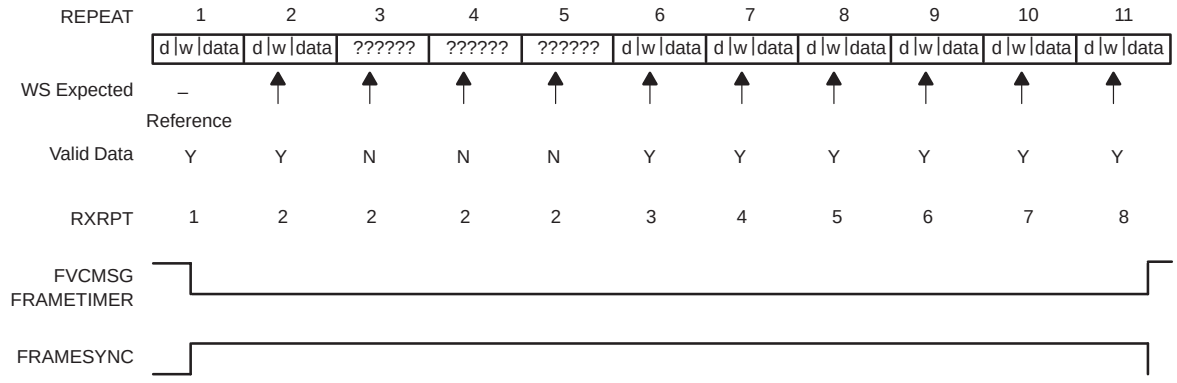
Figure 3–8. FVC Normal Operation



3.3.5 Less Than Five Word Syncs Missed

As with normal operation in FVC mode, in the less than five word syncs missed case (see Figure 3–9), status word 2, bit 2 is raised (set low), the FRAMESYNC transitions from low to high when the RX controller encounters the first word sync, and the RXRPT value is subsequently incremented. With status word 2, bit 2 set, the circuit sets the frame timer for a fixed time interval equal to 11 repeats. For every repeat during the fixed time interval, when the RX controller encounters a word sync pattern, RXRPT (RX repeat count) is incremented. In this case, repeats three, four, and five all contain a corrupted or invalid word sync pattern. For these repeats, the RXRPT value is not incremented.

Figure 3–9. FVC Less Than Five Word Syncs Missed

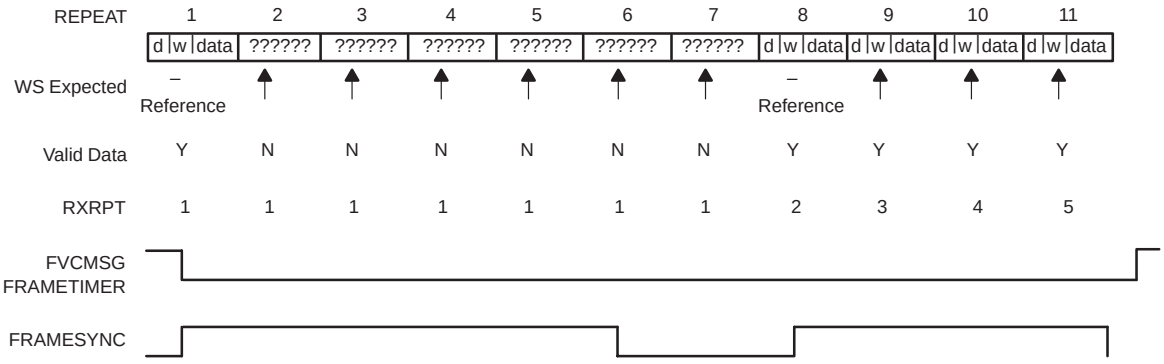


3.3.6 More Than Five Word Syncs Missed

As with normal operation in FVC mode, in the more than five word syncs missed case (see Figure 3–10), status word 2, bit 2 is raised (set low), FRAMESYNC transitions from low to high when the RX controller encounters the first word sync, and the RXRPT value is subsequently incremented. With status word 2, bit 2 set, the circuit sets the frametimer for a fixed time interval equal to 11 repeats. For every repeat during the fixed time interval, when the RX controller encounters a word-sync pattern, RXRPT (RX repeat count) is incremented.

In this case, repeats two, three, four, five, six, and seven all contain a corrupted word sync. For these repeats, the RXRPT value is not incremented. In addition, after the fifth missed word sync, FRAMESYNC transitions from high back to low and the frame synchronization process repeats. This means that the PLL can phase-adjust until it receives a dotting pattern. Then when the RX controller detects a word-sync pattern, the circuit resets the WS Expected timer. This procedure compensates for any phase shift in the incoming data.

Figure 3–10. FVC More Than Five Word Syncs Missed



3.3.7 One Word Received

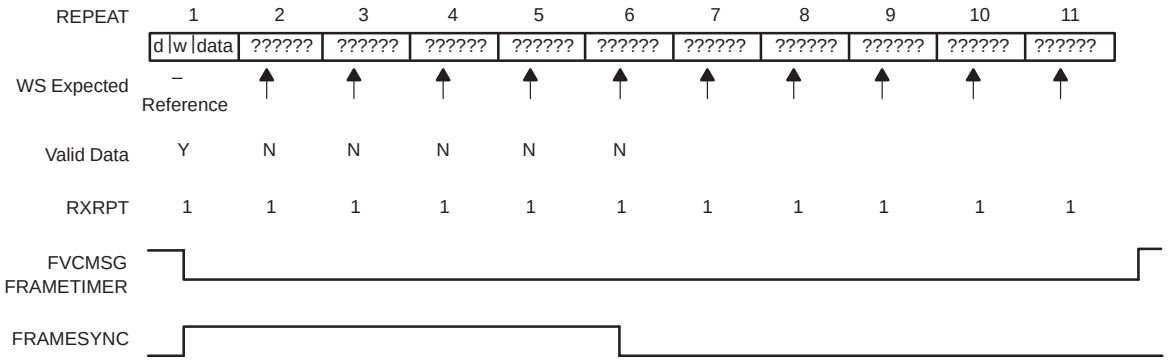
The one word received case (see Figure 3–11) indicates the worst possible situation. In this case, only one repeat is received. Either the first 10 repeats preceding the received repeat are missing or corrupted, or the 10 repeats immediately following are missing or corrupted.

As with normal operation in FVC mode, in this case, the status word 2, bit 2 is raised (set low) to indicate that a message is being received, FRAMESYNC transitions from low to high when the RX controller encounters the first word sync, and the RXRPT value is subsequently incremented. With status word 2, bit 2 set, the circuit sets the frame timer for a fixed time interval equal to 11 repeats.

With the RXRPT register containing a 1, you can test to determine if this is a worst-case situation. In this case, only one word is received. Therefore, after five missed word syncs, the FRAMESYNC transitions from high back to low, frame sync is lost, and the RX controller requires resynchronization (see Section 3.1, *Receive Processing Overview*).

When the frame timer terminates, BCH decodes the majority-voted data (in this case only one repeat) for error correction. Error correction takes between 30 and 80 cycles of the 2.56-MHz clock.

Figure 3–11. FVC One Word Received



Chapter 4

Wideband Data Reverse Channel Transmission Processing

This chapter provides AMPS wideband data reverse channel transmission processing procedures for both the reverse control channel (RECC) and reverse voice channel (RVC). Additionally, it describes each transmission processing mode, and provides word and message formats, with examples of RECC-called address encoding.

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4.3	Coded Digital Color Code (DCC)	4-4
4.4	RECC Word Format	4-5
4.5	Reverse Voice Channel Message Stream Description	4-6
4.6	RVC Word Format	4-7

4.1 Wideband Data Reverse Channel Transmission Processing Overview

Wideband transmission processing allows you to transmit responses, orders, and confirmations using the reverse control channel (RECC) and the reverse voice channel (RVC).

On the reverse control channel (RECC), a wideband data stream generated at 10k bits/s ±1 bit/second for AMPS standard is sent from the mobile station to the base station. The TCM8030 RECC message consists of from one to seven words for either single- or multiple-word transmissions. The message types sent over the RECC are as follows:

- Page response message
- Origination message
- Order confirmation message
- Order message

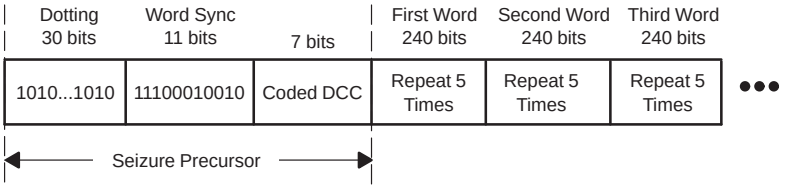
On the reverse voice channel (RVC), a wideband data stream generated at a 100 bit/s Manchester rate for AMPS standard is sent from the mobile station to the base station. The TCM8030 RVC message consists of from one to four words for single- or multiple-word transmissions. The message types sent over the RVC are as follows:

- Order confirmation message
- Called-address message
- Unique challenge order confirmation
- Base station challenge order message

4.2 Reverse Control Channel Message Stream Description

The reverse control channel (RECC) consists of several components. These components are illustrated in Figure 4–1.

Figure 4–1. RECC Message Stream



All messages begin with the RECC seizure precursor. The precursor contains 30 bits of dotting, 11 bits of word sync, and the 7-bit coded digital color code (DCC), as detailed in Table 4–1.

For a single word transmission, following the seizure precursor, a single RECC message word repeats five times. After the fifth repeat, the RECC message stream ends. For a mulitple-word transmission following the seizure precursor, the first RECC message word repeats five times, then the second RECC message word repeats five times, and then the third up to seventh RECC message word each repeats five times.

4.3 Coded Digital Color Code (DCC)

You obtain each coded digital color code by translating the received digital color code (see Table 4–1). You control the digital color code by writing to DCC/SAT/DSAT control word, bits 1 and 0 (write address 01H).

Table 4–1. Coded Digital Color Code

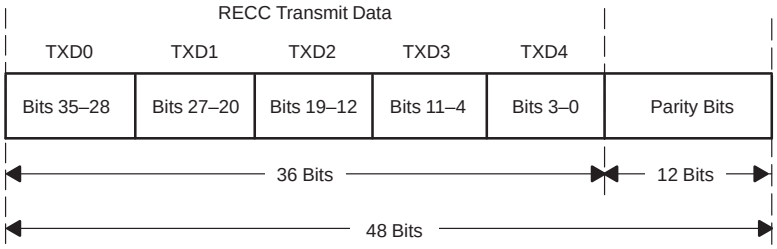
DCC/SAT/DSAT Control Word Write ADDRESS 01H		
Bit 1	**Bit 0**	**Transmitted Code**
0	0	0000000
0	1	0011111
1	0	1100011
1	1	1111100

4.4 RECC Word Format

The TCM8030 forms the RECC word by encoding 36 content bits into a (48, 36) BCH code. You set the transmit data content bit by writing to write addresses TXD0 (10H), TXD1 (11H), TXD2 (12H), TXD3 (13H), and TXD4 (14H). See the *TCM8030 Analog Baseband Data Manual* for details on writing data to the TCM8030.

The leftmost bit (earliest in time) is the most significant bit. The 36 most significant bits of the 48-bit field are the content bits (see Figure 4–2).

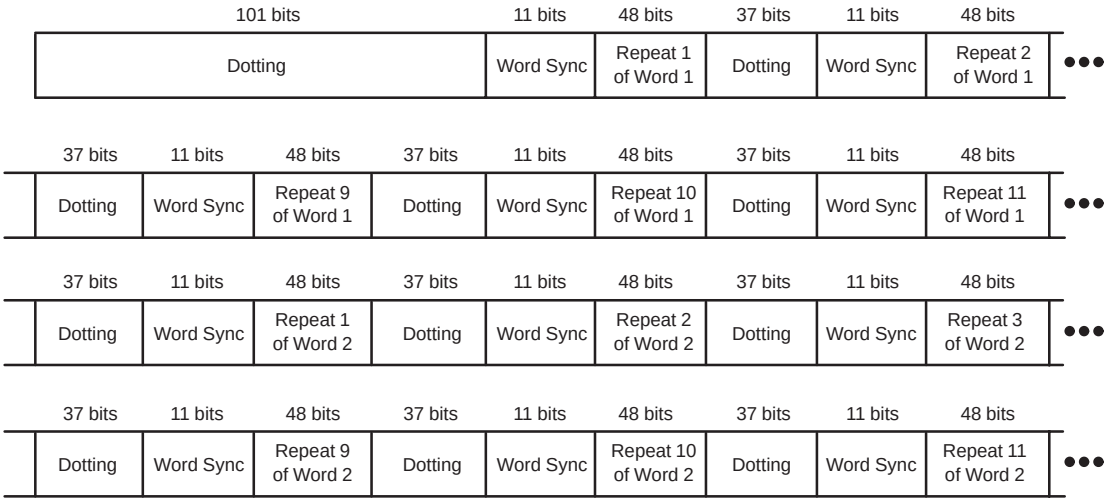
Figure 4–2. RECC Word Format



4.5 Reverse Voice Channel Message Stream Description

The reverse voice channel (RVC) consists of several components, with each word containing 48 bits (including parity). These components are illustrated in Figure 4–3.

Figure 4–3. RVC Message Stream



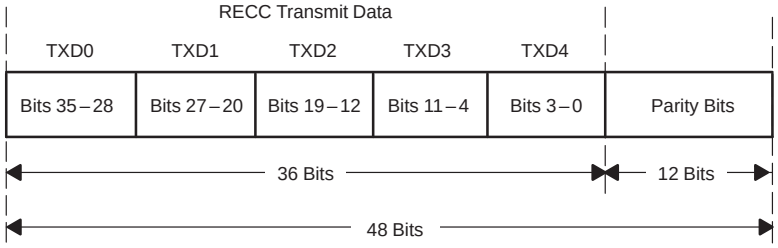
The RVC message stream begins with 101 bits of dotting and 11 bits of word sync. After this initial synchronization, word 1 repeats 11 times with 37 bits of dotting and 11 bits of word sync between every repeat. If a multiple word transmission occurs following the eleventh repeat of word 1, 37 bits of dotting (not a new 101 bits) and 11 bits of word sync occur. After the 37 bits of dotting and word sync, word 2 repeats 11 times, with 37 bits of dotting and 11 bits of word sync between every repeat.

4.6 RVC Word Format

The TCM8030 forms the RVC word in the same manner as the RECC word, by encoding the 36 content bits into a (48, 36) BCH code. As with the RECC word, you set the transmit data content bits by writing to write addresses TXD0 (10H), TXD1 (11H), TXD2 (12H), TXD3 (13H), and TXD4 (14H). See the *TCM8030 Analog Baseband Data Manual* for details on writing data to the TCM8030.

The leftmost bit (earliest in time) is the most significant bit. The 36 most significant bits of the 48-bit field are the content bits (see Figure 4–4).

Figure 4–4. RVC Word Format



Chapter 5

Wideband Data Transmission

This chapter describes TCM8030 wideband data transmissions and provides wideband data transmission examples for both the reverse control and reverse voice channels.

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5.1	Wideband Transmission Overview	5-2
5.2	Reverse Control Channel (RECC) Wideband Data Transmission	5-3
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5.1 Wideband Transmission Overview

The TCM8030 transmits wideband data on both the reverse control channel (RECC) and the reverse voice channel (RVC). In both cases, the TCM8030 Manchester-encodes and transmits the data at a rate of 10 kbits/second for AMPS standard. The message stream sent for the reverse control channel is illustrated in Figure 5–1. The message stream sent for the reverse voice channel is illustrated in Figure 5–2.

Figure 5–1. RECC Message Stream

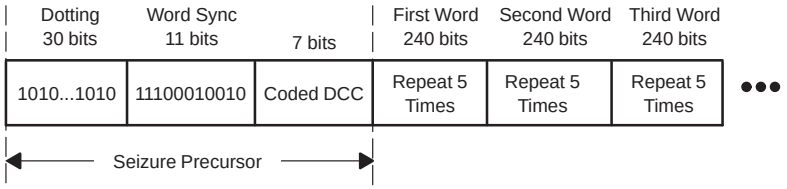
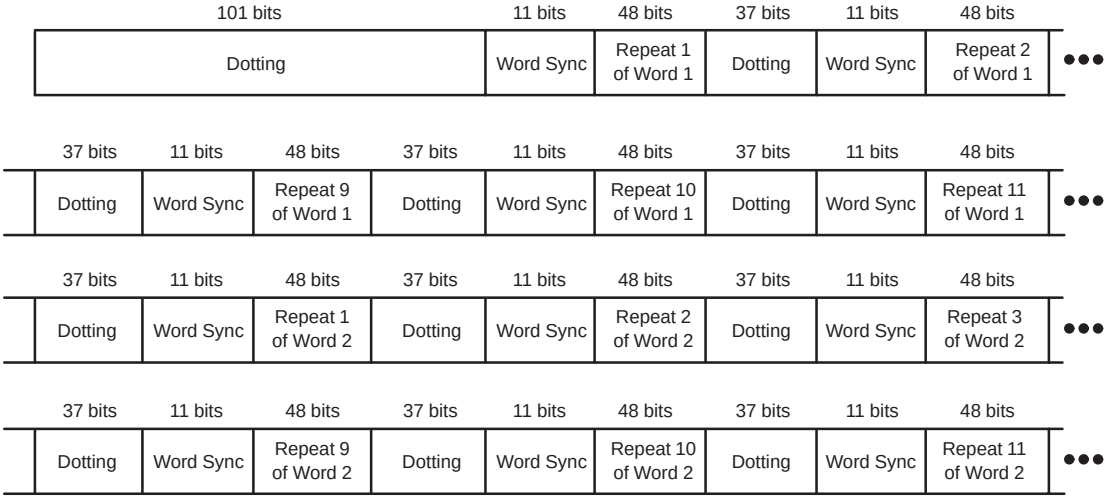


Figure 5–2. RVC Message Stream



5.2 Reverse Control Channel (RECC) Wideband Data Transmission

The reverse control channel can be formed for either single- or multiple-word transmissions. Depending on which is necessary, certain procedures need to be followed. These are described in the tables that follow.

5.2.1 Setup Procedures

When transmitting data on the reverse control channel, use the setup procedures detailed in Table 5–1.

Table 5–1. Setup Procedures for Wide-Band Data Transmission on RECC

Address	Data	Description
0×0D	0×00	Reset TCM8030 (Only use reset when initially powering on the phone — not at the beginning of every transmission — or use when it is necessary to reset the phone.)
0×00	0×01	C1 – AMPS, RECC
0×06	0×??	IE2, Enable necessary interrupts
0×03	0×15	C4, Full operation, DTMF off
0×05	0×??	IE1 – Enable necessary interrupts
0×33	0×18	TX voice, TX data enabled at TXSUM

Note: 0×?? indicates user selection of data.

5.2.2 Write to TX Buffer

Write WORD 1 data to TX buffer (TXD0–TDX4) as detailed in Table 5–2.

Table 5–2. Write to TX Buffer

Address	Data	Description
0×10	0×??	Write word 1, bits 35–28 to TXD0.
0×11	0×??	Write word 1, bits 27–20 to TXD1.
0×12	0×??	Write word 1, bits 19–12 to TXD2.
0×13	0×??	Write word 1, bits 11–4 to TXD3.
0×14	0×??	Write word 1, bits 3–0 (LSBs) to TXD4.

Note: 0×?? indicates user selection of data.

5.2.3 Commence Transmission

When the commence transmission executes, TCM8030 transmits the Manchester-encoded data on the control channel at a rate of 10 kbits/second for AMPS standard.

Table 5–3. Commence Transmission

Address	Data	Description
0×08	0×00	Initiate transmission.

5.2.4 Single-Word Transmission

Form the single-word-transmission data stream as follows:

1) 30 bits of dotting, 11 bits of word sync, 7 bits coded DCC, 240 bits (word 1 repeated five times)

2) Write to interrupt control word 1 (write address 05H, bit 3) to enable the transmission-complete interrupt. After the fifth repeat occurs, the transmission-complete interrupt generates on INTRPT (pin 2).

3) Read event 1 (E1, read address 05H) and event 2 (E2, read address 06H) to clear the interrupt.

4) After clearing, you may write a new word to the TX buffer for another single-word transmission.

5.2.5 Multiple-Word Transmission

When transmitting multiple words on the reverse control channel, use the same setup procedures as the single-word transmission, but use the TX buffer-available interrupt rather than the transmission-complete interrupt, as follows:

1) Write a one to interrupt control word 1 (write address 05H, bit 1) to enable the TX buffer-available interrupt.

2) After word 1 begins to transmit, an interrupt will appear on INTRPT (pin 2), indicating that the TX buffer is available.

3) Read event 1 (E1, read address 05H) and event 2 (E2, read address 06H) to clear the interrupt.

4) After clearing, begin writing word 2 to the TX data buffer.

A TX commence is not required after writing word 2 to the TX data buffer. This sequence is detailed in Table 5–4.

Table 5–4. Write to TX Buffer

Address	Data	Description
0×05	0×??	INTRPT event read address E1
0×06	0×??	INTRPT event read address E2
0×10	0×??	Write word 2, bits 35–28 to TXD0
0×11	0×??	Write word 2, bits 27–20 to TXD1
0×12	0×??	Write word 2, bits 19–12 to TXD2
0×13	0×??	Write word 2, bits 11–4 to TXD3
0×14	0×??	Write word 2, bits 3–0 (LSBs) to TXD4

Note: 0×?? indicates user selection of data.

To transmit word 3, follow the same procedure as indicated for word 2.

The following sequence continues the transmission after the fifth repeat of word 1:

1) 30 bits of dotting, 11 bits of word sync, 7 bits of coded DCC, 240 bits (word 1 repeated five times)

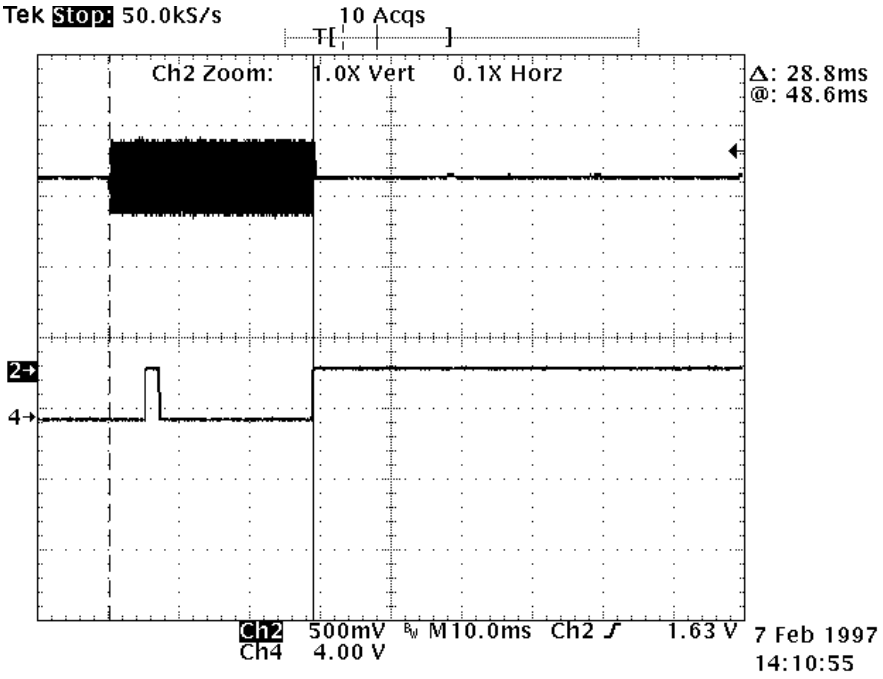
2) 240 bits (word 2 repeated five times)

3) 240 bits (word 3 repeated five times), etc.

5.2.6 Single-Word Transmission Example

An example of a RECC single-word transmission is illustrated in Figure 5–3.

Figure 5–3. RECC Wideband Data Transmission, Word 1



CH2 – TXO, CH4 – INTRPT

The time of the burst is as follows:

30 bits dotting, 11 bits word sync, 7 bits DCC,

240 bits (word 1, 5 repeats)

Total = 288 bits

Time (10 kbits/s AMPS transmission rate) = 28.8 ms

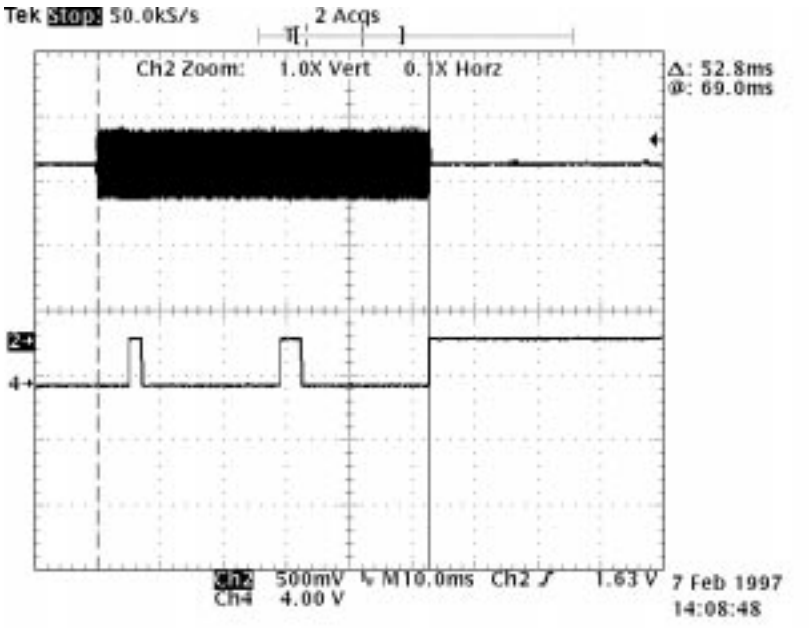
Note:

When INTRPT transitions to high the first time, this correlates to the TX data-buffer-available interrupt. When INTRPT transitions to high the second time, this correlates to the TX sequence-complete interrupt.

5.2.7 Multiple-Word Transmission Examples

Figure 5–4 and Figure 5–5 are examples of multiple-word transmissions.

Figure 5–4. RECC Wideband Data Transmission, Words 1 and 2 (Multiple-Word Transmission)



CH2 – TX0, CH4 – INTRPT

The time of the burst consists of the following:

30 bits dotting, 11 bits word sync, 7 bits coded DCC,

240 bits (word 1, 5 repeats), 240 bits (word 2, 5 repeats)

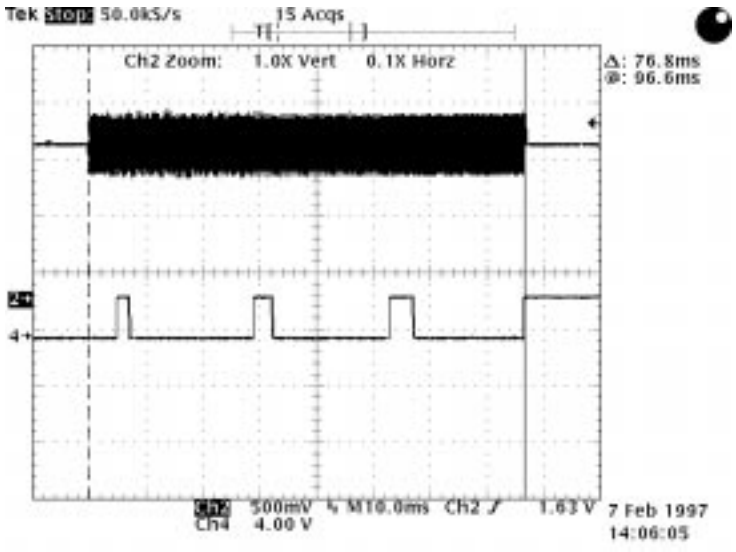
Total = 528 bits

Time (10 kbits/s AMPS transmission rate) = 52.8 ms

Note:

When INTRPT transitions to high the first and second times, this correlates to the TX data-buffer-available interrupt. When INTRPT transitions to high the third time, this correlates to the TX sequence-complete interrupt.

Figure 5–5. RECC Wideband Data Transmission, Words 1, 2, and 3 (Multiple-Word Transmission)



CH2 – TX0, CH4 – INTRPT

The time of the burst is as follows:

30 bits dotting, 11 bits word sync, 7 bits coded DCC,

240 bits (word 1, 5 repeats)

240 bits (word 2, 5 repeats)

240 bits (word 3, 5 repeats)

Total = 768 bits

Time (10 kbits/s AMPS transmission rate) = 76.8 ms

Note:

When INTRPT transitions to high the first, second, and third times, this correlates to the TX data-buffer-available interrupt. When INTRPT transitions to high the fourth time, this correlates to the TX sequence-complete interrupt.

5.3 Reverse Voice Channel (RVC) Wideband Data Transmission

The reverse voice channel can be formed for either single- or multiple-word transmissions. Depending on which is necessary, certain procedures need to be followed. These are described in the tables that follow.

5.3.1 Setup Procedures

When transmitting data on the reverse voice channel, use the setup procedures detailed in Table 5–5.

Table 5–5. Setup Procedures for Wideband Data Transmission on RVC

Address	Data	Description
0×0D	0×00	Reset TCM8030 (Only use reset when initially powering on the phone — not at the beginning of every transmission — or use when it is necessary to reset the phone)
0×00	0×05	C1 – AMPS, RVC
0×06	0×??	IE2, Enable necessary interrupts
0×03	0×15	C4, Full operation, DTMF off
0×05	0×??	IE1 – Enable necessary interrupts
0×33	0×18	TX Voice, TX data enabled at TXSUM

Note: 0×?? indicates user selection of DATA.

5.3.2 Write to TX Buffer

Write word 1 to TX buffer (TXD0–TDX4) as detailed in Table 5–6.

Table 5–6. Write to TX Buffer

Address	Data	Description
0×10	0×??	Write word 1, bits 35–28 to TXD0
0×11	0×??	Write word 1, bits 27–20 to TXD1
0×12	0×??	Write word 1, bits 19–12 to TXD2
0×13	0×??	Write word 1, bits 11–4 to TXD3
0×14	0×??	Write word 1, bits 3–0 (LSBs) to TXD4

Note: 0×?? indicates user selection of data.

5.3.3 Commence Transmission

When the commence transmission executes, the TCM8030 transmits the Manchester-encoded data on the voice channel at a rate of 10 kbits/second for AMPS standard.

Table 5–7. Commence Transmission

Address	Data	Description
0×08	0×00	Initiate transmission

5.3.4 Single-Word Transmission

Use the following procedure for single-word transmissions:

1) Form the single-word-transmission data stream as follows:
   a) 101 bits of dotting, 11 bits of word sync, 48 bits (first repeat of word 1)
   b) 37 bits of dotting, 11 bits of word sync, 48 bits (second repeat of word 1)
   c) 37 bits of dotting, 11 bits of word sync, 48 bits (third repeat of word 1)
   d) 37 bits of dotting, 11 bits of word sync, 48 bits (fourth repeat of word 1)
   e) 37 bits of dotting, 11 bits of word sync, 48 bits (fifth repeat of word 1)
2) Write a one to interrupt control word 1 (write address 05H, bit 3) to enable the transmission complete interrupt. After the fifth repeat occurs, the transmission complete interrupt generates on INTRPT (pin 2).
3) Read event 1 (E1, read address 05H) and event 2 (E2, read address 06H)) to clear the interrupt. After clearing, you may write a new word to the TX buffer for another single-word transmission.

5.3.5 Multiple-Word Transmission

When transmitting multiple words on the reverse voice channel, use the same setup procedures as the single-word transmission, but use the TX buffer-available interrupt rather than the transmission-complete interrupt.

1) Write a one to interrupt control word 1 (write address 05H bit 1) to enable the TX buffer-available interrupt. After word 1 begins to transmit, an interrupt will appear on INTRPT (pin 2), indicating that the TX buffer is available.
2) Read event 1 (E1, read address 06H) and event 2 (E2, read address 06H) to clear the interrupt.
3) Begin writing word 2 to the TX data buffer.

A TX commence is not required after writing word 2 to the TX data buffer. This sequence is detailed in Table 5–8.

Table 5–8. Write to TX Buffer

Address	Data	Description
0×05	0×??	INTRPT Event Read Address E1
0×06	0×??	INTRPT Event Read Address E2
0×10	0×??	Write word 2, bits 35–28 to TXD0
0×11	0×??	Write word 2, bits 27–20 to TXD1
0×12	0×??	Write word 2, bits 19–12 to TXD2
0×13	0×??	Write word 2, bits 11–4 to TXD3
0×14	0×??	Write word 2, bits 3–0 (LSBs) to TXD4

Note: 0×?? indicates user selection of data.

To transmit word 3, follow the same procedure as indicated above for word 2.

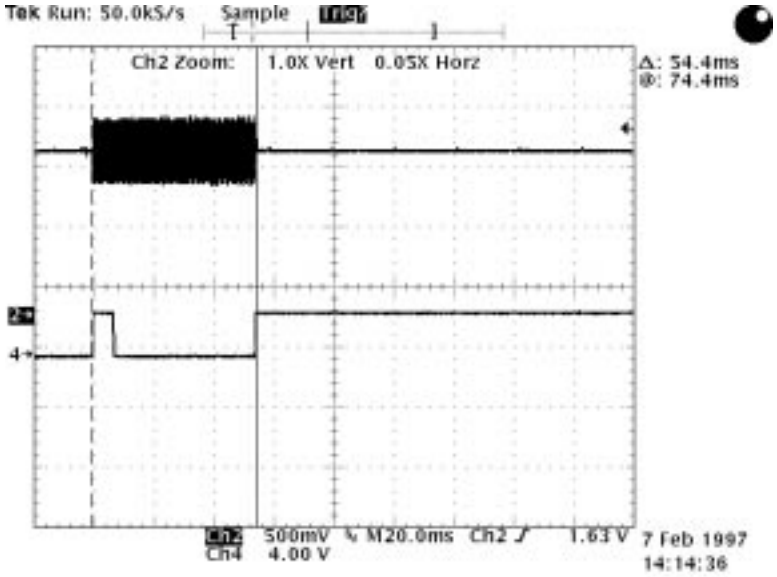
The following continues the transmission after the fifth repeat of word 1:

1) 48 bits (fifth repeat of word 1)
2) 37 bits of dotting, 11 bits of word sync, 48 bits (first repeat of word 2)
3) 37 bits of dotting, 11 bits of word sync, 48 bits (second repeat of word 2)
4) 37 bits of dotting, 11 bits of word sync, 48 bits (third repeat of word 2)
5) 37 bits of dotting, 11 bits of word sync, 48 bits (fourth repeat of word 2)
6) 37 bits of dotting, 11 bits of word sync, 48 bits (fifth repeat of word 2)

5.3.6 RVC Single-Word Transmission Example

An example of a RVC single-word transmission is illustrated in Figure 5–6.

Figure 5–6. RVC Wideband Data Transmission, Word 1



CH2 – TXO, CH4 – INTRPT

The time of the burst is as follows:

101 bit dotting, 11 bits word sync, 48 bits repeat 1 word 1,

(37 bits dotting, 11 bits word sync, and 48 bits word 1) × 4 repeats

Total = 544 bits

Time (10 kbits/s AMPS transmission rate) = 54.4 ms

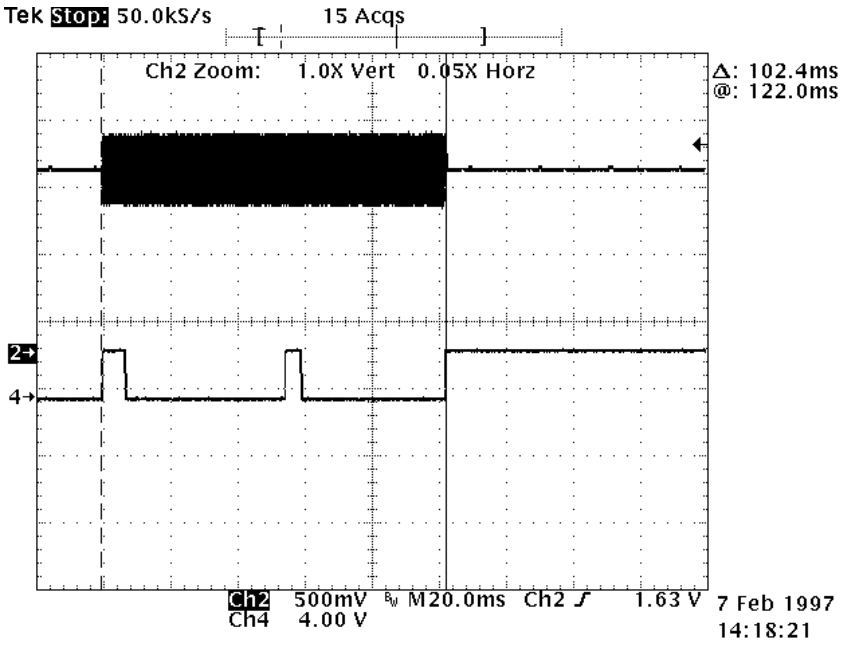
Note:

When INTRPT transitions to high the first time, this correlates to the TX data-buffer-available interrupt. When INTRPT transitions to high the second time, this correlates to the TX sequence-complete interrupt.

5.3.7 RVC Multiple-Word Transmission Examples

Figure 5–7 and Figure 5–8 are examples of multiple-word transmissions.

Figure 5–7. RVC Wideband Data Transmission, Words 1 and 2 (Multiple-Word Transmission)



CH2 – TXO, CH4 – INTRPT

The time of the burst is as follows:

101 bits dotting, 11 bits word sync, 48 bits repeat 1 word 1,

(37 bits dotting, 11 bits word sync, and 48 bits word 1) × 4 repeats,

(37 bits dotting, 11 bits word sync, and 48 bits word 2) × 5 repeats

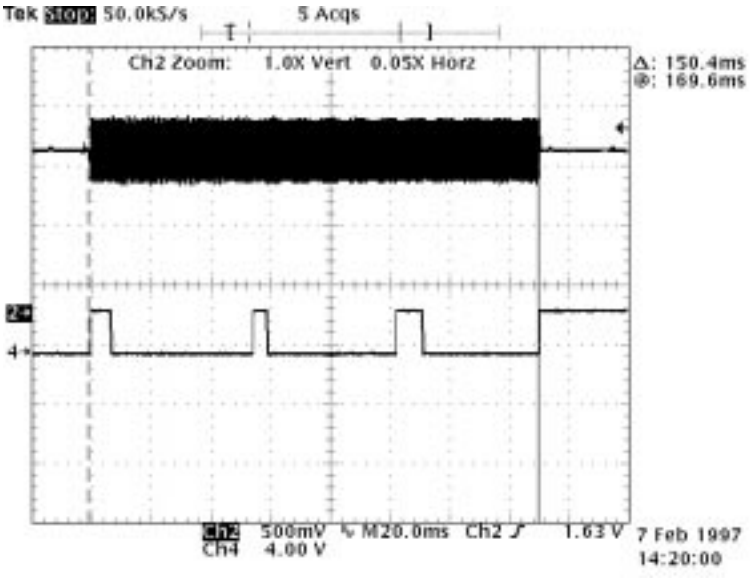
Total = 1024 bits

Time (10 kbits/s AMPS transmission rate) = 102.4 ms

Note:

When INTRPT transitions to high the first and second times, this correlates to the TX data-buffer-available interrupt. When INTRPT transitions to high the third time, this correlates to the TX sequence-complete interrupt.

Figure 5–8. RVC Wideband Data Transmssion, Words 1, 2, and 3 (Multiple-Word Transmission)



CH2 – TX0, CH4 – INTRPT

The time of the burst is as follows:

101 bits dotting, 11 bits word sync, 48 bits repeat 1 word 1,

(37 bits dotting, 11 bits word sync, and 48 bits word 1) × 4 repeats

(37 bits dotting, 11 bits word sync, and 48 bits word 2) × 5 repeats

(37 bits dotting, 11 bits word sync, and 48 bits word 3) × 5 repeats

Total = 1504 bits

Time (10 kbits/s AMPS transmission rate) = 150.4 ms

Note:

When INTRPT transitions to high the first, second and third times, this correlates to the TX data-buffer-available interrupt. When INTRPT transitions to high the fourth time, this correlates to the TX sequence-complete interrupt.

5.4 Wideband Data Transmission Precautions

The TCM8030 wideband data transmission operates as designed. However, unless you use the correct procedures, the device may not behave as expected. If transmitting one word of data, use the TX sequence-complete interrupt before sending a second burst. This ends the message stream for the first word before any additional message streams start.

If transmitting multiple words, use the TX buffer-available interrupt to indicate that the TX buffer is available. The TX buffer-available interrupt allows multiple words to occur in a single-transmission message stream, in accordance with the IS-91 Mobile Station – Base Station Compatibility Standard for 800-MHz Analog Cellular.

After you observe this interrupt, clear the interrupt event registers (IE1 and IE2). After clearing, you can write bits 35–0 to the data buffers (TXD0–TXD4). In either the RECC or RVC, the proper transmission of word 2 begins after the last repeat of word 1, *without* the need for a new commence transmission. If you use the commence transmission, the formatting of the message stream will restart and corrupt prior data.

In addition to performing a RECC transmission using the TCM8030, consider the channel seizure procedure that the mobile station must follow to ensure a correct seizure. This procedure is covered in Chapter 6, *Reverse Control Channel Arbitration Processing*.

Chapter 6

Reverse Control Channel Arbitration Processing

This chapter describes the process and methods used during reverse control channel arbitration.

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6.1	Reverse Control Channel Arbitration Processing Overview	6-2
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6.1 Reverse Control Channel Arbitration Processing Overview

During RECC transmission, the TCM8030 monitors the FOCC to determine if a busy/idle bit transitions to busy in a predefined window. This window occurs 0.8 ms following the RECC seizure precursor, through 5.6 ms after seizure. If a transition from idle to busy occurs in this window, the transmission continues. If the transition occurs before or after this window, the transmission ends. See Figure 6–1 and Figure 6–2 for the RECC and FOCC message streams.

Figure 6–1. RECC Message Stream (Arbitration)

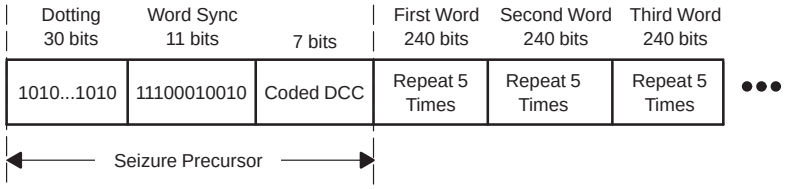
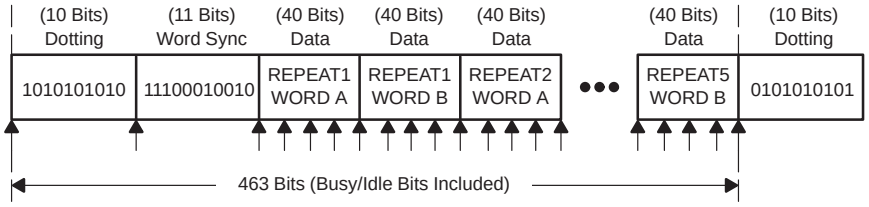


Figure 6–2. FOCC Message Stream



Note: Busy/idle bits are inserted in the bit stream at each arrow.

6.2 RECC Arbitration Methods

Several methods may be implemented during RECC arbitration processing.

6.2.1 Software Control Arbitration

Control word 1 (write address 00H, bit 4): Writing 0 to this address places arbitration processing under software control. In this case, when arbitration failure occurs, event register 1 (read address 05H, bit 2) and status register 1 (read address 00H, bit 2) indicate failure. In addition, if interrupt control register 1 (write address 05H, bit 2) is 1, an interrupt generates on INTRPT (TCM8030 device pin 2).

6.2.2 Hardware Control Arbitration

Control word 1 (write address 00H, bit 4): Writing one to this address performs two functions. First, it enables software control arbitration, as defined above. Second, it disables TXRFEN and TXO when arbitration failure occurs. Only an arbitration reset (write address 0EH) can re-enable TXRFEN.

Control word 3 (write address 02H, bit 2): Controls the signal polarity of TXRFEN and RXRFEN (Only TXRFEN applies to arbitration failure)

- Write address 02H (bit 2) = 0: Active high (low indicates arbitration failure, see the following note)

Note:

Since TXRFEN and RXRFEN are open-drain drivers with active pulldown resistors**,** you must apply an external pullup resistor to pull the TXRFEN and RXRFEN signals high.

- Write address 02H (bit 2) = 1: Active low (high indicates arbitration failure)

6.2.3 One or Two Busy/Idle Bits Observed

Control word 5 (write address 04H, bit 0): Controls the number of busy/idle bits observed.

- Write address 04H (bit 0) = 0: One busy/idle bit observed. The window occurs from RECC TX bit 56 to bit 104.

- Write address 04H (bit 0) = 1: Two busy/idle bits are observed in arbitration processing. This requires the window to move 10 bits. This window occurs from RECC TX bit 66 to bit 114, due to the first busy bit indicated 10 bits prior to the second busy bit.

Monitoring the busy/idle bit transition using two busy/idle bits is more accurate than monitoring the transition with one. It reduces the occurrence of FOCC random glitches that erroneously indicate a busy state when there actually is none.

Chapter 7

Automatic Frequency Control

This chapter defines automatic frequency control and its system cycle.

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7.2	AFC Reference	7-3
7.3	AFC System Concept	7-4
7.4	AFC Sample Cycle Detailed Description	7-5

7.1 Automatic Frequency Control Overview

The TCM8030 provides the internal circuitry for automatic frequency control (AFC) of an external temperature-compensated crystal oscillator (TCXO). AFC reduces any error in the TCXO frequency so that in a closed-loop system, the relative frequency of the TCXO adheres to the IF frequency requirement. The TCXO frequency must have minimal frequency errors: many components and circuits within a mobile phone, such as frequency synthesizers, microcontrollers, and data processors, are referenced to this frequency.

7.2 AFC Reference

The second IF frequency of the mobile phone receive section is the reference for the AFC circuitry. The second IF frequency is derived from the receive RF (RXRF) signal. This signal is generated at the cell base station using frequency references with tolerances less than 1 ppm. Because TCXO-referenced synthesizers derive the second IF frequency from the RXRF signal, TCXO frequency deviations can be corrected using a closed-loop system.

7.3 AFC System Concept

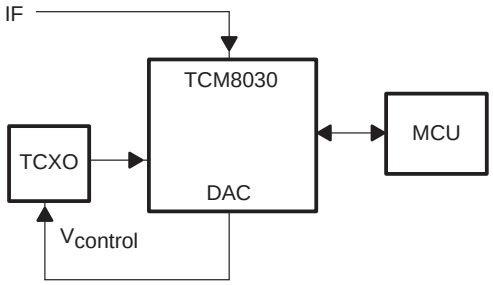
Figure 7–1 shows a TCXO, a microcontroller unit (MCU), and the TCM8030. The IF frequency reference and the TCXO connect to the IF and TCXO terminals of the TCM8030, respectively. Using counters and registers internal to the TCM8030, the MCU obtains a 20-bit AFC sample result following a MCU- initiated AFC cycle.

The MCU determines the TCXO frequency (within a resolution of 500 Hz typical) from the result of the AFC cycle. Once the MCU determines the TCXO frequency error sign and magnitude, the TCXO control voltage offset and gain parameters determine the control voltage necessary to correct the TCXO frequency error.

Once the MCU determines the control voltage for the TCXO, the MCU loads an appropriate coefficient into the digital-to-analog converter (DAC) register. With the DAC enabled and programmed, the error-correcting TCXO control voltage is present at the DAC output terminal, to correct the TCXO frequency.

This process can be repeated on a periodic basis as needed.

Figure 7–1. AFC Closed-Loop System Block Diagram



7.4 AFC Sample Cycle Detailed Description

After the MCU writes the 4-bit AFCTERM (corresponding to an AFCTERM VALUE) and sends the AFCSTART bit to the TCM8030, the 20-bit AFC terminal count read register clears and samples the IF signal for a given sampling period based on the TCXO frequency. Calculate this sampling period as shown in Equation 7–1.

Equation 7–1.

$$T_{SAMPLE} = (T_{TCXO} \times 2^{20} \times AFCTERM)$$

Note:

T_{SAMPLE} = sample period, T_{TCXO} = TCXO period, AFCTERM – decimal value applied.

Upon completing this sampling period, the TCM8030 stops the 20-bit AFC terminal count, sets the AFC event bit (E2: read address 06, bit 7) assuming the AFC interrupt bit (IE2: write address 06, bit 7) is enabled, and writes the result to the 20-bit AFC terminal count read registers – AFCIF1, AFCIF2, and AFCIF3 (read addresses 43–45). Upon completion of the AFC terminal count, the TCM8030 sets the AFCSTART bit to low. This stops the count but does not clear the registers. The MCU reads AFCIF1, AFCIF2, and AFCIF3. This read operation resets the counters. The value in the AFCIF1, AFCIF2 and AFCIF3 registers determines the current TCXO frequency, and the MCU makes adjustments in the closed-loop setup to correct the TCXO. Calculate the TCXO value as shown in Equation 7–2.

Equation 7–2.

$$TCXO = (IF \times 2^{20} \times AFCTERM)/(20\text{-}bit\ AFC\ Terminal\ Count)$$

Note:

TCXO and IF are measured in Hertz, and AFCTERM and the 20-bit AFC terminal count are decimal values translated from hex values. Figure 7–2 shows the system setup of the AFC within the TCM8030.

Figure 7–2. AFC Diagram

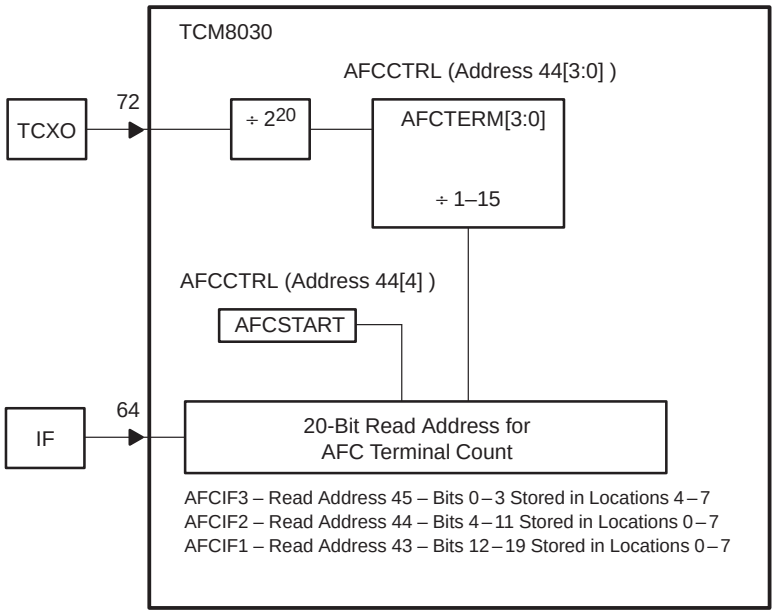


Table 7–1 describes the AFC 20-bit terminal count read address control execution.

Table 7–1. AFC 20-Bit Terminal Count Read Address Control Execution

Operation	Description
Apply IF signal (450-kHz typical value), apply TCXO signal, 14.85-MHz typical value.	
Write to address 31H–0×04.	Enables CLKOUT terminal to verify TCXO signal entering AFC circuitry. CLKSEL must be tied high externally to observe TCXO on CLKOUT. This is only for observation purposes and does not have to be implemented for AFC operation (see Note 3).
Write to address 06H (bit 7).	Enables AFC interrupt by writing 1 to bit 7
Write to address 44H (bits 0–3).	Sets AFCTERM = 0×?? (see Note 2)
Write to address 44H (bit 4).	AFCSTART = 1 starts AFC count/AFCSTART = 0 stops AFC count (see Note 1).
AFC terminal count begins.	
AFC terminal value reached.	Resets AFCSTART.
AFC terminal count is written to AFCIF1, AFCIF2, and AFCIF3.	
AFC has reached terminal count interrupt.	Event interrupt (read address 06H bit 7) is set and INTRPT (device pin 2) is generated.
Microcontroller reads the 20-bit AFC terminal count.	Reads in the following order at addresses 43 (8-bit), 44 (8-bit), and 45 (4-bit, bits 4–7).
Apply this AFC terminal count read address to Equation 2 to verify TCXO frequency.	

Notes: 1) For AFC execution to commence, IFAMP must be enabled – write address 30 H (bit 4).

2) The AFCTERM 4-bit register can range from 1 to 15 (01H to 0FH). The TCXO frequency can be resolved with one AFC sample period (AFCTERM = 1). Multiples of one AFC sample period can be used to find an average TCXO frequency error by setting the AFCTERM to a value greater than one.

3) In this case, TCXO is also the TCM8030 clocking scheme. CLKSEL must be high, and the TCXO frequency must be one of those indicated in Table 2–2. If TCXO is not selected as the TCM8030 clocking scheme, another scheme must be selected with CLKSEL low. Then the AFC circuit can operate with any frequency less than 20 MHz. See Section 2.6, *Clocks*, for additional clocking scheme information.

Chapter 8

Keyboard Interface and Set Monitoring

This chapter provides basic information regarding the programmable expansion input/output (I/O) ports PIO3, PIO2, and PIO1. It also describes the special function port keys 3–0 of the PIO3 I/O port, as well as supplies read and write register definitions and a microcontroller and keyboard interfacing diagram.

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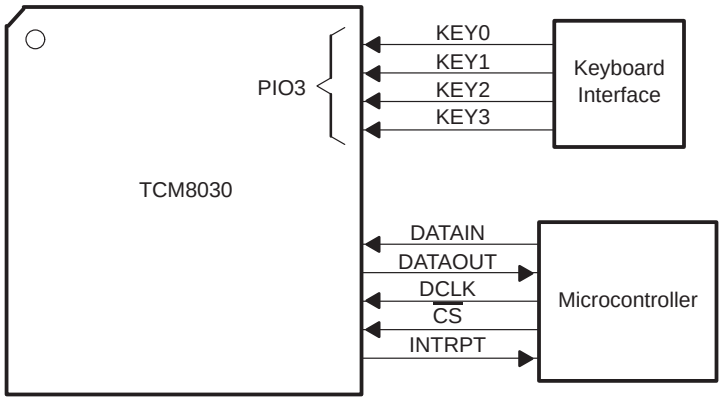
8.3	**TCM8030 8-Bit Programmable Expansion I/O Ports**	**8-5**

8.1 Keyboard Interface and Set Monitoring Overview

The TCM8030 has several programmable I/O ports that enable simple interfacing with the keyboard and monitoring of the cellular handset. PIO1 and PIO2 are two 8-bit digital programmable expansion I/O ports that can be programmed as either inputs or outputs. PIO3 is a 4-bit port that can be used as either a digital keyboard interrupt input [KEY3:KEY0] or a digital programmable expansion I/O port.

Keys 3–0 allow you to monitor the keyboard to ensure that when the power button is pressed, the TCM8030 wakes from total power-down mode. For more information, see Section 2.7, *Power Modes*, and Figure 8–1 below.

Figure 8–1. TCM8030 Keyboard and Microcontroller Interface



Note:

You need only connect one PIO3 terminal to the telephone ON/OFF key in order to supply the wake-up signal that terminates the total power-down mode. The remaining three terminals can be reconfigured as general-purpose I/O ports.

8.2 Keyboard Interrupt Inputs [KEY3:KEY0]

You can implement the TCM8030 PIO3 programmable I/O port as a keyboard interrupt input. Write to the PIO control word, PIOC3 (address 19H), which sets up the PIO3 direction (input/output). After the direction initializes as an input, set the PIO3 pullup control, PI3PULL (address 1BH). Finally, to send an interrupt to the microcontroller when the keyboard power-on button is on, set the PIO3 interrupt control PI3INT (address 1CH) as an interrupt port. This interrupt will occur on event register 2, E2 (read address 06H, bit 6).

Write to interrupt control word 2 (IE2: write address 06H, bit 6) to enable the PIO3 input-port sensed signal interrupt to appear on INTRPT (TCM8030 device terminal 2).

8.2.1 PIO Control Word (PIOC3 – Write Address 19H)

PIOC3 selects whether PIO3 is an input or an output as shown in Table 8–1. In order to use PIO3 as the keyboard scan, you need to define PIO3 as an input.

Table 8–1. PIO Control Word – PIOC3

Value	Corresponding Terminal Function
0	Input
1	Output

8.2.2 PIO3 Pullup Enabling (PI3PULL – Write Address 1BH)

When set to one, bits 0 to 3 of this register activate small pullup transistors that drive inputs using open-drain drivers. After a reset, the ports (PIO3) configure as inputs and the pullup transistors are enabled.

8.2.3 PIO3 Interrupt Control (PI3INT – Write Address 1CH)

PI3INT serves two purposes. First, PI3INT bits 0–3 set an interrupt when a signal is sensed on PIO3. Second, PI3INT bits 4–7 set the polarity of the interrupt (active high or active low). See Table 8–2 and Table 8–3 below.

Table 8–2. PIO3 Interrupt Control (PI3INT, Bits 3–0) Definition

PI3INT Bit (0–3)	Function
0	PIO3 operates as a normal port.
1	Signal sensed on PIO3 causes interrupt when IE2.6 is high.

Table 8–3. PIO3 Interrupt Control (PI3INT, Bits 7–4) Definition

PI3INT Bit (4–7)	Function
0	Active low interrupt
1	Active high interrupt

8.2.4 Event Register 2 (E2 – Read Address 06) Bit 6

The E2 register is eight bits wide and maintains the status of certain interrupt flags. For the PIO3 input-sensed signal, this status is E2 – bit 6. These flags indicate which events occurred since the previous read transaction, regardless of their associated interrupt control bits. The microcontroller must read E2 after E1 because of protocol for queuing and clearing events. The event registers clear following a read transaction. Since there are two registers, the following protocol occurs:

1) The microcontroller addresses E1.

2) The INTRPT terminal goes low, the contents of both interrupt registers transfer to buffers, and the registers clear to catch new events.

3) The serial microcontroller interface clocks out the buffered event information.

4) Any new events are caught in the main interrupt register; however, at this time INTRPT remains low.

5) The microcontroller addresses E2.

6) The buffered E2 information, caught in step 2, clocks out.

7) Once the read transaction is complete, INTRPT goes high if any interrupts occurred during steps 2 through 6. The event register now contains all events that occurred during the read transaction.

8.3 TCM8030 8-Bit Programmable Expansion I/O Ports

TCM8030 has two 8-bit expansion ports that can be programmed as either inputs or outputs.

8.3.1 PIO Control Words (PIOC1 and PIOC2 – Write Address 15H and 17H)

PIOC1 and PIOC2 select PIO1 and PIO2 terminals as either inputs or outputs as shown in Table 8–4.

Table 8–4. PIO Control Words – PIOC1 and PIOC2

Value	Corresponding Terminal Function
0	Input
1	Output

8.3.2 PIO Output Words (PIO1 and PIO2 – Write Address 16H and 18H)

PIO1 and PIO2 set the state of PIO terminals configured as outputs.

Chapter 9

Typical Analog Cellular Telephone Processing

This chapter describes the baseband processing techniques to apply necessary external circuitry to the TCM8030.

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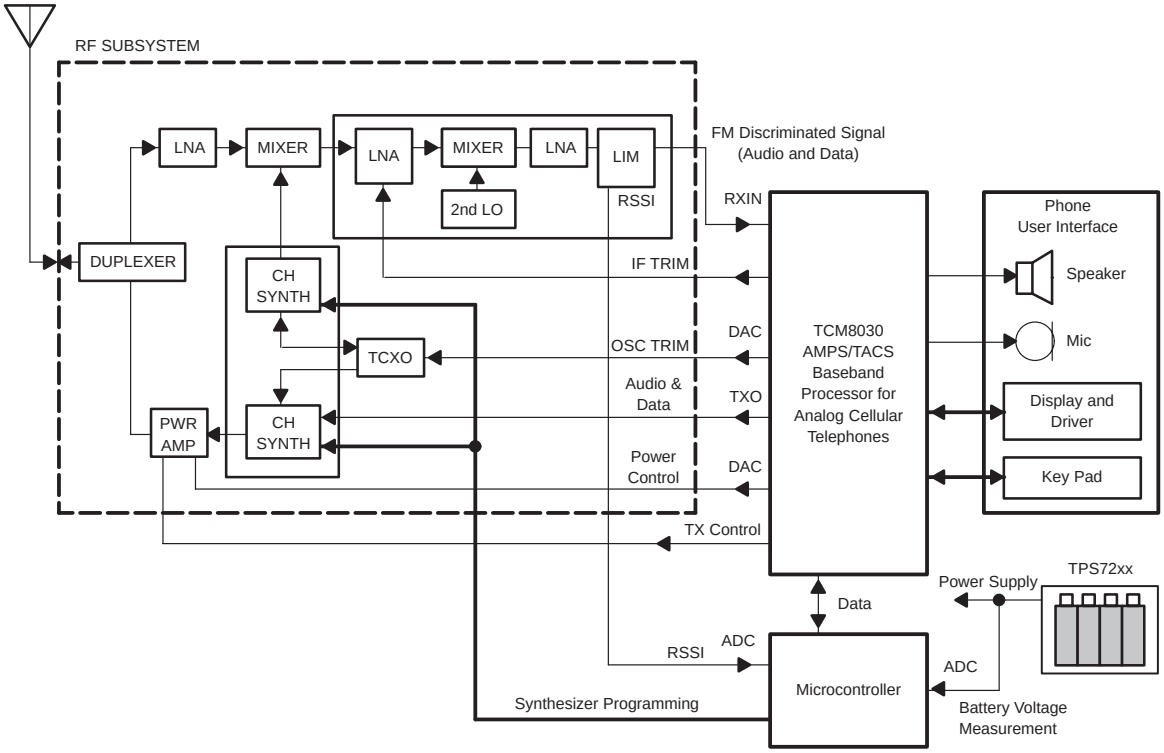
9.1 Typical Analog Cellular Telephone System Overview

The TCM8030 baseband processor provides a complete solution to cellular telephone audio and data filtering, decoding, and encoding requirements in AMPS, NAMPS, TACS, ETACS, NTACS, and JTACS systems.

The block diagram shown in Figure 9–1 illustrates typical analog cellular telephone system.

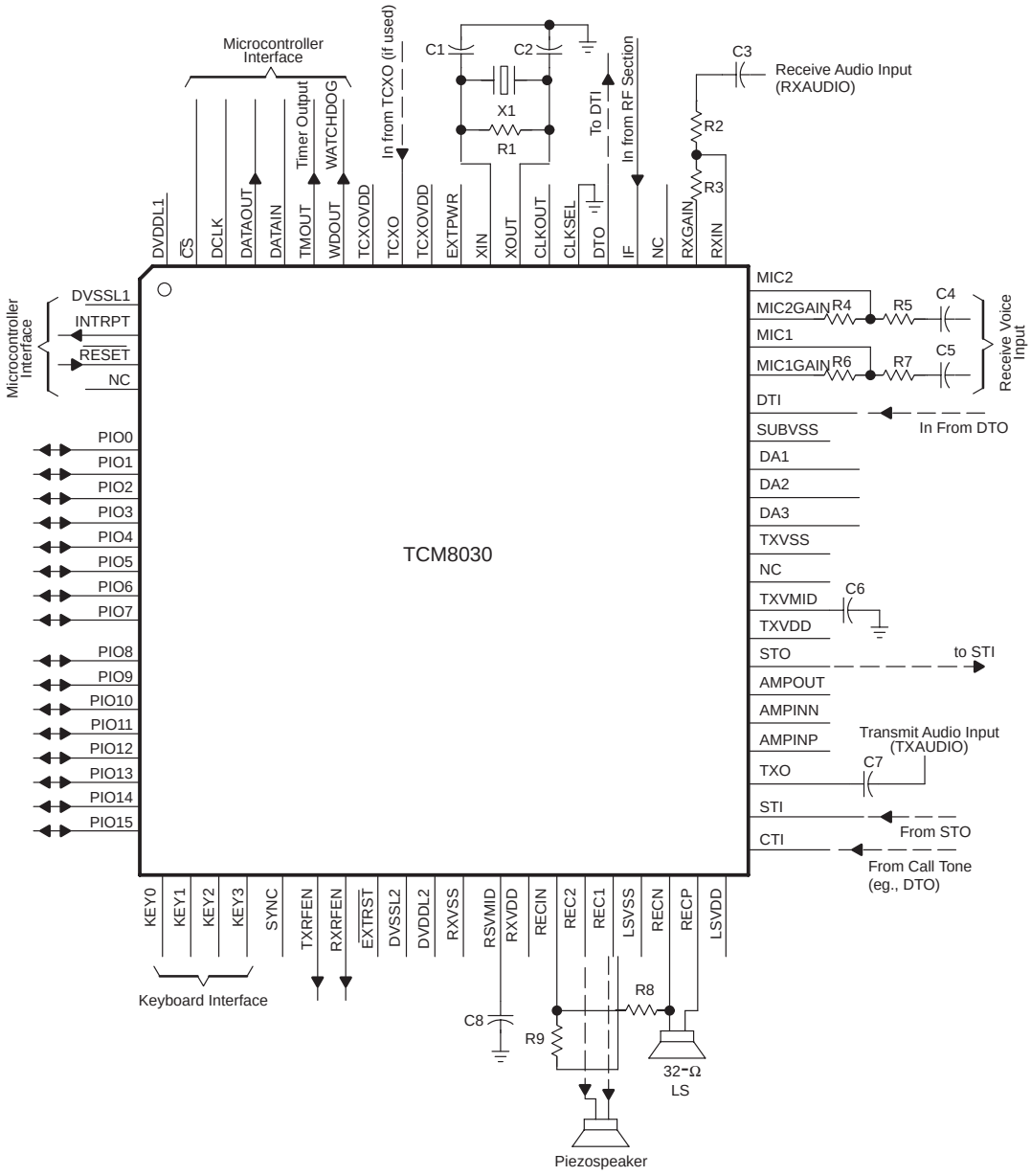
Figure 9–1. Typical Analog Cellular Telephone System



9.2 Circuit Description

Figure 9–2 illustrates the circuitry used in analog cellular telephone baseband processing. For additional information on the internal circuits of the TCM8030 see Chapter 2, *TCM8030 Principles of Operation*.

Figure 9–2. Analog Cellular Telephone Baseband Schematic



Note: For DTI, STI, and CTI, if necessary, apply external resistors to attenuate the incoming signal.

9.2.1 Parts List

The components used in analog cellular telephone baseband processing are listed in Table 9–1.

Table 9–1. Analog Cellular Telephone Components List

Component Designator	Typical Value	Function
R1	1 MΩ	Biasing resistor for crystal oscillator
R2	10 kΩ	Recommended minimum value. RXIN amplifier; gain = R3/R2.
R3	10 kΩ	Recommended minimum value
R4	10 kΩ	Recommended minimum value. Microphone amplifier number one; gain = R4/R5.
R5	10 kΩ	Recommended minimum value
R6	10 kΩ	Recommended minimum value. Microphone amplifier number two; gain = R6/R7.
R7	10 kΩ	Recommended minimum value
R8	10 kΩ	Recommended minimum value. REC amplifier; gain = R8/R9.
R9	50 kΩ	Recommended minimum value
C1	33 pF	Provides X1 with necessary capacitive loading for 180° phase inversion
C2	33 pF	Provides X1 with necessary capacitive loading for 180° phase inversion
C3	100 nF	AC couples the RXIN (audio and data input) from the FM discriminator/ demodulator.
C4	100 nF	AC couples the MIC2 amplifier input from the receive voice input.
C5	100 nF	AC couples the MIC1 amplifier input from the receive voice input.
C6	22 nF	Provides a low AC impedance reference for the transmit path
C7	100 nF	AC couples the output from the transmit voice, data, ST, and SAT signals to the FM modulator in the RF section.
C8	22 nF	Provides a low AC impedance for the receive path
X1	5.12 MHz	Fundamental crystal (or appropriate crystal as specified in the OSC and PROG DIV sections) (5.12 MHz is the default selection for the TCM8030 clocking scheme.)

9.2.2 Clock and Control

The TCM8030 communicates to the microcontroller through the microcontroller interface. You can program the TCM8030 to generate interrupt events. See the *TCM8030 Analog Baseband Processor Data Manual* for a listing of possible interrupt events that you can generate.

The microcontroller sends and receives all data communications using the microcontroller interface (MICRO CONTRL I/F). You program internal data, command, and interrupt registers using write operations, and you monitor internal data, status, and interrupt registers using read operations.

9.2.3 Transmit Path

The transmit voice inputs, MIC1 and MIC2, feed a pair of microphone amplifiers. Outputs from these amplifiers feed back into MICGAIN1 and MICGAIN2. An applied external resistor pair sets the gain for each amplifier.

The TCM8030 uses a single power supply. The reference voltage TXVMID biases the inputs of the microphone amplifiers, MIC1 and MIC2.

The voice, wideband or narrowband data, signaling tone (ST), and supervisory audio tone (SAT) signal levels are programmable throughout the transmit path, therefore eliminating the need for external adjustments.

The TCM8030 data encoder, TX ENCODER, performs all necessary control and voice channel signal formatting before it transmits the digital signal to the transmit output (TXO).

In wideband mode, the TCM8030 produces a digitally filtered signal, phase-locked to the received SAT signal. This received digital SAT signal is first separated from any signal noise and then measured and regenerated.

In narrowband mode, the received signal is continuously compared to the DSAT word. The DSAT word is regarded as correctly detected and determines when the receiver is locked onto the voice channel. The DSAT circuit in the TCM8030 generates the DSAT that corresponds to the DSAT color coding independent of the DSAT received from the base station.

For both SAT and DSAT, the TCM8030 conditions the digital signal and outputs the signal at TXO transmit output.

Along with the SAT, the TCM8030 also transmits a 10-kHz signaling tone (ST) on the voice channel to confirm channel orders and to request a flash-hook by the mobile, mobile-alert, or mobile-ending call. The TCM8030 outputs this signal at TXO transmit output. From TXO, the TCM8030 connects the audio signal to the RF modulator section.

9.2.4 Receive Path

The output from the FM demodulator/discriminator connects to the receive input (RXIN) of the TCM8030.

The TCM8030 audio outputs, REC1 and REC2, can be used as two separate outputs. For example, one can drive the phone earpiece, and the other can drive test equipment or accessories such as a hands-free unit. These two audio outputs can otherwise be configured to provide a differential output in order to increase the maximum level.

The TCM8030 filters and converts the received data to a digital signal. In wideband mode, after this data recovery, the data processor majority-votes and error-corrects the data. In narrowband mode, after this data recovery, the data processor error-corrects the data.

After data recovery, an interrupt signals the microcontroller that received data is available.

In addition to the data, the TCM8030 also recovers the SAT signal from the RX audio path through a filter and comparator. This signal feeds to the TCM8030 data processor where it is detected and regenerated.

9.2.5 Digital-to-Analog Converters

The TCM8030 contains three 8-bit DACs. The DAC outputs are at terminals DAC1, DAC2, and DAC3. These DACs are all 8-bit linear digital-to-analog converters. One provides power control of the RF transmit amplifier. The other two provide voltage adjustments to the RF stage for such purposes as calibrating the temperature-compensated crystal oscillator (TCXO) and trimming the first intermediate frequency (IF) stage.

9.2.6 Timers

The TCM8030 contains a watchdog timer and programmable timer. The watchdog timer resets the telephone's microcontroller if a time-out condition occurs. This is a requirement of AMPS and TACS systems. An uncommitted programmable 8-bit timer has an output, TMOUT, that pulses low when the counter reaches zero.

9.2.7 Keyboard Scan

The TCM8030 has a 4-bit port that accepts inputs from a keyboard and generates interrupts to the microcontroller. This port can also be configured as a general-purpose I/O port. One I/O terminal connected to the telephone ON/OFF key supplies a wake-up signal that terminates the total power-down mode.

9.2.8 I/O Expansion

The TCM8030 contains two 8-bit programmable expansion I/O ports. These are provided for communication with the telephone's microcontroller. Each bit is programmable as either an output or an input, with optional, current source pullup resistors.

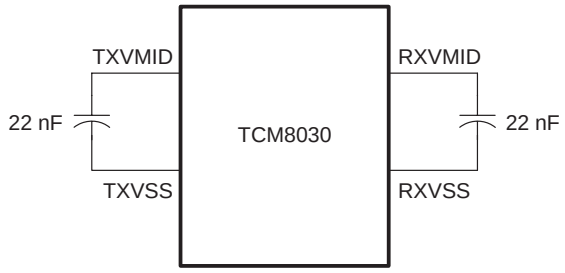
9.3 Decoupling on Supply Lines

The transmit supply (TXVDD and TXVSS), receive supply (RXVDD and RXVSS), digital 1 supply (DVDDL1 and DVSSL1), digital 2 supply (DVDDL2 and DVSSL2), and TCXO supply (TCXOVDD and TCXOVSS) require decoupling. You can achieve this by applying a 0.1-μF ceramic and a 1.0-μF tantalum capacitor in parallel, between the previous source's supply (VDD) and the ground (VSS). The values of these capacitors are minimum recommended values.

9.4 Decoupling TXVMID and RXVMID

TXVMID and RXVMID require separate decoupling from the supplies. You can achieve this by applying a 22-nF capacitor between RXVMID and RSVSS and also between TXVMID and TXVSS. The values of these capacitors are minimum recommended values. Figure 9–3 illustrates this decoupling.

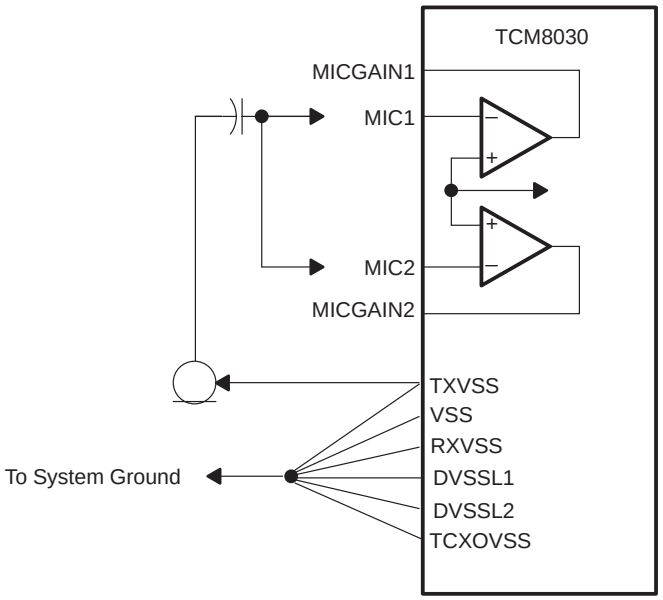
Figure 9–3. Decoupling TXVMID and RXVMID



9.5 Microphone Grounding

In order to reduce noise, observe the grounding scheme shown in Figure 9–4. Connect microphone VSS (ground) to TXVSS, and then use a star-connected circuit to connect to the system.

Figure 9–4. Microphone Grounding



9.6 Suggested Trim Adjustment Sequence

The TCM8030 is designed so that it requires no manual trims. All levels can be adjusted to meet system requirements and to compensate for production tolerances by writing to the microcontroller interface on the TCM8030. The microcontroller can then store the required data in a nonvolatile memory in the phone. When the phone is turned on, an initialization routine can write this calibrated data to the TCM8030.

The suggested sequence of adjustments is detailed below.

9.6.1 Transmit Adjustment Procedure

Voice Trim (VDTRIM) – Write Address 34H – [VD3 – VD0]

nominal setting [VD3 – VD0] = <1000>

1) Mute the signaling tone and SAT.
2) Apply an audio signal, at the desired level, into the amplifiers for MIC1 and MIC2.
3) Adjust VDTRIM register [VD3 – VD0] to set the frequency deviation. This also adjusts the TX DTMF level.

DTMF Trim

Set the DTMF level by using external resistors between the DTO output and the DTI input (TX path) and CTI input (RX path). There is not an independent DTMF trim register for the TCM8030.

Limiter Trim (LIMITER) – Write Address 35H – [LIM3 – LIM0]

nominal setting [LIM3 – LIM0] = <1010>

1) Increase the audio signal level by 20 dB.
2) Adjust [LIM3 – LIM0] to produce the required maximum deviation.

SAT Trim (SATTRIM) – Write Address 36H – [SAT3 – SAT0]

nominal setting [SAT3 – SAT0] = <1000>

1) Turn off the signaling tone and turn on the SAT path.
2) Make the TCM8030 generate its own 6000-Hz SAT tone.
3) Adjust [SAT3 – SAT0] to give the required frequency deviation.

TX-DAT Trim – (TX-DAT TRIM) – Write Address 37H – [DAT2 – DAT0]

(NAMPS or NTACS)

nominal setting [DAT2 – DAT0] = <100>

1) Set the TCM8030 to transmit the signaling tone.
2) Adjust [DAT2 – DAT0] for necessary narrowband data.

Transmit Trim (TXTRIM) – Write Address 38H – [TXT4 – TXT0]

nominal setting [TXT4 – TXT0] = <10000>

1) Set TX–DAT TRIM to nominal = 100.
2) Set the TCM8030 to transmit the signaling tone.
3) Adjust [TXT4 – TXT0] to set the frequency deviation to that required by the AMPS or TACS system.

9.6.2 Receive Adjustment Procedure

Receive Trim (RXTRIM) – Write Address 39H – [RXT3 – RXT0]

nominal setting [RXT3 – RXT0] = <1000>

1) Input a modulated signal to the telephone.
2) Adjust [RXT3 – RXT0] to produce the required level at REC1 and REC2.

9.6.3 Muting the Audio Path

Transmit Path –

Writing 00H to TXCFG (write address 33H) mutes the TX path. The path is actually muted at two positions: TXSW and TXSUM by connecting to TXVMID.

Receive Path –

Writing 00H to RXCFG (write address 32H) mutes the RX path. The path is actually muted at two positions: REC1SW and RECBUF by connecting to RXVMID.

9.6.4 RF Stage Adjustment Procedure

DACs to Trim RF Sections

Use the three 8-bit DACs to trim sections of the RF stage.

1) Write to address 40H – DAC range select (DACRANGE): Each DAC can independently set to full or half-range scale. For full range, the step size is TXVDD/256, and for half range, the step size is TXVDD/512.

2) Write to address 41H–43H: DAC data (DAC1DAT, DAC2DAT, DAC3DAT) can write to DAC1, DAC2, or DAC3, respectively.

The RF stage adjustment is typically used for RF transmit power control, TCXO trim, and first IF section trim. The TCM8030 is designed for AMPS, NAMPS, TACS, and NTACS standards, as detailed in Table 9–2, Table 9–3, Table 9–4, Table 9–5, Table 9–6, Table 9–7, Table 9–8, and Table 9–9. These tables suggest levels for transmitted and received audio, SAT, and data signals.

The numbers in Table 9–2 to Table 9–9 are from the AMPS standard and do not exactly reflect the device specification.

Table 9–2. Typical Tranmsit Signal Levels AMPS Mode (3-V Operation)

Signal	Peak Frequency Deviation (kHz)	Level At TXO	Unit
Design level	8	240	mVrms
Peak voice level	12	1018.234	mV peak-to-peak
SAT	2	60	mVrms
ST	8	60	mVrms
DATA	8	678.823	mV peak-to-peak
DTMF low tone, 697 Hz	3.1365	94.095	mVrms
DTMF high tone, 1477 Hz	6.6465	199.395	mVrms

Table 9–3. Typical Transmit Signal Levels NAMPS Mode (3-V Operation)

Signal	Peak Frequency Deviation (kHz)	Level At TXO	Unit
Design level	3	90	mVrms
Peak voice level	5	424.264	mV peak-to-peak
DSAT	0.7	20.893	mVrms
DST	0.7	20.893	mVrms
DATA	0.7	54.094	mV peak-to-peak
DTMF low tone, 697 Hz	1.30751	39.225	mVrms
DTMF high tone, 1477 Hz	2.77072	83.122	mVrms

Table 9–4. Typical Transmit Signal Levels TACS Mode (3-V Operation)

Signal	Peak Frequency Deviation (kHz)	Level At TXO	Unit
Design level	5.7	216	mVrms
Peak voice level	9.5	1018.234	mV peak-to-peak
SAT	1.7	59.979	mVrms
ST	6.4	242.526	mVrms
DATA	6.4	685.968	mV peak-to-peak
DTMF low tone, 697 Hz	1.2 max	45.432	mVrms
DTMF high tone, 1477 Hz	3.19 max	120.896	mVrms

Table 9–5. Typical Transmit Signal Levels NTACS Mode (3-V Operation)

Signal	Peak Frequency Deviation (kHz)	Level At TXO	Unit
Design level	3	113,684	mVrms
Peak voice level	5	535.913	mV peak-to-peak
DSAT	0.7	26.363	mVrms
DST	0.7	26.363	mVrms
DATA	0.7	74.567	mV peak-to-peak
DTMF low tone, 697 Hz	1.4288	54.144	mVrms
DTMF high tone, 1477 Hz	3.0278	114.738	mVrms

Table 9–6. Typical Receive Signal Levels AMPS Mode (3-V Operation)

Signal	Peak Frequency Deviation (kHz)	Level At REC1 & REC2	Unit
Design level	8	471.964	mVrms
Peak voice level	12	2002.373	mV peak-to-peak
SAT	2	117.991	mVrms
ST	8	471.964	mVrms
DATA	8	1334.915	mV peak-to-peak

Table 9–7. Typical Receive Signal Levels NAMPS Mode (3-V Operation)

Signal	Peak Frequency Deviation (kHz)	Level At REC1 & REC2	Unit
Design level	3	176.986	mVrms
Peak voice level	5	834.322	mV peak-to-peak
DSAT	0.7	41.297	mVrms
DST	0.7	41.297	mVrms
DATA	0.7	116.805	mV peak-to-peak

Table 9–8. Typical Receive Signal Levels TACS Mode (3-V Operation)

Signal	Peak Frequency Deviation (kHz)	Level At REC1 & REC2	Unit
Design level	5.7	424.768	mVrms
Peak voice level	9.5	2002.373	mV peak-to-peak
SAT	1.7	126.685	mVrms
ST	6.4	476.932	mVrms
DATA	6.4	1348.967	mV peak-to-peak

Table 9–9. Typical Receive Signal Levels NTACS Mode (3-V Operation)

Signal	Peak Frequency Deviation (kHz)	Level At REC1 & REC2	Unit
Design level	3	223.562	mVrms
Peak voice level	5	1053.881	mV peak-to-peak
DSAT	0.7	52.164	mVrms
DST	0.7	52.164	mVrms
DATA	0.7	147.543	mV peak-to-peak

Appendix A

Glossary

A

AFC: *Automatic Frequency Control.* The closed loop process that calibrates a TCXO frequency by using a more stable IF frequency as a reference.

AMPS: *Advanced Mobile Phone Services*

arbitration logic: A stage in the data processor that monitors the FOCC for an idle-to-busy transition to correlate messages sent on the corresponding RECC.

B

BCH code: Bose-Chaudhuri-Hocquenghem Code.

BPF: *Band-Pass Filter*

busy-idle bits: The portion of the data stream transmitted by a land station on a forward control channel that is used to indicate the current busy-idle status of the corresponding reverse control channel.

C

CBSW: *Compressor Bypass Switch*

compandor: A combination of a compressor at the transmitter to reduce the dynamic range of the transmitted signal and an expandor at the receiver to recover this signal to the original dynamic range. Used in communications systems to improve signal-to-noise as a result of reduced transmitted dynamic range. In analog cellular, 2:1 syllabic compression is used to limit the maximum peak voice deviation to ±2.9 kHz.

control channel: A channel used for the transmission of digital control information from a land station to a mobile station or from a mobile station to a land station.

CTI: *Call Tone Input*

D

DAC: *Digital-to-Analog Converter*

DCC: *Digital Color Code.* A digital signal transmitted by a land station on a forward control channel that is used to detect capture of a land station by an interfering mobile station.

de-emphasis: A stage in the receiver path that restores frequency components to their original level.

dotting: A fixed frequency tone that corresponds the phase of the receiver clock to the rate of the incoming data.

DSAT: *Digital Supervisory Audio Tone*

DST: *Digital Signaling Tone*

DTI: *DTMF Signaling Input*

DTMF: *Dual-Tone Multifrequency Generator*

DTO: *Dual-Tone Multifrequency Generator Output*

E

EBSW: *Expandor Bypass Switch*

ETACS: *Extended Total Access Communication Systems*

extended protocol: An optional expansion of the signaling messages between the land station and mobile station to allow for the addition of new system features and operational capabilities.

F

FOCC: *Forward Control Channel.* A control channel used from a land station to a mobile station.

full operation mode: TCM8030 power mode where power is applied to the device, and the phone is in conversation mode. The DTMF generator can be separately enabled along with several auxiliary functional blocks.

FVC: *Forward Voice Channel.* A voice channel used from a land station to a mobile station.

I

idle mode: TCM8030 power mode where power is applied to the device and the device is monitoring the FOCC from the base station.

IF: *Intermediate Frequency*

J

JTACS: *Japanese Total Access Communication Systems*

L

land station: A station in the Domestic Public Cellular Radio Telecommunications Service, other than a mobile station, used for radio communications with mobile stations.

limiter: A stage in the receiver path that reduces amplitude variations in the incoming signal from the FM demodulator/discriminator.

LS DRIVER: *Loudspeaker Driver*

M

majority voting: A vote of three out of five words to determine whether to eliminate the recognition of corrupted data.

MCU: *Microcontroller Unit*

mobile station: A station in the Domestic Public Cellular Radio Telecommunications Service used while in motion or during halts at unspecified points. It is assumed that mobile stations include portable units (e.g., hand-held “personal” units) as well as units installed in vehicles.

N

NAMPS: *Narrowband Advanced Mobile Phone Services*

NTACS: *Narrowband Total Access Communication Services*

P

PLL: *Phase-Locked Loop*

pre-emphasis: A stage in the transmitter path that optimizes the frequency components of the audio signals for FM transmission.

R

RECC: *Reverse Control Channel.* The control channel used from a mobile station to a land station.

RECC multiple-word transmission: Message format that continues the second word (240 bits) immediately following the completion of the first word (240 bits) in a single, continuous RECC message stream. This can consist of one to five words.

RFI: *Radio Frequency Interference*

RVC: *Reverse Voice Channel.* The voice channel used from a mobile station to a land station.

RVC multiple-word transmission: Message format that continues the second word sequence immediately following the completion of the first word sequence in a single, continuous RVC message stream. This can consist of one or two words.

S

SAT: *Supervisory Audio Tone.* One of three tones in the 6-kilohertz region that are transmitted by a land station and transponded by a mobile station.

seizure precursor: The initial digital sequence transmitted by a mobile station to a land station on a reverse control channel.

shutdown mode: TCM8030 power savings mode where power is applied to the device, but the phone is unable to answer calls.

signaling tone: A 10-kHz tone transmitted by a mobile station on a voice channel to: (1) confirm orders, (2) signal flash requests, and (3) signal release requests.

SPI: *Serial Peripheral Interface*

ST: *Signaling Tone*

STI: *Sidetone Input*

synchronization: The process by which the data processor attempts to correlate its clock phase with the incoming received data stream.

T

TACS: *Total Access Communication Systems*

TCXO: *Temperature-Compensated Crystal Oscillator*

tone mode: TCM8030 power mode where power is applied to the device, the phone is not in communication with the base station, and the user interface is enabled.

total power-down mode: TCM8030 power savings mode where all circuits in the device are powered down except a static power-up.

TXBPF: *Transmit Band-Pass Filter*

TXLPF: *Transmit Low-Pass Filter*

TXO: *Transmit Output*

TXSW: *Transmit Switch*

TXVMID: *Transmit Voltage Mid-rail Reference*

V

voice channel: A channel on which a voice conversation occurs and on which brief digital messages may be sent from a land station to a mobile station or from a mobile station to a land station.

W

word sync: An 11-bit Barker code (11100010010) that is used as part of the FOCC, RECC, FVC, and RVC preamble formats.

X

XTALOSC: *Crystal Oscillator*

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