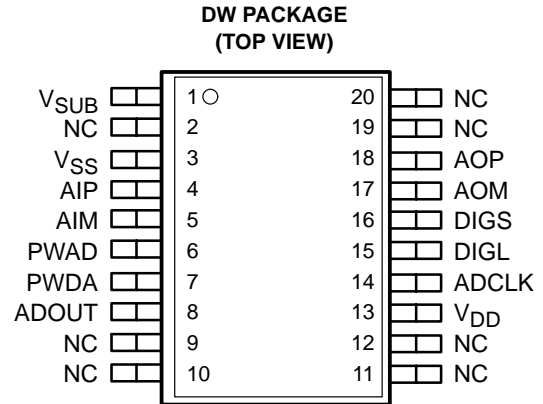


MSP58C20 AUDIO-BAND CONVERTER

SPSS015B – DECEMBER 1993 – REVISED JULY 1996

- Analog Portion of ADC and DAC for Audio-Band Signal-Processing Applications
- 5-V Supply Voltage
- Oversampling Second-Order Sigma-Delta Modulator
- 1.024-MHz Master Clock Frequency
- On-Chip Continuous-Time Antialiasing and Smoothing Filters
- High-Performance Fully Differential and Symmetrical Analog Data Paths
- Internal Reference Voltage and Common-Mode Bias Voltage Generation
- Very Low Power Consumption Mode



NC – No internal connection

description

The MSP58C20 is the analog portion of an audio-band sigma-delta analog-to-digital and digital-to-analog converter and is a companion part to the MSP58C80. The MSP58C20 is designed to operate only with the MSP58C80, which contains the digital portion of the audio-band converter. The circuit consists of three main blocks: the analog-to-digital converter (ADC), the digital-to-analog converter (DAC), and internal reference and bias voltages.

The analog-to-digital conversion chain consists of a continuous-time antialiasing stage, an analog oversampled modulator, and the modulator bias voltage. The antialiasing stage is a second-order low-pass filter with a cutoff frequency of typically 190 kHz. The modulator is a sigma-delta feedback loop, which oversamples the signal at 1.024 MHz and provides second-order noise shaping. It performs the conversion of the differential analog input signal to a pulse-density-modulated single-bit digital output (ADOUT). When a maximum positive differential input voltage (i.e., a maximum positive voltage difference of AIP – AIM) is applied at the AIP and AIM inputs, the resulting code at the ADOUT output is all ones.

The digital-to-analog conversion chain consists of a fast DAC, an analog low-pass filter, and the filter's bias voltage. The two input bits (DIGS and DIGL), sampled at 0.512 MHz from a digital modulator on the MSP58C80, are the inputs of the DAC conversion chain. Based on the values for DIGS (the sign bit) and DIGL (the level bit), the following table shows the DAC voltage steps that are produced.

DIGS	DIGL	DAC VOLTAGE STEPS
L	L	$-1 \times V_{ref}$
L	H	$-2 \times V_{ref}$
H	L	$+1 \times V_{ref}$
H	H	$+2 \times V_{ref}$

When DIGS = L, the AOM analog output has a more positive voltage than AOP. When DIGL = H, the absolute value of the voltage difference between AOP and AOM is greater than when DIGL = L. A band-gap voltage source is used to produce the DAC and ADC reference voltages. These two references are different to avoid crosstalk between the two converters.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

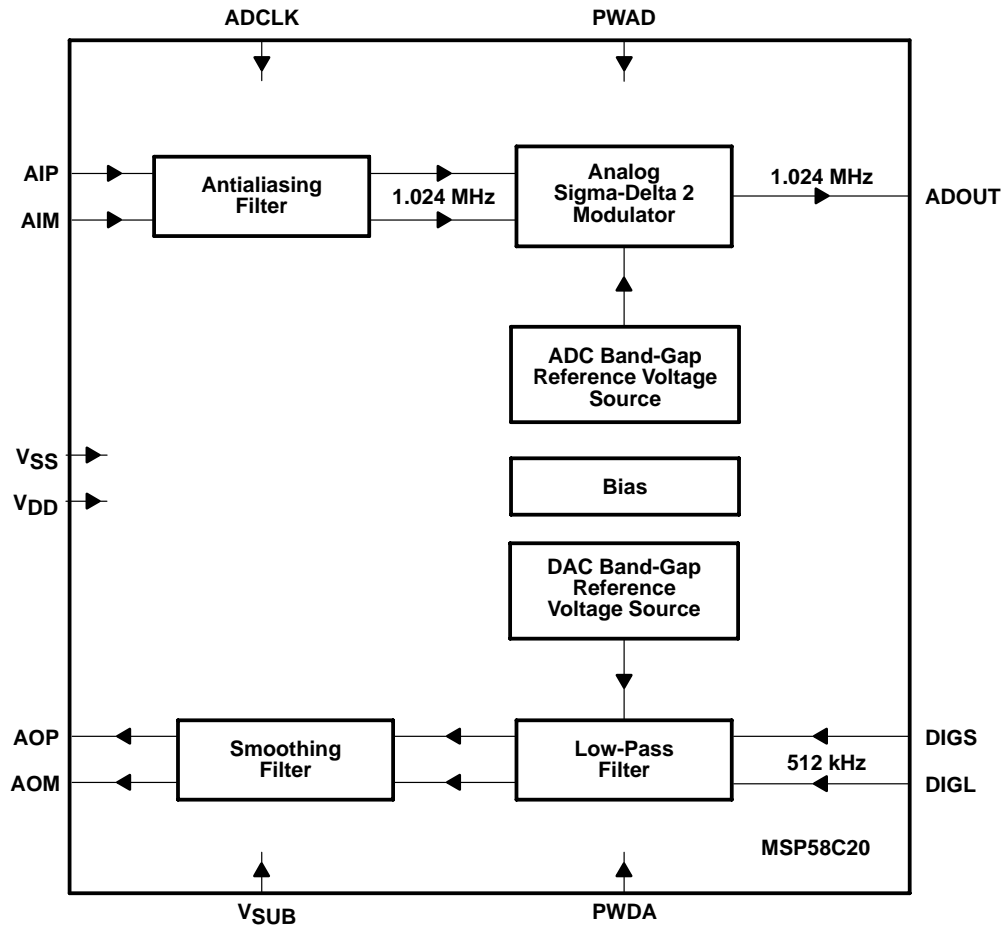
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functional block diagram



Terminal Functions

TERMINAL NAME	NO.	A/D	I/O	DESCRIPTION
ADCLK	14	D	I	ADCLK is a 1.024-MHz clock input.
ADOUT	8	D	O	ADOUT is the 1-bit output of the ADC modulator and is sampled at 1.024 MHz.
AIM	5	A	I	AIM is a negative differential input for the ADC. AIP and AIM together form a balanced differential input. The biasing of this terminal is fixed through resistors by the internal common-mode voltage source. This terminal can be ac coupled or dc coupled. If the terminal is dc coupled, external common-mode bias should satisfy recommended operating conditions.
AIP	4	A	I	AIP is a positive differential input for the ADC. AIP and AIM together form a balanced differential input. The biasing of this terminal is fixed through resistors by the internal common-mode voltage source. This terminal can be ac coupled or dc coupled. If the terminal is dc coupled, external common-mode bias should satisfy recommended operating conditions.
AOM	17	A	O	AOM is a negative differential DAC output. AOP and AOM together form a balanced differential output. The common-mode voltage at this terminal is fixed by the internal common-mode circuitry.
AOP	18	A	O	AOP is a positive differential DAC output. AOP and AOM together form a balanced differential output. The common-mode voltage at this terminal is fixed by the internal common-mode circuitry.
DIGL	15	D	I	DIGL is the input level bit of the DAC and is sampled at 0.512 MHz.
DIGS	16	D	I	DIGS is the input sign bit of the DAC and is sampled at 0.512 MHz.
PWAD	6	D	I	When PWAD is high, it puts the ADC part of the circuit into a power-down mode. When both PWAD and PWDA are high, the MSP58C20 is in a stable low-power-consumption state.
PWDA	7	D	I	When PWDA is high, it puts the DAC part of the circuit in a power-down mode. When both PWAD and PWDA are high, the MSP58C20 is in a stable low-power-consumption state.
V _{SUB}	1	n/a	n/a	V _{SUB} and V _{SS} must be connected together to minimize substrate currents during power up, power down, and normal operation.
V _{DD}	13	n/a	n/a	V _{DD} is the 5-V power supply.
V _{SS}	3	n/a	n/a	V _{SS} is ground. The internal band-gap voltage and the common-mode bias voltages are referenced to V _{SS} .

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{DD} (see Note 1)	–0.3 V to 6 V
Input voltage range, V _I (any digital or analog input, see Note 1)	–0.3 V to V _{DD} + 0.3 V
V _{SUB} , V _{SS} voltage range, relative to each other	–30 mV to 30 mV
Operating free-air temperature range, T _A	0°C to 70°C
Storage temperature range, T _{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} unless otherwise noted.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 1)	4.75	5	5.25	V
High-level input voltage, digital inputs, V_{IH} (see Note 1)	2			V
Low-level input voltage, digital inputs, V_{IL} (see Note 1)			0.8	V
Maximum differential input voltage between AIP and AIM (ac or dc peak-to-peak voltage), V_{ID}	-3		3	V
Common-mode input voltage at AIP and AIM, V_{IC} (see Note 1)	$0.45 \times V_{DD}$	$0.5 \times V_{DD}$	$0.55 \times V_{DD}$	V
Input clock frequency, ADCLK		1.024		MHz
Resistive load between AOP and AOM	15			k Ω
Capacitive load at AOP and AOM (at each output versus V_{SS})			50	pF
Operating free-air temperature, T_A	0		70	$^{\circ}$ C

NOTE 1: All voltage values are with respect to V_{SS} unless otherwise noted.



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, ADCLK input frequency = 1.024 MHz, PWDA = L and PWAD = L (power-up mode) (unless otherwise noted)

supply current characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DD}	Supply current	PWAD = H, PWDA = H, Digital inputs = V _{DD} or V _{SS} , Digital output = no load			50	μA
		PWAD = L, PWDA = L	6.5	9	16	mA

analog input characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmit dynamic range, maximum differential input voltage (between AIP and AIM)		dc or ac voltage	±2.22	±2.36	±2.5	V
V _{IO}	Transmit differential input offset voltage	See Note 2	-150		150	mV
V _{IC}	Internal common-mode voltage at AIP and AIM		0.4 × V _{DD}	0.5 × V _{DD}	0.6 × V _{DD}	V
z _i	Input impedance	AIP Between AIP and internal common-mode voltage source (AIM = V _{DD} /2)	15	25	35	kΩ
		AIM Between AIM and internal common-mode voltage source (AIP = V _{DD} /2)	15	25	35	
	Input capacitance	AIP Measured at 5 MHz between AIP and V _{SS} (AIM = V _{DD} /2)			50	pF
		AIM Measured at 5 MHz between AIM and V _{SS} (AIP = V _{DD} /2)			50	

NOTE 2: Calculated by linear regression based on five dc measurements between -1 V and 1 V

digital output characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	Digital high-level output voltage versus V _{SS}	I _{OH} = 300 μA	2.4			V
V _{OL}	Digital low-level output voltage versus V _{SS}	I _{OL} = 1 mA			0.4	V

analog output characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OD}	Differential output voltage, dynamic range, AOP to AOM	Balanced loads, dc measurement	±2.82	±3	±3.18	V
V _{OO}	Differential output offset voltage	dc measurement	-150		150	mV
V _{OC}	Common-mode output voltage at AOP and AOM		0.4 × V _{DD}	0.5 × V _{DD}	0.6 × V _{DD}	V

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, ADCLK input frequency = 1.024 MHz, PWDA = L and PWAD = L (power-up mode) (unless otherwise noted) (continued)

ADC transmit characteristics†

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Transmit absolute gain tolerance	$V_{DD} = 5\text{ V}$, Input = 1-kHz sine wave at -13 dBrl				± 0.5	dB
Transmit gain versus input level	Input = 1-kHz sine wave, Gain reference level = gain measured at input level of -13 dBrl , See Note 3	Input level = -1 dBrl to -43 dBrl			± 0.25	dB
		Input level = -43 dBrl to -53 dBrl			± 0.5	
		Input level = -53 dBrl to -58 dBrl			± 1	
Transmit gain versus supply voltage	$V_{DD} = 4.75\text{ V}$ to 5.25 V , Input = 1 kHz at -13 dBrl				± 0.15	dB
Transmit idle channel in-band noise	Psophometrically-weighted output noise, Transmit channel idle				-76	dBrlp
Transmit idle channel single-frequency noise spectrum (see Note 4)	$T_A = 25^\circ\text{C}$, FFT rectangular window bandwidth = 125 Hz, Transmit channel idle, See Figure 5	$f = 50\text{ Hz}$			-80	dBrl
		$f = 300\text{ Hz}$			-82	
		$f = 3.4\text{ kHz}$			-82	
		$f = 4\text{ kHz}$			-80	
		$f = 7\text{ kHz}$			-72	
		$f = 20\text{ kHz}$			-64	
Transmit single-frequency distortion	Input = one frequency in 0.7-kHz to 1.1-kHz band at -4 dBrl , Measured first two harmonics				-50	dB
Transmit intermodulation distortion (see Note 4)	Input = two frequencies in 0.3-kHz to 3.4-kHz band, Input levels = -7 dBrl and -24 dBrl , Measured second and third intermodulation products				-40	dBrl
Transmit-signal-to-total-noise-plus-distortion ratio (see Note 5)	$V_{DD} = 5.25\text{ V}$, $T_A = 25^\circ\text{C}$, Input = 1-kHz sine wave, Measured psophometrically-weighted total noise plus distortion, See Figure 6	Input level = -70 dBrl	-13			dB
		Input level = -20 dBrl	50			
		Input level = -1 dBrl	50			
Transmit gain variations versus input frequency (see Notes 4 and 6)	$f = 0.1\text{ kHz}$ to 4 kHz , Input level = -13 dBrl				± 0.6	dB
Transmit power supply rejection	See Note 7				30	dB
I_{lkg} Leakage current	Voltage applied to terminal is between V_{SS} and V_{DD} , PWDA = H (power-down mode)	AIP	-10		10	μA
		AIM	-10		10	
Receive-to-transmit crosstalk	Receive input = one frequency in 0.3-kHz to 3.4-kHz band at -3 dBrl , Crosstalk measured at transmit digital output, Transmit channel idle				-70	dB

† This table contains specifications in which the power levels are expressed in dBrl; dBrl stands for dB above reference level. 0 dBrl is the ADC theoretical overload point. This overload point corresponds to a sine wave at the input of the modulator with peak amplitude equal to 2.25 V dBrlp is a psophometrically-weighted value being compared against a psophometrically-weighted reference.

NOTES: 3. Input satisfies CCITT G.714 15.3, Method 2.

4. This parameter is characterized but not tested.

5. Input satisfies CCITT G.714 14.3, Method 2.

6. Gain is relative to gain at 1 kHz.

7. The power-supply rejection measurement is made with a 50-mVrms, 0- to 20-kHz signal applied to V_{DD} and with the transmit channel idle.



electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, ADCLK input frequency = 1.024 MHz, PWDA = L and PWAD = L (power-up mode) (unless otherwise noted) (continued)

DAC receive characteristics†

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
Receive gain tolerance	$V_{DD} = 5\text{ V}$, Input = 1-kHz sine wave at -28 dBrl				± 0.5	dB	
Receive gain versus input level	Input = 1-kHz sine wave, Gain reference level = gain measured at input level of -28 dBrl , See Note 8	Input level = -1 dBrl to -43 dBrl			± 0.25	dB	
		Input level = -43 dBrl to -53 dBrl			± 0.5		
		Input level = -53 dBrl to -58 dBrl			± 1		
Receive gain versus supply voltage	$V_{DD} = 4.75\text{ V}$ to 5.25 V , Digital input = 1-kHz sine wave at -28 dBrl				± 0.15	dB	
Receive idle channel in-band noise	Receive channel idle, Psophometrically-weighted output noise				-75	dBrlp	
Receive idle channel single-frequency noise spectrum (see Note 4)	$T_A = 25^\circ\text{C}$, Receive channel idle, Measurement bandwidth = 125 Hz , See Figure 6	$f = 100\text{ Hz}$			-82	dBrl	
		$f = 3\text{ kHz}$			-82		
		$f = 10\text{ kHz}$			-64		
		$f = 100\text{ kHz}$			-64		
Receive single-frequency distortion	Input = one frequency in 0.7-kHz to 1.1-kHz band at -6 dBrl , Measured first two harmonics				-50	dB	
Receive intermodulation distortion (see Note 4)	Input = two frequencies in 0.3-kHz to 3.4-kHz band, Input levels = -7 dBrl and -24 dBrl , Measured second and third intermodulation products				-40	dBrl	
Receive signal-to-total-noise-plus-distortion ratio (see Note 9)	$V_{DD} = 5.25\text{ V}$, $T_A = 25^\circ\text{C}$, Input = 1-kHz sine wave, Measured psophometrically-weighted total noise plus distortion, See Figure 7	Input level = -70 dBrl			0	dB	
		Input level = -20 dBrl			50		
		Input level = -1 dBrl			50		
Receive gain variations versus input sine wave frequency (see Note 6)	$V_{DD} = 4.75\text{ V}$, $T_A = 25^\circ\text{C}$, Input level = -13 dBrl , See Figure 9	$f = 156\text{ Hz}$ to 4 kHz			-0.6^\ddagger	0.6	dB
		$f = 4.6875\text{ kHz}$			-0.7	-0.4	
		$f = 6.25\text{ kHz}$			-1.75	-1.4	
		$f = 7.8125\text{ kHz}$			-3.35	-2.9	
		$f = 9.375\text{ kHz}$			-5.25	-4.8	
		$f = 10.9375\text{ kHz}$			-7.25	-6.8	
		$f = 12.5\text{ kHz}$			-9.2	-8.7	
$f = 15.625\text{ kHz}$			-12.8	-12.2			
Receive power supply rejection	See Note 10				30	dB	

† This table contains specifications in which the power levels are expressed in dBrl; dBrl stands for dB above reference level. 0 dBrl is the DAC overload point. Overload levels of the digital modulator (see parameter measurement information) are 32767 and -32767 peak values. The 0-dBrl level is related to maximum differential output voltage, which is typically 2.25 V.

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for receive gain variations versus input sine-wave frequency.

NOTES: 4. This parameter is characterized but not tested.

6. Gain is relative to gain at 1 kHz.

8. Input satisfies CCITT G.714 15.4 Method 2.

9. Input satisfies CCITT G.714 14.4 Method 2.

10. The power supply rejection measurement is made with a 50-mVrms, 0-kHz to 20-kHz signal applied to V_{DD} and with the receive channel idle.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, ADCLK input frequency = 1.024 MHz, PWDA = L and PWAD = L (power-up mode) (unless otherwise noted) (continued)

DAC receive characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{lkg}	Leakage current	AOP	-10		10	μA
		AOM	-10		10	
Output impedance, differential, between AOP and AOM (see Note 4)			30			kΩ
Transmit-to-receive crosstalk		Transmit input = one frequency in 0.3-kHz to 3.4-kHz band at -3 dB _r , Receive channel idle, Crosstalk measured at receive analog output			-70	dB

NOTE 4. This parameter is characterized but not tested.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{su1}	Transmit setup time at power up (PWAD transition from H to L)	ADCLK input frequency = 1.024 MHz, See Note 11		20		μs
t _{su2}	Receive setup time at power up (PWDA transition from H to L)	ADCLK input frequency = 1.024 MHz, See Note 12		20		μs
t _{su3}	Receive setup time, DIGS or DIGL setup before ADCLK↑	See Figure 4	50			ns
t _h	Receive hold time, DIGS or DIGL hold after ADCLK↑	See Figure 4	50			ns
t _c	Cycle time, ADCLK			1		μs
t _{w1}	Pulse duration, ADCLK high		470			ns
t _{w2}	Pulse duration, ADCLK low		470			ns
t _f	Fall time, ADCLK				20	ns
t _r	Rise time, ADCLK				20	ns

NOTES: 11. After the setup time, the transmit channel displays normal operating characteristics.

12. After the setup time, the receive channel displays normal operating characteristics.

switching characteristic over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t _a	Transmit access time, ADO _{UT} after ADCLK↑ (see Note 4)	See Figure 3			100	ns

NOTE 4. This parameter is characterized but not tested.



PARAMETER MEASUREMENT INFORMATION

The receive characteristics in the electrical characteristics table are measured by activating the MSP58C20 receive path through a digital modulator. This modulator consists of two functional blocks (see Figure 1 and Figure 2) connected in series. The output of the decoder (see Figure 2) is shown in Table 1.

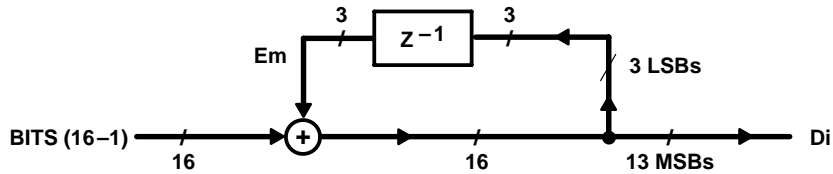


Figure 1. 16- to 13-Bit Modulator at 512-kHz Sampling Rate

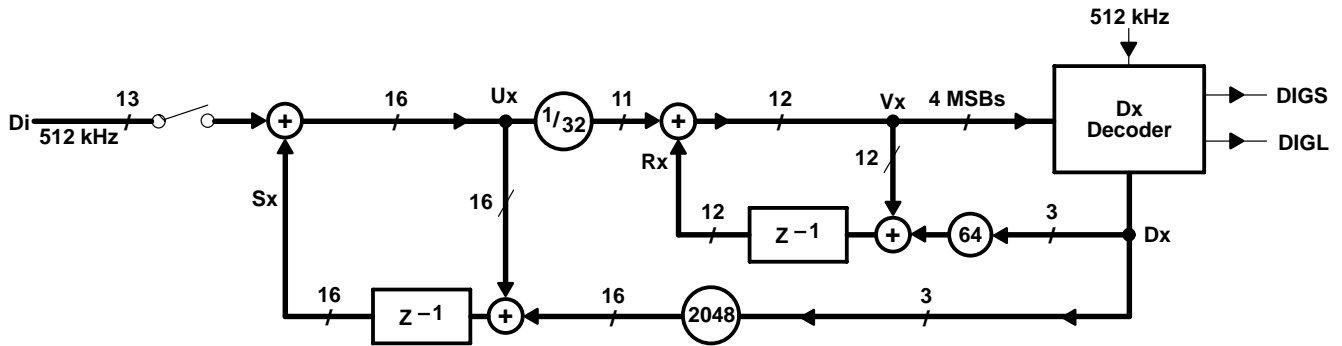


Figure 2. Sigma-Delta-2 Modulator at 512-kHz Sampling Rate

Table 1. Dx Decoder

DECODER INPUT				DECODER OUTPUT				
Vx (11)	Vx (10)	Vx (9)	Vx (8)	Dx (2)	Dx (1)	Dx (0)	DIGS	DIGL
0	1	X	X	H	H	L	L	H
0	0	1	X	H	H	L	L	H
0	0	0	1	H	H	L	L	H
0	0	0	0	H	H	H	L	L
1	1	1	1	L	L	H	H	L
1	1	1	0	L	H	L	H	H
1	1	0	X	L	H	L	H	H
1	0	X	X	L	H	L	H	H

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PARAMETER MEASUREMENT INFORMATION

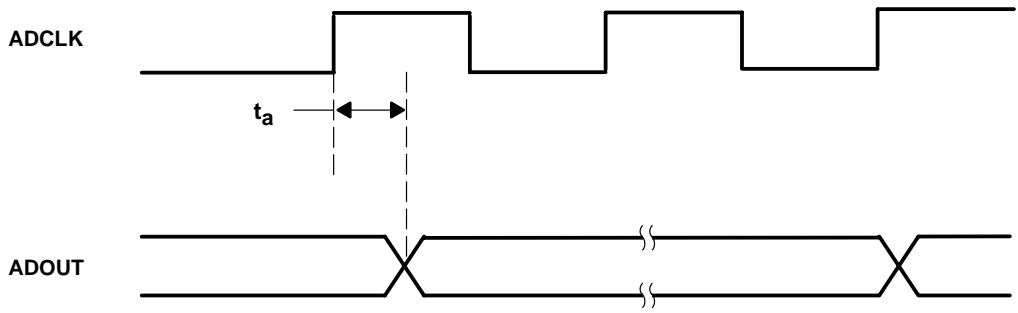


Figure 3. Transmit Access Timing Waveforms

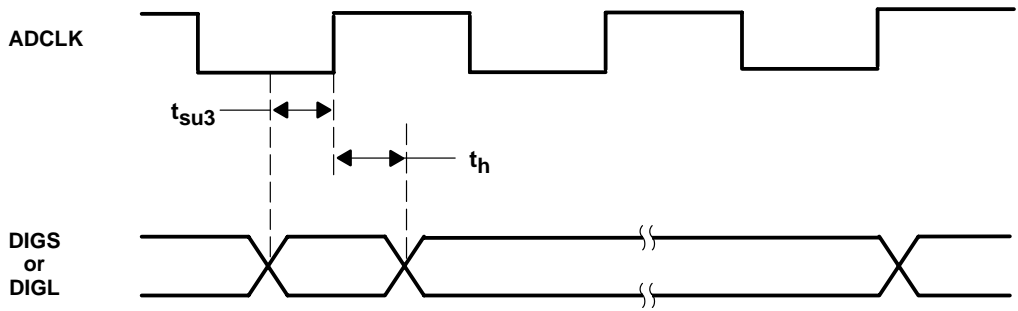


Figure 4. Receive Setup and Hold Time Waveforms



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TYPICAL CHARACTERISTICS

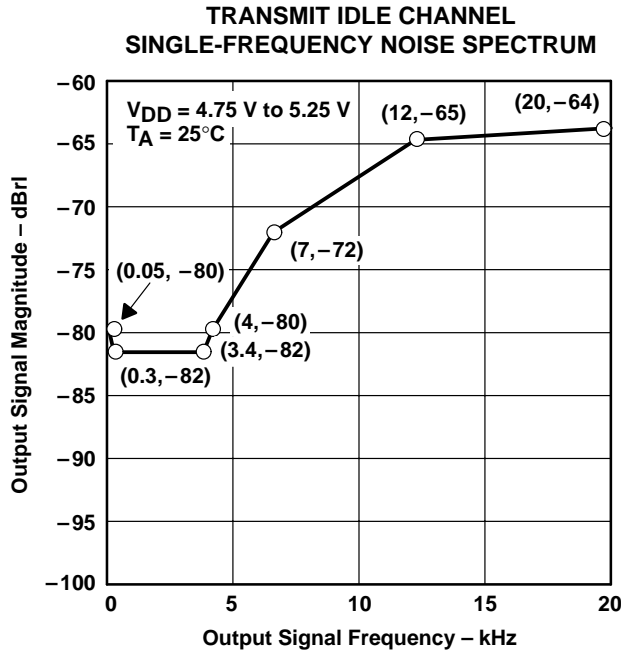
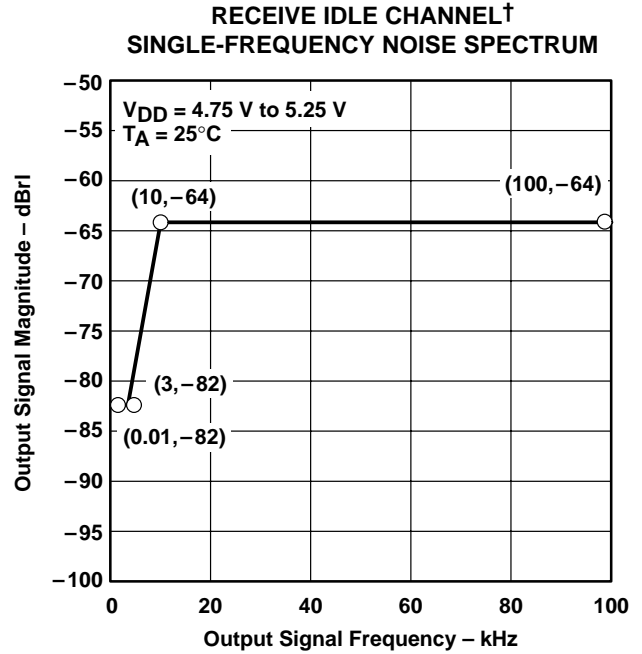
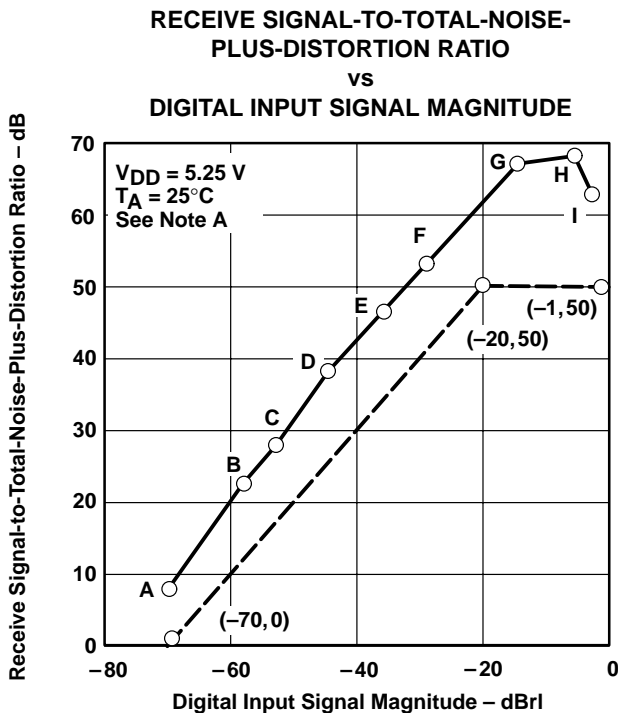


Figure 5



† This parameter is characterized but not tested.

Figure 6



SET OF POINTS	LOCATION
A	(-70, 9)
B	(-58, 23)
C	(-53, 28)
D	(-43, 38)
E	(-35, 46)
F	(-28, 53)
G	(-13, 67)
H	(-5, 69)
I	(-1, 64)

NOTE A: The three points on the dashed line are minimum qualification standards, which every MSP58C20 must pass. The curve shows empirical data from a representative lot.

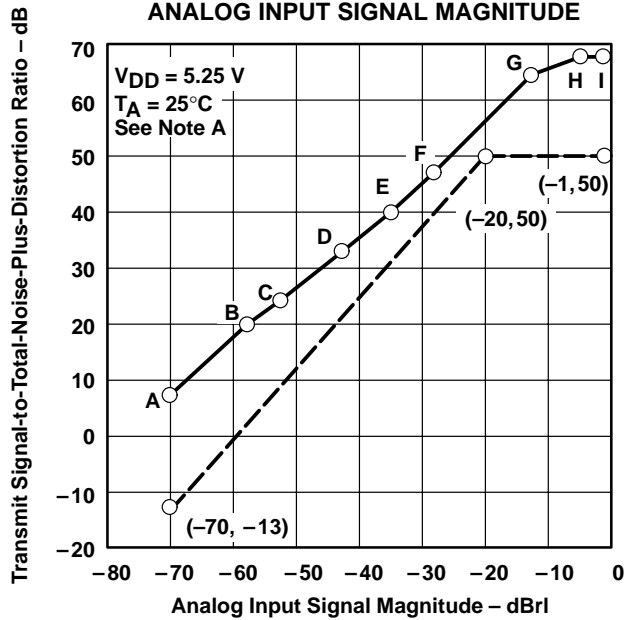
Figure 7

MSP58C20 AUDIO-BAND CONVERTER

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TYPICAL CHARACTERISTICS

TRANSMIT SIGNAL-TO-TOTAL-NOISE-
PLUS-DISTORTION RATIO
vs
ANALOG INPUT SIGNAL MAGNITUDE



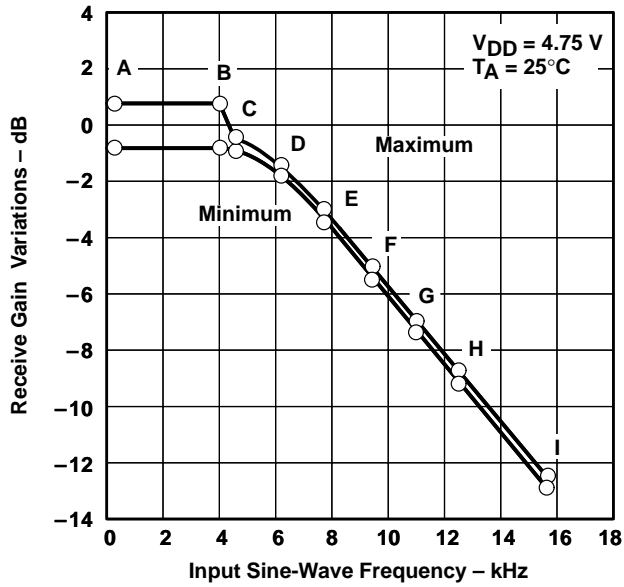
SET OF POINTS	LOCATION
A	(-70, 8)
B	(-58, 20)
C	(-53, 24)
D	(-43, 32)
E	(-35, 40)
F	(-28, 48)
G	(-13, 65)
H	(-5, 69)
I	(-1, 69)

NOTE A. The three points on the dashed line are minimum qualification standards, which every MSP58C20 must pass. The curve shows empirical data from a representative lot.

Figure 8

MAXIMUM AND MINIMUM CHARACTERISTICS

RECEIVE GAIN VARIATIONS
vs
INPUT SINE-WAVE FREQUENCY



SET OF POINTS	MIN	MAX
A	(0.156, -0.6)	(0.156, 0.6)
B	(4, -0.6)	(4, 0.6)
C	(4.6875, -0.7)	(4.6875, -0.4)
D	(6.25, -1.75)	(6.25, -1.4)
E	(7.8125, -3.35)	(7.8125, -2.9)
F	(9.375, -5.25)	(9.375, -4.8)
G	(10.9375, -7.25)	(10.9375, -6.8)
H	(12.5, -9.2)	(12.5, -8.7)
I	(15.625, -12.8)	(15.625, -12.2)

Figure 9

MSP58C20 AUDIO-BAND CONVERTER

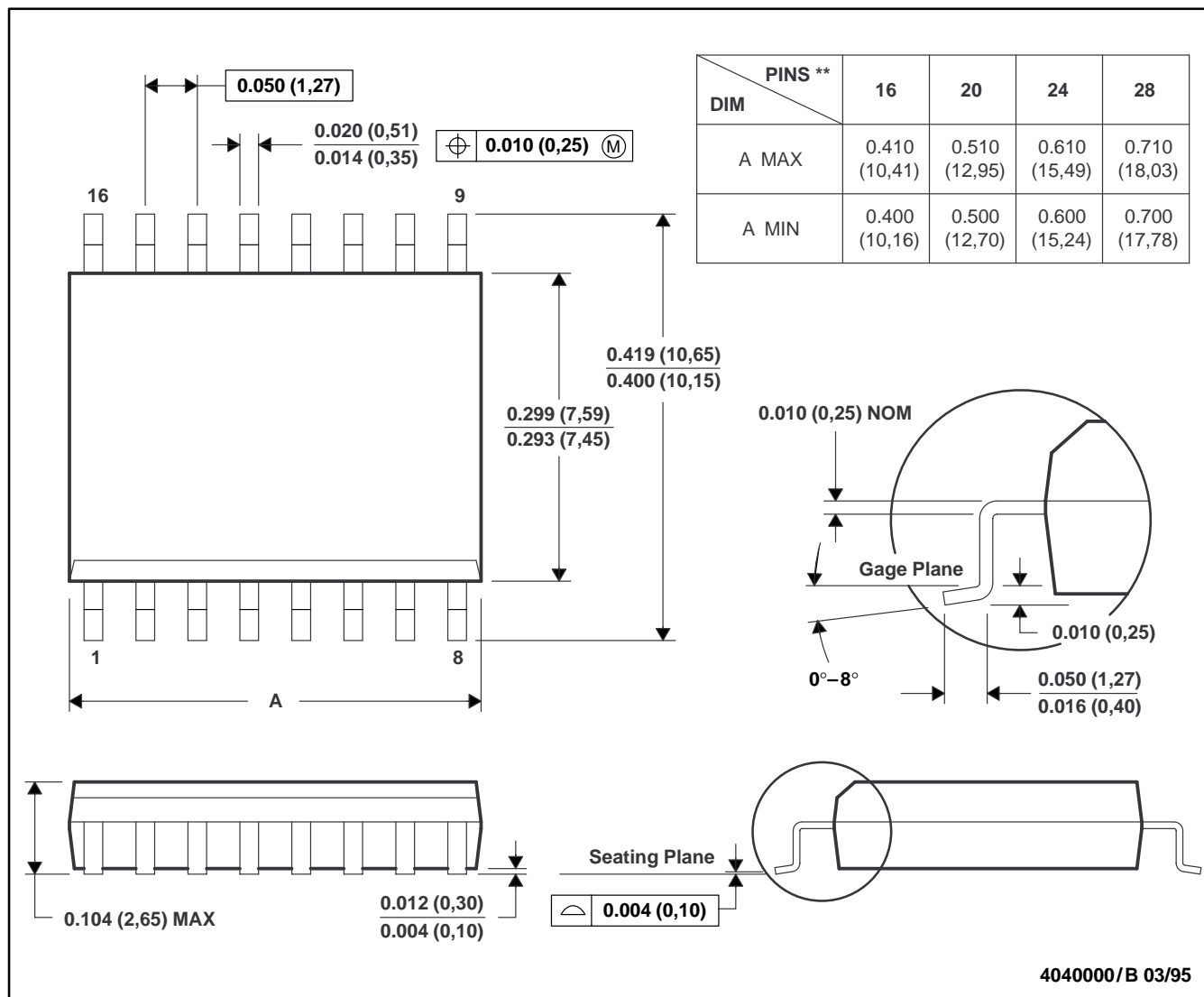
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MECHANICAL DATA

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

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