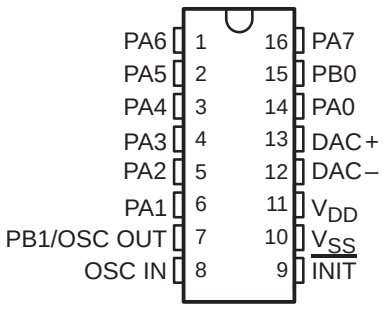
- **Dual Programmable LPC-12 Speech Synthesizers**
- **Simultaneous LPC and PCM Waveforms**
- **8-Bit Microprocessor with 61 instructions**
- **32 Twelve-Bit Words and 224 Bytes of RAM**
- **3.3V to 6.5V CMOS Technology for Low Power Dissipation**
- **Direct Speaker Drive Capability**
- **Mask Selectable Internal or External Clock**
- **Internal Clock Generator that Requires No External Components**
- **Two Software-Selectable Clock Speeds**
- **10-kHz or 8-kHz Speech Sample Rate**

**N PACKAGE**
**(TOP VIEW)**




## description

The MSP50x3x family uses a revolutionary architecture to combine an 8-bit microprocessor, two speech synthesizers, ROM, RAM, and I/O in a low-cost single-chip system. The architecture uses the same arithmetic logic unit (ALU) for the two synthesizers and the microprocessor, thus reducing chip area and cost and enabling the microprocessor to do a multiply operation in 0.8 μs. The MSP50x3x family features two independent channels of linear predictive coding (LPC), which synthesize high-quality speech at a low data rate. Pulse-code modulation (PCM) can produce music or sound effects. LPC and PCM can be added together to produce a composite result. For more information, see the MSP50x3x User's Guide (literature number SPSU006).

**Table 1. MSP50x3x Family**

| DEVICE | AMOUNT OF ROM/PROM | FEATURES |
|---|---|---|
| MSP50C32 | 16K bytes mask ROM | 9/10 I/O lines |
| MSP50C33 | 32K bytes mask ROM | 9/10 I/O lines |
| MSP50C34 | 64K bytes mask ROM | 9/10 I/O lines, 24 I/O lines in die form |
| MSP50P34 | 64K bytes PROM | 9/10 I/O lines |
| MSP50C37 | 16K bytes mask ROM | 18 I/O lines, A/D converter/analog amplifier |
| MSP50P37 | 16K bytes PROM | 18 I/O lines, A/D converter/analog amplifier |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

### absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{DD}$ (see Note 1) . . . . . –0.3 V to 8 V
Supply current, $I_{DD}$ or $I_{SS}$ (see Note 2) . . . . . 100 mA
Input voltage range, $V_I$ (see Note 1) . . . . . –0.3 V to $V_{DD}$ + 0.3 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.3 V to $V_{DD}$ + 0.3 V
Storage temperature range . . . . . –30°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground.
2. The total supply current includes the current out of all the I/O terminals and DAC terminals as well as the operating current of the device.

### recommended operating conditions (MSP50C32, MSP50C33, MSP50x34)

| | | | MAX | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage† | | 3.3 | 6.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{DD}$ = 3.3 V | 2.5 | 3.3 | V |
| | | $V_{DD}$ = 5 V | 3.8 | 5 | |
| | | $V_{DD}$ = 6 V | 4.5 | 6 | |
| $V_{IL}$ | Low-level input voltage | $V_{DD}$ = 3.3 V | 0 | 0.65 | V |
| | | $V_{DD}$ = 5 V | 0 | 1 | |
| | | $V_{DD}$ = 6 V | 0 | 1.3 | |
| $T_A$ | Operating free-air temperature | Device functionality | 0 | 70 | °C |
| Rspeaker | Minimum speaker impedance | Direct speaker drive using 2 pin push-pull DAC option | 32 | | Ω |

† Unless otherwise noted, all voltages are with respect to $V_{SS}$.

### recommended operating conditions (MSP50x37)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage† | | 4 | 6.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{DD}$ = 4 V | 3 | 4 | V |
| | | $V_{DD}$ = 5 V | 3.8 | 5 | |
| | | $V_{DD}$ = 6 V | 4.5 | 6 | |
| $V_{IL}$ | Low-level input voltage | $V_{DD}$ = 4 V | 0 | 1 | V |
| | | $V_{DD}$ = 5 V | 0 | 1.2 | |
| | | $V_{DD}$ = 6 V | 0 | 1.5 | |
| | MUX input voltage | Reference voltage = 6.5 V | 0 | 6.5 | V |
| $T_A$ | Operating free-air temperature | Device functionality | –10 | 70 | °C |
| Rspeaker | Minimum speaker impedance | Direct speaker drive using power amp | 8 | | Ω |

## MSP50C32, MSP50C33, MSP50x34 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive-going threshold voltage (INIT) | $V_{DD}$ = 3.5 V | | | 2 | | V |
| | | $V_{DD}$ = 6 V | | | 3.4 | | |
| $V_{T-}$ | Negative-going threshold voltage (INIT) | $V_{DD}$ = 3.5 V | | | 1.6 | | V |
| | | $V_{DD}$ = 6 V | | | 2.3 | | |
| $V_{hys}$ | Hysteresis ($V_{T+} - V_{T-}$) (INIT) | $V_{DD}$ = 3.5 V | | | 0.4 | | V |
| | | $V_{DD}$ = 6 V | | | 1.1 | | |
| $I_{lkg}$ | Input leakage current (except for OSC IN) | | | | | 2 | µA |
| $I_{standby}$ | Standby current ($\overline{INIT}$ low, SETOFF) | | | | | 10 | µA |
| $I_{DD}$† | Supply current | $V_{DD}$ = 3.3 V, | $V_{OH}$ = 2.75 V | | 2.1 | | mA |
| | | $V_{DD}$ = 5 V, | $V_{OH}$ = 4.5 V | | 3.1 | | |
| | | $V_{DD}$ = 6 V, | $V_{OH}$ = 5.5 V | | 4.5 | | |
| $I_{OH}$ | High-level output current (PA, PB) | $V_{DD}$ = 3.3 V, | $V_{OH}$ = 2.75 V | –4 | –12 | | mA |
| | | $V_{DD}$ = 5 V, | $V_{OH}$ = 4.5 V | –5 | –14 | | |
| | | $V_{DD}$ = 6 V, | $V_{OH}$ = 5.5 V | –6 | –15 | | |
| | | $V_{DD}$ = 3.3 V, | $V_{OH}$ = 2.2 V | –8 | –20 | | mA |
| | | $V_{DD}$ = 5 V, | $V_{OH}$ = 3.33 V | –14 | –40 | | |
| | | $V_{DD}$ = 6 V, | $V_{OH}$ = 4 V | –20 | –51 | | |
| $I_{OL}$ | Low-level output current (PA, PB) | $V_{DD}$ = 3.3 V, | $V_{OL}$ = 0.5 V | 5 | 9 | | mA |
| | | $V_{DD}$ = 5 V, | $V_{OL}$ = 0.5 V | 5 | 9 | | |
| | | $V_{DD}$ = 6 V, | $V_{OL}$ = 0.5 V | 5 | 9 | | |
| | | $V_{DD}$ = 3.3 V, | $V_{OL}$ = 1.1 V | 10 | 19 | | mA |
| | | $V_{DD}$ = 5 V, | $V_{OL}$ = 1.67 V | 20 | 29 | | |
| | | $V_{DD}$ = 6 V, | $V_{OL}$ = 2 V | 25 | 35 | | |
| $I_{OH}$ | High-level output current (D/A) | $V_{DD}$ = 3.3 V, | $V_{OH}$ = 2.75 V | –30 | –50 | | mA |
| | | $V_{DD}$ = 5 V, | $V_{OH}$ = 4.5 V | –35 | –60 | | |
| | | $V_{DD}$ = 6 V, | $V_{OH}$ = 5.5 V | –40 | –65 | | |
| | | $V_{DD}$ = 3.3 V, | $V_{OH}$ = 2.3 V | –50 | –90 | | mA |
| | | $V_{DD}$ = 5 V, | $V_{OH}$ = 4 V | –90 | –140 | | |
| | | $V_{DD}$ = 6 V, | $V_{OH}$ = 5 V | –100 | –150 | | |
| $I_{OL}$ | Low-level output current (D/A) | $V_{DD}$ = 3.3 V, | $V_{OL}$ = 0.5 V | 50 | 80 | | mA |
| | | $V_{DD}$ = 5 V, | $V_{OL}$ = 0.5 V | 70 | 90 | | |
| | | $V_{DD}$ = 6 V, | $V_{OL}$ = 0.5 V | 80 | 110 | | |
| | | $V_{DD}$ = 3.3 V, | $V_{OL}$ = 1 V | 100 | 140 | | mA |
| | | $V_{DD}$ = 5 V, | $V_{OL}$ = 1 V | 140 | | | |
| | | $V_{DD}$ = 6 V, | $V_{OL}$ = 1 V | 150 | | | |
| | Pullup resistance | Resistors selected by software and connected between terminal and $V_{DD}$ | | 10 | 20 | 50 | kΩ |
| $f_{osc(low)}$ | Oscillator frequency‡ | $V_{DD}$ = 5 V, $T_A$ = 25°C, Target frequency = 15.36 MHz | | 14.89 | 15.36 | 15.86 | MHz |
| $f_{osc(high)}$ | Oscillator frequency‡ | $V_{DD}$ = 5 V, $T_A$ = 25°C, Target frequency = 19.2 MHz | | 18.62 | 19.2 | 19.7 | MHz |

† Operating current assumes all inputs are tied to either $V_{SS}$ or $V_{DD}$ with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.

‡ The frequency of the internal clock has a temperature coefficient of approximately –0.2 %/°C and a $V_{DD}$ coefficient of approximately ±1%/V.

## MSP50x37 electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{T+}$ | Positive-going threshold voltage (INIT) | $V_{DD}$ = 4.5 V | | 2.7 | | V |
| | | $V_{DD}$ = 6 V | | 3.65 | | |
| $V_{T-}$ | Negative-going threshold voltage (INIT) | $V_{DD}$ = 4.5 V | | 2.3 | | V |
| | | $V_{DD}$ = 6 V | | 3.15 | | |
| $V_{hys}$ | Hysteresis ($V_{T+} - V_{T-}$) (INIT) | $V_{DD}$ = 4.5 V | | 0.4 | | V |
| | | $V_{DD}$ = 6 V | | 0.5 | | |
| $I_{lkg}$ | Input leakage current (except for OSC IN) | | | | 1 | µA |
| $I_{standby}$ | Standby current ($\overline{INIT}$ low, SETOFF) | | | 10 | | µA |
| $I_{DD}$† | Supply current | Power amplifier is on | | 25 | | mA |
| | | Power amplifier is off | | 10 | | |
| $I_{OH}$ | High-level output current (PA, PB, PD) | $V_{DD}$ = 4 V, $V_{OH}$ = 3.5 V | –4 | –6 | | mA |
| | | $V_{DD}$ = 5 V, $V_{OH}$ = 4.5 V | –5 | –7.5 | | |
| | | $V_{DD}$ = 6 V, $V_{OH}$ = 5.5 V | –6 | –9.2 | | |
| | | $V_{DD}$ = 4 V, $V_{OH}$ = 2.65 V | –8 | –13 | | mA |
| | | $V_{DD}$ = 5 V, $V_{OH}$ = 3.33 V | –14 | –20 | | |
| | | $V_{DD}$ = 6 V, $V_{OH}$ = 4 V | –20 | –29 | | |
| $I_{OL}$ | Low-level output current (PA4 – PA7) | $V_{DD}$ = 4 V, $V_{OL}$ = 0.5 V | 20 | 28 | | mA |
| | | $V_{DD}$ = 5 V, $V_{OL}$ = 0.5 V | 26 | 34 | | |
| | | $V_{DD}$ = 6 V, $V_{OL}$ = 0.5 V | 30 | 39 | | |
| | | $V_{DD}$ = 4 V, $V_{OL}$ = 1.33 V | 40 | 54 | | mA |
| | | $V_{DD}$ = 5 V, $V_{OL}$ = 1.67 V | 60 | 74 | | |
| | | $V_{DD}$ = 6 V, $V_{OL}$ = 2 V | 82 | 103 | | |
| $I_{OL}$ | Low-level output current (PA0 – PA3, PB, PD)) | $V_{DD}$ = 4 V, $V_{OL}$ = 0.5 V | 10 | 17 | | mA |
| | | $V_{DD}$ = 5 V, $V_{OL}$ = 0.5 V | 13 | 20 | | |
| | | $V_{DD}$ = 6 V, $V_{OL}$ = 0.5 V | 15 | 25 | | |
| | | $V_{DD}$ = 4 V, $V_{OL}$ = 1.33 V | 20 | 32 | | mA |
| | | $V_{DD}$ = 5 V, $V_{OL}$ = 1.67 V | 30 | 52 | | |
| | | $V_{DD}$ = 6 V, $V_{OL}$ = 2 V | 41 | 71 | | |
| | Pullup resistance | Resistors selected by software and connected between terminal and $V_{DD}$ | 15 | 30 | 60 | kΩ |
| $f_{osc(low)}$ | Oscillator frequency‡ | $V_{DD}$ = 5 V, $T_A$ = 25°C, Target frequency = 15.36 MHz | 14.89 | 15.36 | 15.82 | MHz |
| $f_{osc(high)}$ | Oscillator frequency‡ | $V_{DD}$ = 5 V, $T_A$ = 25°C, Target frequency = 19.2 MHz | 18.62 | 19.2 | 19.77 | MHz |

† Operating current assumes all inputs are tied to either $V_{SS}$ or $V_{DD}$ with no input currents due to programmed pullup resistors. The DAC output and other outputs are open circuited.

‡ The frequency of the internal clock has a temperature coefficient of approximately –0.2 %/°C and a $V_{DD}$ coefficient of approximately ±1.4%/V.

### MSP50x37 Power Amplifier Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Differential output power | $V_{DD}$ = 5 V, f = 1 kHz, $R_L$ = 8 Ω | | 500 | | mW |
| Bandwidth | | | | 3.5 | kHz |

### MSP50x37 ADC Electrical Characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Linearity | | ±0.5 | | LSB |
| Offset | | ±1.5 | | LSB |
| Full scale error | | ±1.5 | | LSB |
| Conversion time | | 40 | | Instructions |

### switching characteristics (MSP50C32, MSP50C33, MSP50x34)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_r$ | Rise time, PA, PB, D/A | $V_{DD}$ = 3.3 V, $C_L$ = 100 pF, 10% to 90% | | 50 | | ns |
| $t_f$ | Fall time, PA, PB, D/A | $V_{DD}$ = 3.3 V, $C_L$ = 100 pF, 10% to 90% | | 50 | | ns |

### switching characteristics (MSP50x37)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_r$ | Rise time, PA, PB, PD | $V_{DD}$ = 4 V, $C_L$ = 100 pF, 10% to 90% | | 22 | | ns |
| $t_f$ | Fall time, PA, PB, PD | $V_{DD}$ = 4 V, $C_L$ = 100 pF, 10% to 90% | | 10 | | ns |

## timing requirements

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **Initialization** | | | | | |
| $t_{INIT}$ | $\overline{INIT}$ pulsed low while the MSP50x3x has power applied (see Figure 1) | | 1 | | µs |
| **Wakeup** | | | | | |
| $t_{su(wakeup)}$ | Setup time prior to wakeup terminal negative transition (see Figure 2) | | 1 | | µs |
| **External Interrupt** | | | | | |
| $t_{su(interrupt)}$ | Setup time prior to B1 terminal negative transition (see Figure 3) | $f_{clock}$ = 15.36 MHz | 1 | | µs |
| | | $f_{clock}$ = 19.2 MHz | 1.5 | | |
| **Writing (Slave Mode)** | | | | | |
| $t_{su1(B1)}$ | Setup time, B1 low before B0 goes low (see Figure 4) | | 20 | | ns |
| $t_{su(d)}$ | Setup time, data valid before B0 goes high (see Figure 4) | | 100 | | ns |
| $t_{h1(B1)}$ | Hold time, B1 low after B0 goes high (see Figure 4) | | 20 | | ns |
| $t_{h(d)}$ | Hold time, data valid after B0 goes high (see Figure 4) | | 30 | | ns |
| $t_w$ | Pulse duration, B0 low (see Figure 4) | | 100 | | ns |
| $t_r$ | Rise time, B0 (see Figure 4) | | | 50 | ns |
| $t_f$ | Fall time, B0 (see Figure 4) | | | 50 | ns |
| **Reading (Slave Mode)** | | | | | |
| $t_{su2(B1)}$ | Setup time, B1 before B0 goes low (see Figure 5) | | 20 | | ns |
| $t_{h2(B1)}$ | Hold time, B1 after B0 goes high (see Figure 5) | | 20 | | ns |
| $t_{dis}$ | Output disable time, data valid after B0 goes high (see Figure 5) | | 0 | 30 | ns |
| $t_w$ | Pulse duration, B0 low (see Figure 5) | | 100 | | ns |
| $t_r$ | Rise time, B0 (see Figure 5) | | | 50 | ns |
| $t_f$ | Fall time, B0 (see Figure 5) | | | 50 | ns |
| $t_d$ | Delay time for B0 low to data valid (see Figure 5) | | | 50 | ns |

## PARAMETER MEASUREMENT INFORMATION

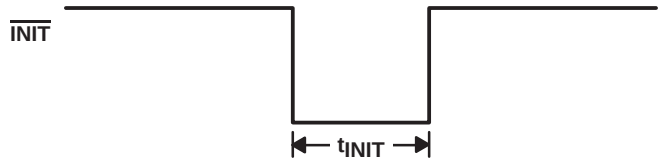



**Figure 1. Initialization Timing Diagram**

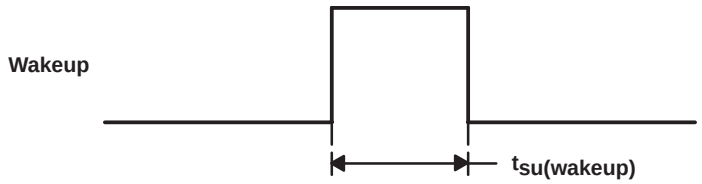



**Figure 2. Wakeup Terminal Setup Timing Diagram**

## PARAMETER MEASUREMENT INFORMATION

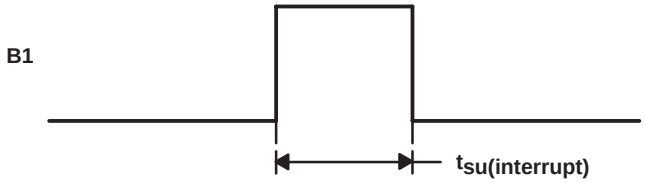



**Figure 3. External Interrupt Terminal Setup Timing Diagram**

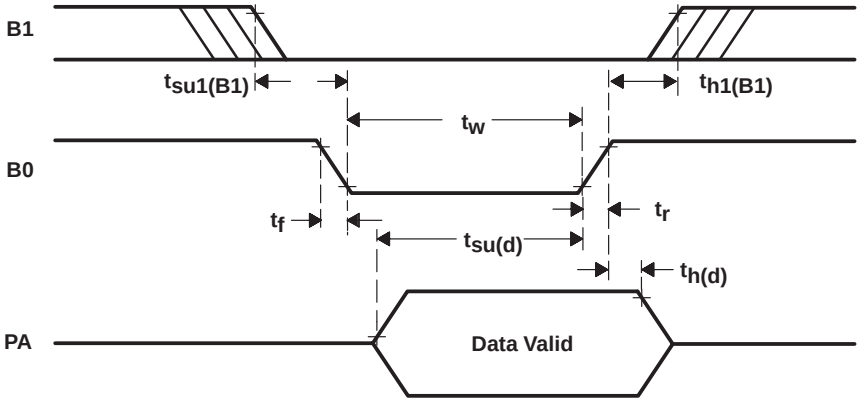



**Figure 4. Write Timing Diagram (Slave Mode)**

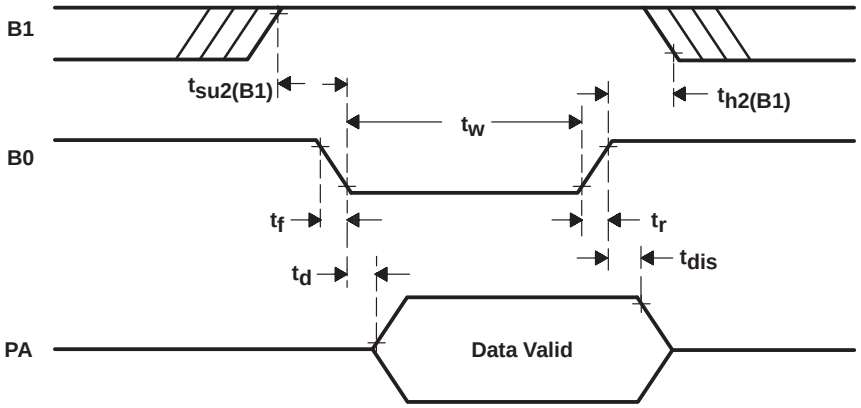


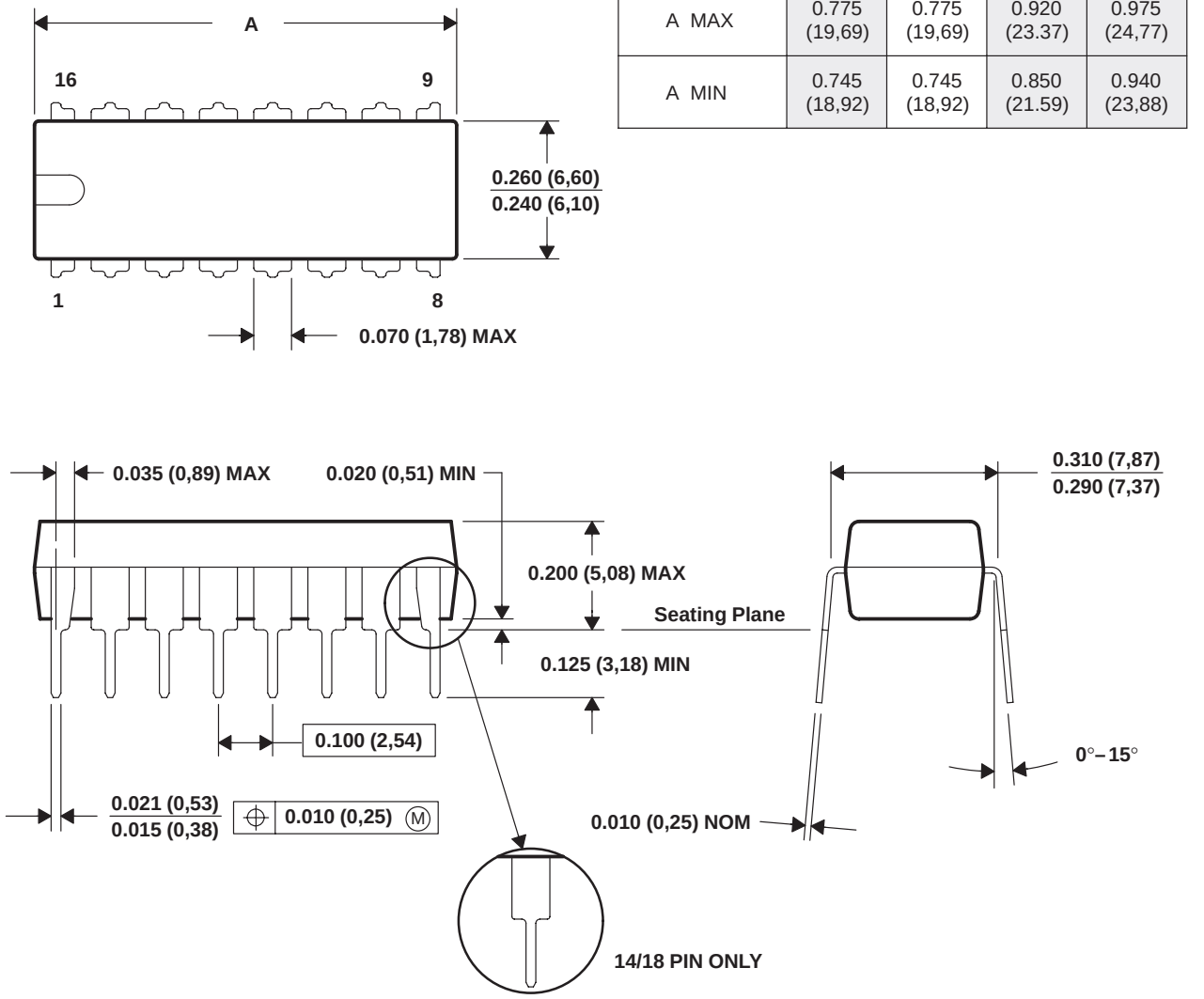

**Figure 5. Read Timing Diagram (Slave Mode)**

## MECHANICAL DATA

**N (R-PDIP-T**)** **PLASTIC DUAL-IN-LINE PACKAGE**

**16 PIN SHOWN**

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23.37) | 0.975 (24,77) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21.59) | 0.940 (23,88) |




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

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