TEXAS INSTRUMENTS

MSP50C32/33

Mixed-Signal Processors

Product Information

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Preface

Read This First

About This Manual

This document describes the MSP50C32 and MSP50C33 mixed-signal processors. This description includes a functional block diagram, a list of features, a pinout, signal descriptions, and a brief introduction to sythesized speech.

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Chapter 1

Introduction to the MSP50C32/33

The MSP50C32/33 uses a revolutionary architecture to combine an 8-bit microprocessor, two speech synthesizers, ROM, RAM, and I/O in a low-cost single-chip system. The architecture uses the same arithmetic logic unit (ALU) for the two synthesizers and the microprocessor, thus reducing chip area and cost and enabling the microprocessor to do a multiply operation in 0.8 µs. The MSP50C32/33 features two independent channels of linear predictive coding (LPC), which synthesize high-quality speech at a low data rate. Pulse-code modulation (PCM) can produce music or sound effects. LPC and PCM can be added together to produce a composite result.

Topic **Page**

1.1 MSP50C32/33 Devices

Table 1–1 lists each device with the amount of ROM included on each.

Table 1–1. MSP50C32/33 Devices

DEVICE	AMOUNT OF ROM/PROM	FEATURES
MSP50C32	16K bytes mask ROM	9/10 I/O lines
MSP50C33	32K bytes mask ROM	9/10 I/O lines

1.2 Applications

The MSP50C32/33 is highly flexible and programmable, making them suitable for a wide variety of applications. Its low system cost opens up new applications for solid-state speech. These include:

- Talking Clocks
- Toys
- Games
- Telephone Answering Machines
- Home Monitors
- Navigation Aids
- Laboratory Instruments
- Personal Computers
- Inspection Controls
- Inventory Controls
- Machine Controls
- Warehouse Systems
- Warning Systems
- Appliances
- Voice Mailboxes
- Equipment for the Handicapped
- Learning Aids
- Computer-Aided Instruction
- Magazine and Direct–Mail Advertisements
- Point-of-Sale Displays
- Talking Books

1.3 Description

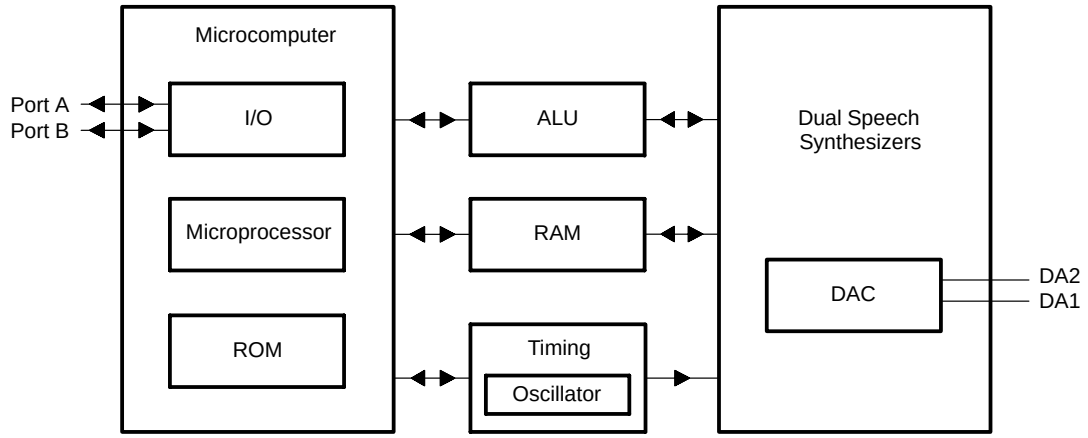
The MSP50C32/33 can be divided into several functional blocks (see Figure 1–1). The ALU and RAM are shared by the two speech synthesizers and the microcomputer.

The MSP50C32/33 implements an LPC-12 speech-synthesis algorithm using two 12-pole lattice filters. The internal microprocessor fetches speech data from the internal ROM, decodes the speech data, and sends the decoded data to the synthesizer. The microprocessor also interpolates (smooths) the speech data between fetches. The microprocessor can calculate a PCM waveform, which can be added to the output of one of the two lattice filters to create composite PCM + LPC waveforms.

The general purpose microprocessor in the MSP50C32/33 is also capable of a variety of logical, arithmetic, and control functions and can be used for the nonsynthesis tasks of the application as well.

The MSP50C32/33 family of parts incorporates a built-in oscillator and has the capability of directly driving a 32-Ω speaker.

Figure 1–1. MSP50C32/33 Functional Block Diagram



1.4 Features

The key features of the MSP50C32/33 devices are in the following bulleted list.

- Dual Programmable LPC-12 Speech Synthesizers
- Simultaneous LPC and PCM Waveforms
- 8-Bit Microprocessor with 61 instructions
- Thirty-Two 12-Bit Words and 224 Bytes of RAM
- 3.3-V to 6.5-V CMOS Technology for Low Power Dissipation
- Direct Speaker Drive Capability
- Mask-Selectable Internal or External Clock
- Internal Clock Generator that Requires No External Components
- Two Software-Selectable Clock Speeds
- 10-kHz or 8-kHz Speech Sample Rate
- Seven Levels of Stack
- Internal Timer
- Externally-Controlled Interrupt
- Single-Cycle Multiply Instruction
- Executes 1 200 000 Instructions per Second
- Built-In Slave Mode to Act as a Microprocessor Peripheral
- Software-Configurable Wake-up Function from Any A-Port I/O Line
- Two Digital-to-Analog (D/A) Configurations — Mask Selectable
- Several ROM/EPROM Configurations
  - 16K bytes for MSP50C32
  - 32K bytes for MSP50C33

1.5 D/A Options

The MSP50C32/33 devices offer two digital-to-analog (D/A) output options to match different applications. Table 1–2 gives a list of the device and the options available for each.

Table 1–2. MSP50C32/33 D/A Options

	D/A OPTIONS AVAILABLE	
DEVICE	**OPTION 1**	**OPTION 2**
MSP50C32	32-Ω speaker drive	Operational amplifier
MSP50C33	32-Ω speaker drive	Operational amplifier

1.5.1 Two-Pin Push-Pull (Option 1) — Accurate to 1 part in 1024

Option 1 is a two-pin push-pull. When direct speaker drive is not desired, it works well with a very efficient and inexpensive 4-transistor amplifier. When the digital-to-analog converter (DAC) is idle or the output value is 0, both terminals are low. When the output value is positive, DA1 pulses high with a pulse density proportional to the output value, while DA2 stays low. When the output value is negative, DA2 goes high with a pulse density proportional to the output value, while DA1 stays low. This option can respond to values ranging from –512 to +512.

Figure 1–2 shows examples of D/A output waveforms with different output values. Each sample period of the DAC is divided into 512 segments. For a positive output value, x = 0 to 512, DA1 goes high for x segments while DA2 stays high. When the DAC is idle or the output value is 0, both DA1 and DA2 are low. For a negative value x = 0 to –512, DA2 goes low for |x| segments while DA1 stays low.

Figure 1–2. D/A Output Waveforms for Two-Pin Push-Pull (Option 1)

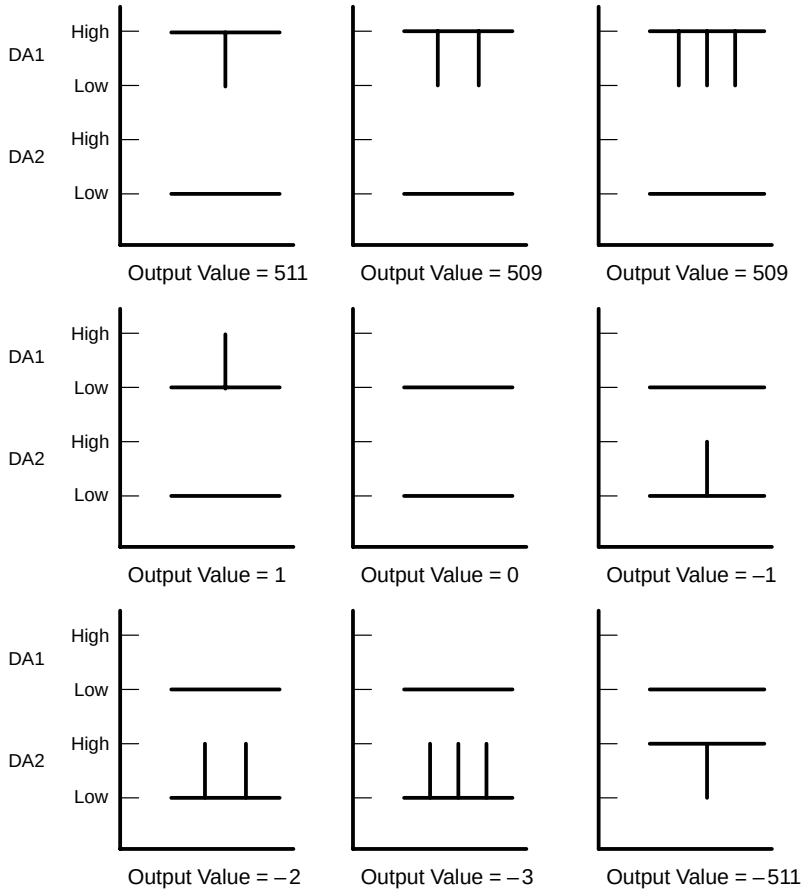


Figure 1–3, Figure 1–4, and Figure 1–5 show examples of circuits that can be used with this option.

Figure 1–3. A 4-Transistor Amplifier Circuit

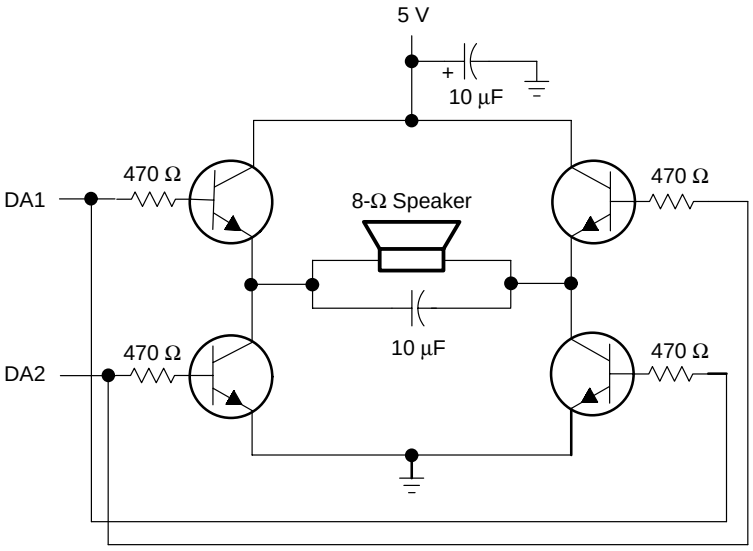


Figure 1–4. Operational-Amplifier Interface Circuit

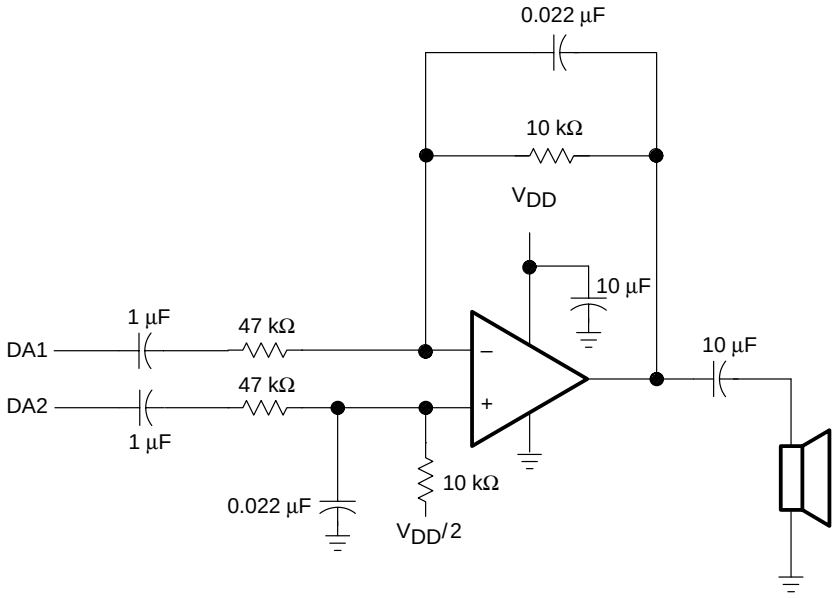
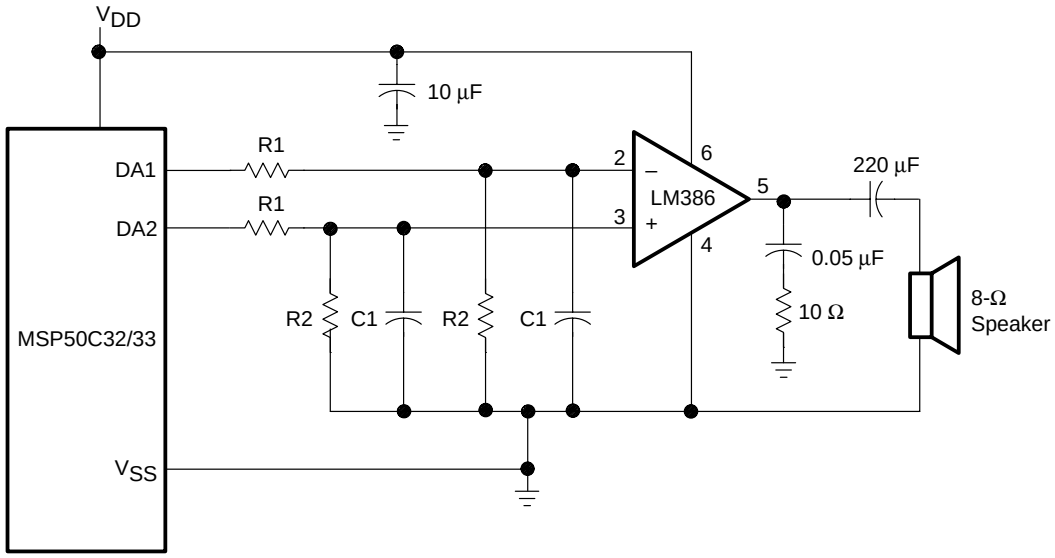


Figure 1–5. Power-Amplifier Interface Circuit



Notes
1. R1 ≈ 56 kΩ 10%
2. R2 = 2 kΩ 10%
3. C1 = 0.022 µF 20%
4. R2 and C1 set low-pass cutoff frequency: $f_c = 1/(2\pi R2 \times C1)$
5. For values given above, f_c = 3.6 kHz
6. Gain control can be added by connecting a 10-µF capacitor in series with a 10-kΩ potentiometer. This series combination is connected between terminals 1 and 8. When this is done, R1 should be increased to approximately 250 kΩ.

1.5.2 Single-Pin Double Ended (Option 2) — Accurate to 1 part in 1024

Option 2 is provided for use with operational and power amplifiers. When the output value is zero, the D/A output is biased at approximately 1/2 V_{DD}. When the output value is positive, the D/A output pulses to about 1/4 V_{DD} with a pulse density proportional to the output value. When the output value is negative, the D/A output pulses to 3/4 V_{DD} with a pulse density proportional to the output value.

Figure 1–6 shows examples of D/A output waveforms with different output values. Each pulse of the DAC is divided into 512 segments per sample period. For a positive output value x = 0 to 512, both DAC output terminals go low to 1/4V_{DD} for x segments. When the DAC is idle, or the output value is 0, both DAC output terminals stay at 1/2 V_{DD}. For a negative value x = 0 to –512, both DAC outputs go high to 3/4 V_{DD} volts for |x| segments.

Figure 1–6. Figure 1–7. D/A Output Waveforms for Single-Pin Double Ended (Option 2)

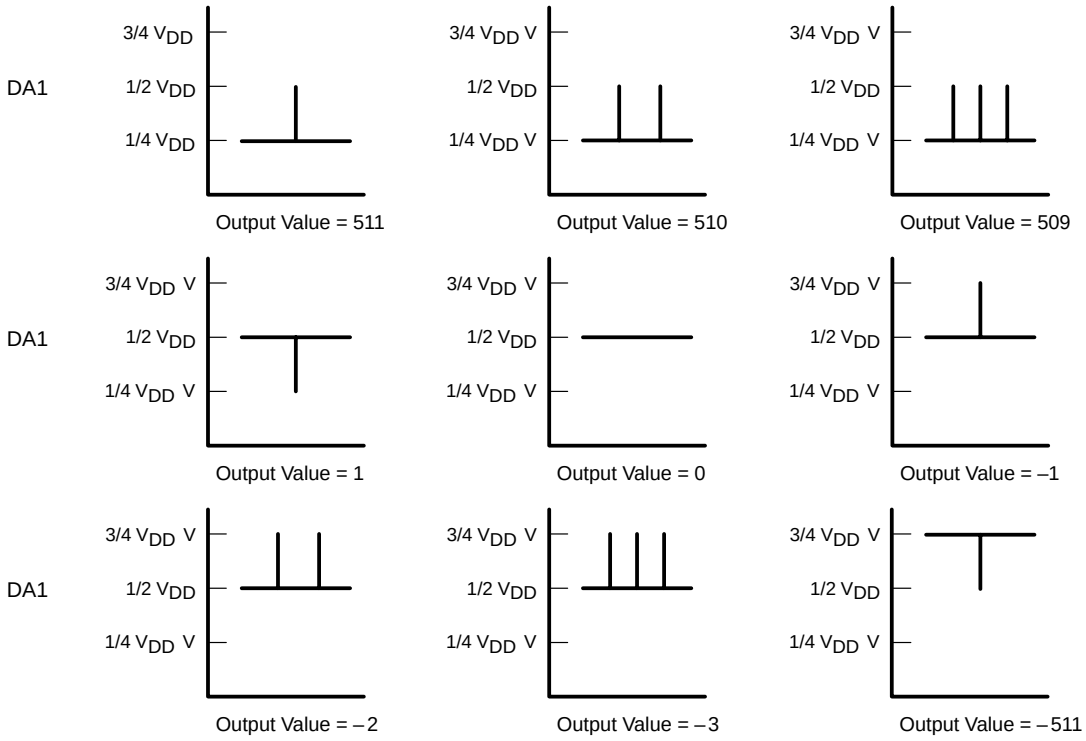
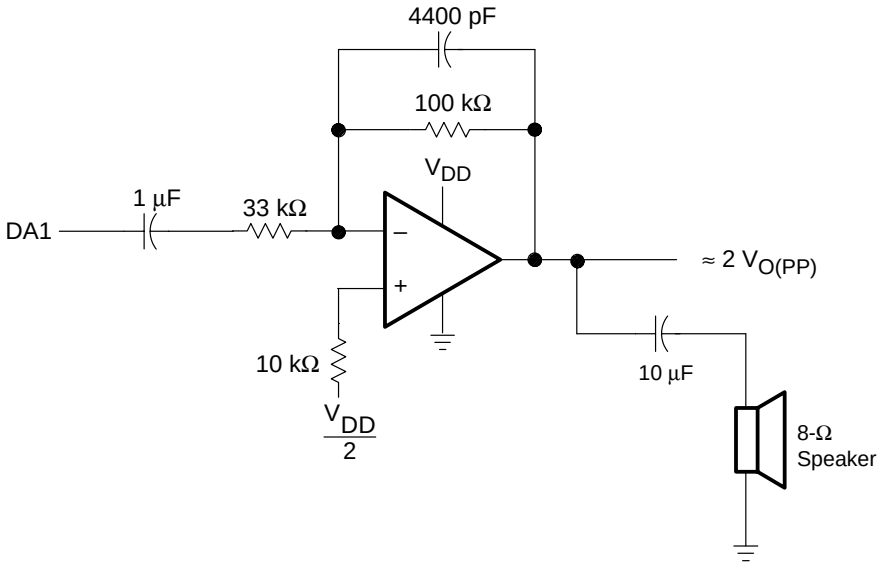


Figure 1–7 gives an example circuit that demonstrates how to interface with this output DAC option.

Figure 1–7. Operational-Amplifier Interface Circuit



1.6 Terminal Assignments and Signal Descriptions

Figure 1–8 shows the terminal assignments for the MSP50C32/33. Table 1–3 provides terminal functional descriptions. Figure 1–9 illustrates the recommended power-up initialization circuit.

Figure 1–8. Terminal Assignments

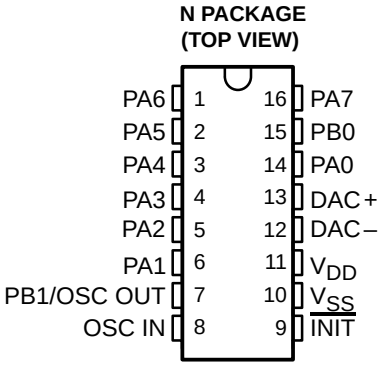
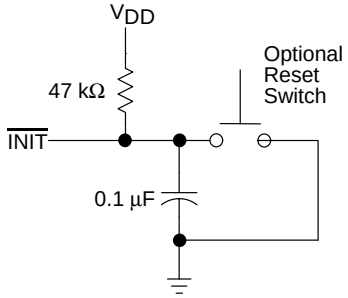


Table 1–3. MSP50C32/33 Terminal Functions

Terminal Name	Terminal Number	I/O	Signal Description
DAC+	13	O	D/A output. When D/A Option 1 is selected, this output pulses high for positive output values. It remains low when negative values are output.
DAC–	12†	O	D/A output. When D/A Options 1 is selected, this output pulses high for negative output values. It remains low when positive values are output. When D/A Option 2 is selected, this terminal is driven low.
$\overline{\text{INIT}}$	9	I	Initialize input. When $\overline{\text{INIT}}$ goes low, the clock stops, the MSP50C32/33 goes into low-power mode, the program counter is set to zero, and the contents of the RAM are retained. An $\overline{\text{INIT}}$ pulse of 1 μs is sufficient to reset the processor.
OSC IN	8	I	Clock input. When not in use, OSC should be tied to V_{SS}.
OSC OUT	7	–	Clock return. When the internal clock option is selected, this terminal is the B1 I/O terminal.
PA0–PA7	1–6, 14, 16	I/O	8-bit bidirectional I/O port
PB0–PB1	7, 15	I/O	2-bit bidirectional I/O port. When the external clock option is selected, PB1 is not available.
V_{DD}	11	–	5-V supply voltage
V_{SS}	10	–	Ground terminal

† If D/A Option 2 is selected, the DAC– terminal is asserted low.

Figure 1–9. Power-Up Initialization Circuit



1.7 Introduction to Linear Predictive Coding (LPC)

The LPC-12 system uses a mathematical model of the human vocal tract to enable efficient digital storage and re-creation of realistic speech. To understand LPC, it is essential to understand how the vocal tract works. This introduction, therefore, begins with a short description of the vocal tract, after which the LPC model and data compression techniques are addressed.

1.7.1 The Vocal Tract

Speech is the result of the interaction among three elements in the vocal tract; air from the lungs, a restriction that converts the air flow to sound, and the vocal cavities that are positioned to resonate properly.

Air from the lungs is expelled through the vocal tract when the muscles of the chest and diaphragm are compressed. Pressure is used as a volume control, with higher pressure producing louder speech.

As air flows through the vocal tract, it makes little sound if there is no restriction. The vocal cords are one type of restriction. They can be tightened across the vocal tract to stop the flow of air. Pressure builds up behind them and forces them open. This happens over and over, generating a series of pulses. The tension on the vocal cords can be varied to change the frequency of the pulses. Many speech sounds, such as the A sound, are produced by this type of restriction, which is called voiced speech.

A different type of restriction in the mouth causes a hissing sound called white noise. The S sound is a good example. White noise occurs when the tongue and some part of the mouth are in close contact or when the lips are pursed. This restriction causes high flow velocities that cause turbulence producing white noise, called unvoiced speech.

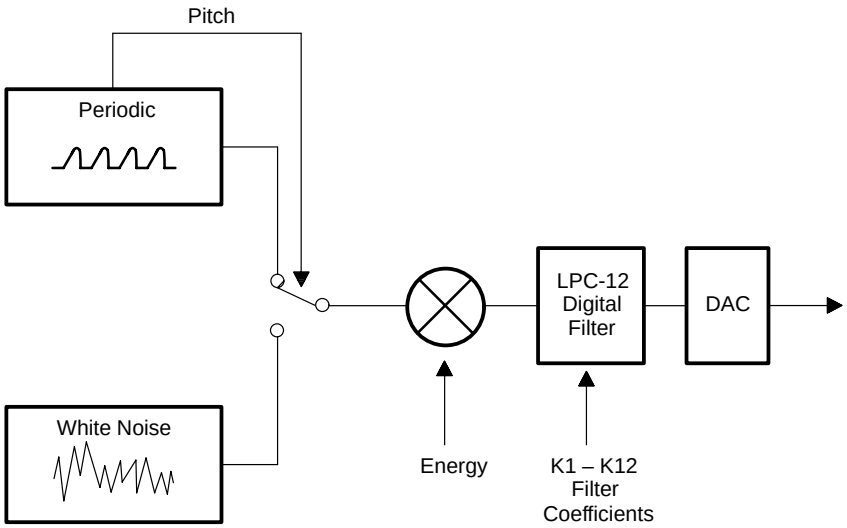
The pulses from the vocal cords and the noise from the turbulence have fairly broad, flat spectral characteristics. In other words, they are noise, not speech. The shape of the oral cavity changes noise into recognizable speech. The positions of the tongue, the lips, and the jaws change the resonance of the vocal tract, shaping the raw noise of restricted airflow into understandable sounds.

1.7.2 The LPC Model

The LPC model incorporates elements analogous to each of the elements of the vocal tract described subsection 1.7.1, *The Vocal Tract*. It has an excitation function generator that models both types of restriction, a gain multiplication stage to model the possible levels of pressure from the lungs, and a digital filter to model the resonance in the oral and nasal cavities.

Figure 1–10 shows the LPC model in schematic form. The excitation function generator accepts coded pitch information as an input and can generate a series of pulses similar to vocal cord pulses. It can also generate white noise. The waveform is then multiplied by an energy factor that corresponds to the pressure from the lungs. Finally, the signal is passed through a digital filter that models the shape of the oral cavity. In the MSP50C32/33, this filter has twelve poles, so the synthesis is referred to as LPC-12.

Figure 1–10. LPC-12 Vocal Tract Model



1.7.3 LPC Data Compression

The data compression for LPC-12 takes advantage of other characteristics of speech. Speech changes fairly slowly, and the oral and nasal cavities tend to fall into certain areas of resonance more that others. The speech is analyzed into frames generally from 10 ms to 25 ms long. The inputs to the model are calculated as an average for the entire frame. The synthesizer smooths or interpolates the data during the frame so that there is no abrupt transition at the end of each frame. Often speech changes even more slowly than the frame.

The Texas Instruments LPC model allows for a repeat frame in which the only values changed are the pitch and the energy. The filter coefficients are kept constant from the previous frame. To take advantage of the recurrent nature of resonance in the oral cavity, all the coefficients are encoded, with 3 bits to 7 bits of encoding for each coefficient. The coding table is designed so that more coverage is given to the coefficient values that occur more frequently.

1.8 Mask Options

The MSP50C32/33 can be configured to suit different applications with a variety of mask options.

1.8.1 Clock Select Option

The MSP50C32/33 family has three mask-selectable clock options. An internal oscillator; an external oscillator; or an input driven by an external clock.

The internal oscillator is recommended when the lowest-cost solution is required and the absolute accuracy of the oscillator is a secondary consideration. The internal clock is trimmed at probe to standard frequencies of 15.36 MHz and 19.2 MHz. The frequency of the internal clock may be switched between these two values by the software by setting or clearing the SPEED bit in mode register 2. When using the internal clock option, terminal 7 is available as port B1.

The external oscillator mask option is recommended when an accurate frequency standard is important. When the external oscillator mask option is selected, port B1 is not available because terminal 7 is used as the Oscillator return line. Either a ceramic resonator or quartz crystal may be connected between the OSC IN and OSC OUT lines with appropriate capacitors (see Figure 1–9) to provide the desired frequency clock. Alternatively, the OSC IN terminal may be driven with an externally derived clock signal. When the external oscillator option is used, the SPEED bit in the mode register 2 has no function. The SETOFF instruction and INIT terminal disable the operation of the clock circuit. See Figure 1–11 for a suggested oscillator circuit.

The external clock mask option is recommended when an externally derived clock is available to drive the device. A 15.36-MHz or 19.2-MHz clock should be fed to OSC IN. See Figure 1–12 for a recommended circuit for this mask option. When the external clock option is used, the SPEED bit in the mode register 2 has no function. When using the external clock option, terminal 7 is available as port B1.

Figure 1–11. Oscillator Circuit

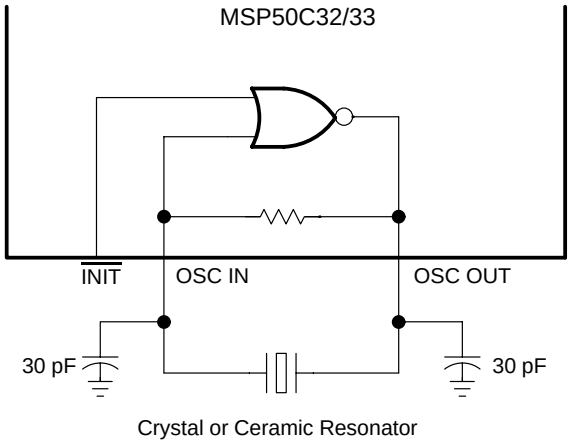
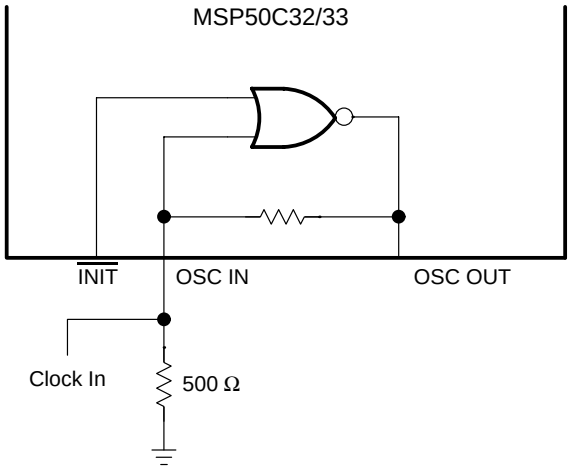


Figure 1–12. External Clock Interface



1.8.2 DAC Option

The DAC can be selected as either a two-pin push-pull or a one-pin analog. See Section 1.5 for more information.

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