Minimizing Input Design Problems with the TLV5590

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Abstract

Difficulty receiving messages on phases B and D of the FLEX™ signal while successfully receiving messages on Phases A and C usually indicates the receiver audio output is not properly interfaced to the TLV5590. The FLEX chipset requires proper consideration of the TLV5590 input interface to insure the correct digital conversion of the demodulated 4 Level FSK (Frequency Shift Keying) audio output of the RF section.

Understanding the input requirements of the TLV5590 and the typical 4 Level demodulated audio signal from the Receiver can correct this difficulty.

This application note explains these input requirements by discussing the following issues:

- General operation of the TLV5590
- Digital conversion of the 4 Level FSK audio signal
- Higher bit errors for 4 Level FSK
- Design considerations for TLV5590-Receiver interface

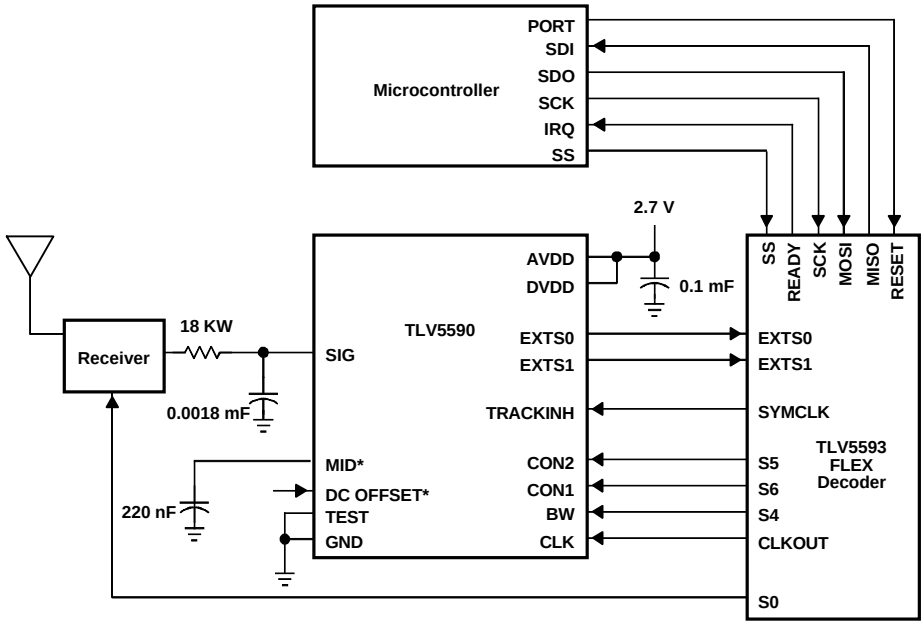
Product Support

The Texas Instruments (TI) TMS320FLEX Family Chipset with Alphanumeric Roaming Decoder simplifies implementation of the FLEX™ protocol in a messaging application by interfacing directly with most popular off-the-shelf messaging receivers and microcontrollers. You can quickly and easily develop a FLEX-compliant product by interfacing the TLV5590 converter and the TLV5593VF decoder to your existing receivers and microcontrollers with virtually no hardware redesign.

FLEX messaging protocol was developed by Motorola to provide a robust form of text and data messaging not previously available. Figure 1 shows a block diagram of a FLEX messaging device. The FLEX protocol brings new levels of functionality and service to pagers while providing you with the following benefits:

- Longer battery life than existing standards
- Support for numeric and alphanumeric messages
- High signal integrity for error protection and positive message termination
- Advanced features, such as group pages between systems
- Support for 1600-, 3200-, or 6400-bps transmissions
- Low upgrade costs by allowing gradual migration from FLEX 1600 to FLEX 3200 to FLEX 6400
- Increased number of subscribers per channel, thereby reducing infrastructure costs

Figure 1. FLEX Messaging Device Block Diagram



* The voltage on the MID terminal is nominally AVDD/2.
* The voltage applied to the DC OFFSET terminal is set to the dc offset voltage of the input signal applied to the SIG ter

FLEX Chipset Product Family

The TMS320FLEX Family includes three decoders.

- TLV5591 - an alphanumeric decoder
- TLV5593 - an alphanumeric/roaming decoder
- TLV5594 - a numeric only decoder

Each decoder is a highly optimized device that processes received and demodulated data from a FLEX transmission. Each design requires only one of these decoders. The decoder selects messages addressed to the messaging device and communicates the messages to the host. These decoders contribute to significant power savings by enabling the host microcontroller to operate in low power mode when message information is not being received. They are pin-for-pin compatible with each other which allows for easy redesign and functionality upgrade. Table 1 shows the common features of TI's FLEX decoder family.

Table 1. FLEX Decoder Family Features

	TLV5591BVF	TLV5593VF	TLV5594VF
Functionality	Alphanumeric	Alphanumeric/ Roaming	Numeric or Tone Only
Programmable Address Words	16	16	4
Bits/Sec Decoding	1600, 3200, 6400	1600, 3200, 6400	1600, 3200
Single-Phase Decoding (S) Or Any-Phase Decoding (A)	A	A	S
Low Battery Indicator	Y	Y	Y
Real -Time Clock Time Base	Y	Y	Y
Packaging	32 Pin TQFP	32 Pin TQFP	32 Pin QFP
Interfaces Gluelessly with the TLV5590 or TLV5592 converters	Y	Y	Y

Related Documentation

The following list specifies product names, part numbers, and literature numbers of corresponding TI documentation.

- *2-Bit Analog-To-Digital Converter for FLEX Pager Chipset*, Literature number SLAS134B
- *Messaging Design Manual*, Literature number SPRA086
- *TMS320FLEX1 Messaging System Solutions Design Manual (Preliminary)*, Literature number SPRA086B
- *TMS320FLEX Family Messaging System Solutions with Numeric Decoder Design Manual*, Literature number SPRA183A
- *TMS320FLEX Family Messaging System Solutions with Alphanumeric Roaming Decoder*, Literature number SPRA193A
- *TMS320FLEX Chipset Family, Putting Advanced Wireless Messaging in Reach*, Literature number SPRT135A
- *TCS320FLEX Chipset Product Brief*, Literature number SSTT004
- *1.8 Volt 2-Bit Floating Analog-To-Digital Converter for FLEX Pager Chipset*, Literature number SLAS145B

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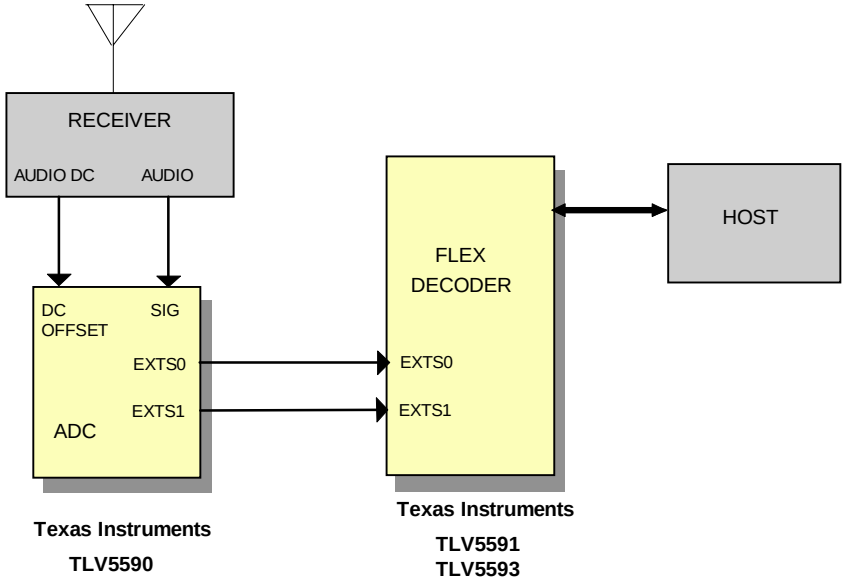
Minimizing Input Design Problems with the TLV5590

Introduction to TLV5590 Operation

Each of the TLV559x decoders is designed to function as half of a glueless chipset along with the TLV5590 analog-to-digital (A/D) converter. As a key component of the TI FLEX chipset, the TLV5590 offers developers a solution for digital demodulation of analog audio signal output of the receiver. The TLV5590 converts the 2 Level and 4 Level demodulated audio signal, generated by the receiver, to a digital baseband signal. The converted digital output is input to the FLEXchip, which decodes and processes the received data according to the FLEX protocol. The decoder provides the decoded message and status information to a Host via the SPI (Serial Peripheral Interface) bus. Figure 2 depicts this signal flow.

Figure 2. Signal Flow Block Diagram

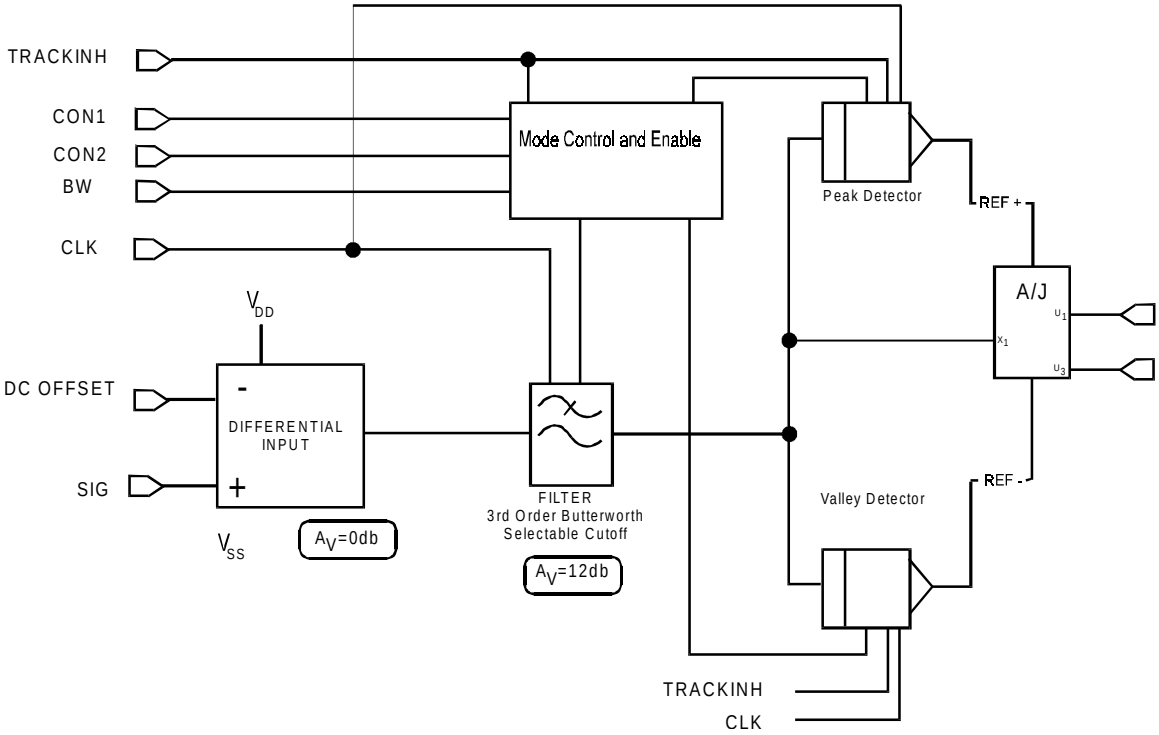


How the TLV5590 works

A simplified block diagram of the TLV5590 internal architecture is shown in Figure 3. The input signal is first processed by a 3rd order switched-capacitor Butterworth low-pass filter, whose bandwidth can be switched between 1 kHz and 2 kHz.

The filtered signal is fed to *peak* and *valley* detect circuits. These detectors are used to find and store the maximum (peak) and minimum (valley) of the signal, while the system is receiving a two-level Sync. The peak and valley detector outputs are then used as V_{ref+} and V_{ref-} for the 2 bit ADC. These detectors enable the *floating* ADC operation.

Figure 3. Simplified TLV5590 Block Diagram



The analog inputs to the TLV5590 are DC offset voltage and the baseband audio signal. Both of these analog inputs may be received from the IF IC. The DC offset voltage is used to set the midpoint of the dynamic range for the TLV5590 to ensure that no signal clipping will occur. The DC voltage applied to OFFSET is subtracted from the SIG pin to minimize the receiver offsets.

NOTE:

Some IF IC devices may not supply the DC offset voltage. In this case, a suitable reference must be used as the input. Special considerations when using this technique will be covered in subsequent paragraphs.

The TLV5590 digital outputs are available at pins EXTS0 and EXTS1. The 2 bit value at these pins represent one of 4 binary codes corresponding to the filtered 4 level input signal. The conversion output is defined as shown in Table 2 where peak denotes the peak detector voltage, valley denotes the valley detector voltage, and FILOUT represents the input signal voltage:

Table 2. 2-Bit ADC Analog Input

2-Bit ADC Analog Input	EXTS1	EXTS0
FILOUT **<** [((peak-valley) * 50/256) + valley]	0	0
[((peak-valley) * 50/256) + valley] < FILOUT < [((peak-valley) * 134/256) + valley]	1	0
[((peak-valley) * 134/256) + valley] < FILOUT < [((peak-valley) * 217/256) + valley]	1	1
[((peak-valley) * 217/256) + valley] < FILOUT	0	1

Digital Demodulation of 4 Level FSK Audio Signal

The FLEX protocol uses 4 Level FSK modulation to achieve 3200 bps and 6400 bps transmission rates. This type of FM modulation is represented in Figure 4 by carrier frequency deviations of +4800 Hz, +1600 Hz, -1600 Hz, and -4800 Hz.

Figure 4. Carrier deviations for 4 Level FSK FLEX Signaling

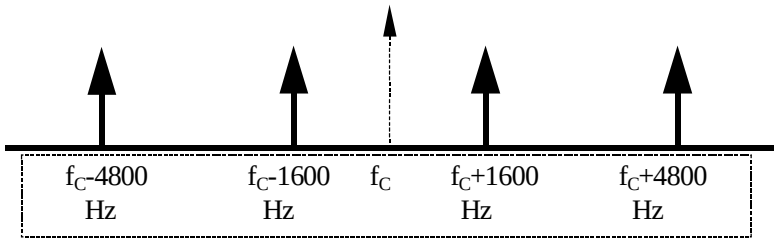
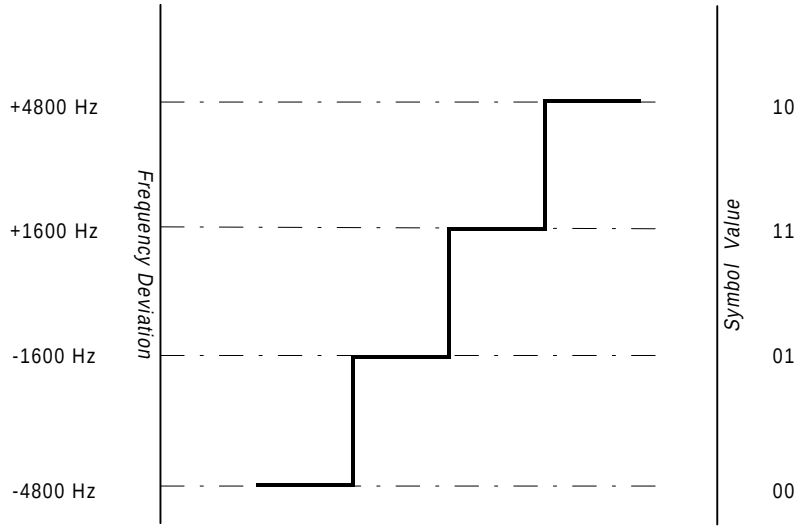


Figure 5 shows a typical 4 Level FSK output function of a discriminator type demodulator. The discriminator demodulation technique outputs an audio frequency signal. With this technique the output amplitude is proportional to the input frequency deviation.

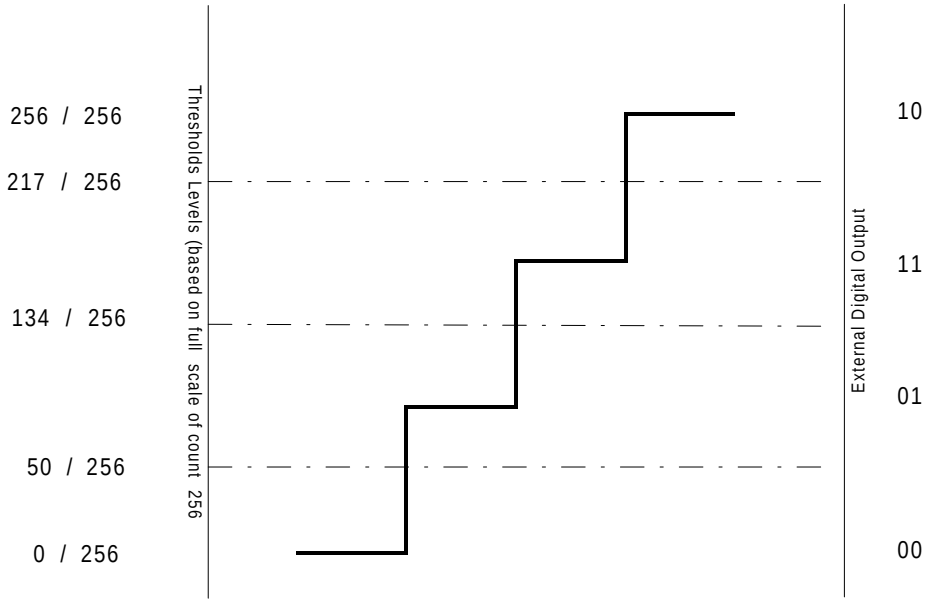
Figure 5. 4 Level FSK FLEX Audio Signaling Waveform



The TLV5590 is designed to perform digital demodulation of the 4 Level audio waveform shown in Figure 5. As discussed previously, the maximum and minimum of the input signal is detected during the 2 Level Sync portion of the FLEX signal. These voltage levels are applied to the positive and negative reference inputs of a 2 bit A/D converter. The filtered FLEX signal is then converted to a digital value based on the dynamically determined reference voltages. This makes the TLV5590 a “floating” A/D converter.

Within the 2 bit A/D converter fixed thresholds are used to determine digital value of the filtered input signal. These thresholds are based on the ratio of the input signal to the full range of the reference voltages. The full range reference voltage, Peak (maximum voltage) minus the Valley (minimum voltage), is represented as a full count of 256. Figure 6 shows the ratios used to fix the thresholds.

Figure 6. Fixed Thresholds for Digital Conversion



Explanation of Higher Bit Errors for 4 Level FSK

Bit errors in the digital output of the TLV5590 can result when the transitions shown in Figure 6 are incorrectly decoded. Since the thresholds used to perform analog to digital conversion within the TLV5590 are based on fixed ratios, clipping of the internal 2 bit ADC input can result in bit errors.

Clipping may result from:

- Excessive input amplitude at SIG input terminal;
- Improper level at DC OFFSET input terminal.

Excessive Input Amplitude at SIG Input Terminal

Referring to the block diagram in Figure 3, the output of the low-pass filter designated FILOUT must not exceed the maximum or minimum values for the internal ADC. When these values are exceeded the Peak and Valley Detectors will saturate. This means the positive and negative reference voltages for the internal ADC will be less/greater than actual peak and valley of the input. The analog to digital conversion, which is based on fixed ratio thresholds, may not correctly decode the input waveform.

Figure 7. Bit Errors Caused by Signal Clipping of FILOUT Signal

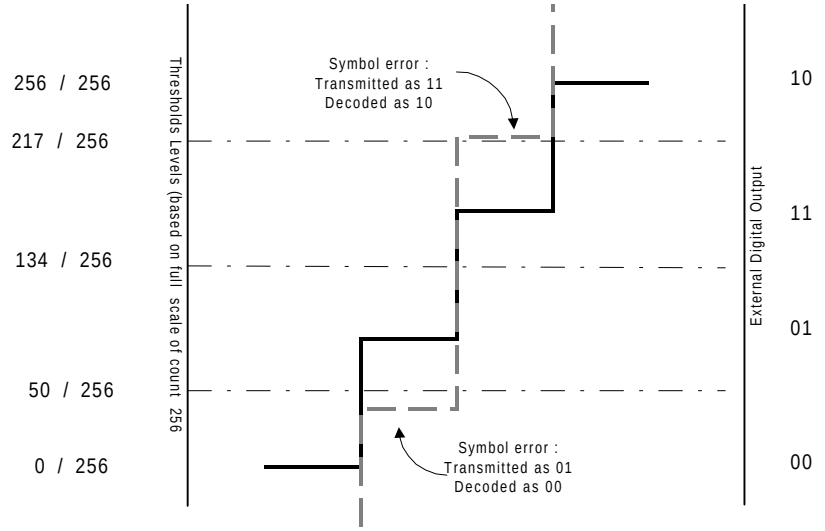


Figure 7 illustrates one example case of excessive amplitude for FILOUT. The solid line shows the normal waveform transitions without clipping. The dotted line shows the change in the waveform after the amplitude has been greatly increased. In this particular instance the amplitude is increased beyond the supply voltages. Clipping of the FILOUT signal occurs and distorts the voltage waveform proportional levels. This results in transitions out of proportion with the fixed ratio thresholds of the internal 2 bit ADC.

From this example, it can be seen that erroneous symbols will be output to the FLEX Decoder. The FLEX signal coding and blocking structure reduces the probability of more than a single bit error in this case.

In the example, the internal transitions correspond to the +/- 1600 Hz frequency deviations of the carrier. These deviations (levels) are only transmitted for 4 Level FSK. Consequently, the probability of error will be greater when 4 Level FSK data rates (6400 bps and 4 FSK 3200 bps) are used if the amplitude of the input signal results in clipping at the filter output.

Improper Level At DC OFFSET Input Terminal

The other case for clipping of the FILOUT signal occurs when the DC OFFSET input signal is not at the proper level to ensure the DC component of FILOUT is sufficiently centered at the internal midpoint voltage.

Observe in Figure 2 and Figure 3 that the SIG and DC OFFSET terminals of the TLV5590 form a differential input pair. For proper operation, the DC OFFSET input DC voltage level should be equal to the DC component of the signal at the SIG terminal. This condition allows for a FILOUT signal bias at V_{DD} / 2.

Since the 3RD order Butterworth filter has a gain of 4.217 or 12 dB, the difference between the actual DC component of the input signal at the SIG terminal and the voltage level input at the DC OFFSET terminal will be increased by this factor at the filter output. If the difference between the pair of differential inputs is so large that FILOUT maximum or minimum peak exceeds the power supply voltages limits, then the input to the 2 bit ADC will be clipped. If this clipping distorts the signal beyond the fixed ratio thresholds, bit errors may occur as discussed earlier.

Note that both of the conditions that can cause the input to the ADC to exceed the power supply limits (excessive dynamic range and improper DC offset) have a higher probability of error when the 4 Level FSK data rates are used.

Design Considerations for TLV5590-Receiver Interface

The designer can avoid problems with 4 FSK data rates by considering the dynamic range and DC level of the FILOUT signal when interfacing the Receiver to the TLV5590.

The maximum peak input to the SIG terminal is given by:

$$V_{I(PEAK)} = \frac{(V_{DD}/2) - 0.25}{4.217} - V_{I(OFFSET)} - 80mV$$

where:

$V_{DD}/2$ = the nominal output voltage at the MID terminal
$V_{I(OFFSET)} = V_Q - V_{I(DC\ OFFSET)}$
V_Q = the DC Quiescent voltage of the input signal

The term $V_{I(OFFSET)}$ is the difference of the DC component of the inputs at the SIG terminal and DC OFFSET terminal. Note that $V_{I(DC\ OFFSET)}$ is the voltage level applied the DC OFFSET terminal. In the equation, 80 mV term represents the tolerance of the midrange voltage at the filter output. ($V_{DD}/2$ - 0.25) represents the specified maximum filter output voltage.

From the above equation, it is seen that the maximum input peak will occur when $V_{I(OFFSET)}$ is equal to zero. This is achieved when the DC OFFSET input is exactly equal to the DC component of the SIG input signal. Setting $V_{I(OFFSET)}$ = 0 and substituting the nominal value of 3.0 V for V_{DD} gives:

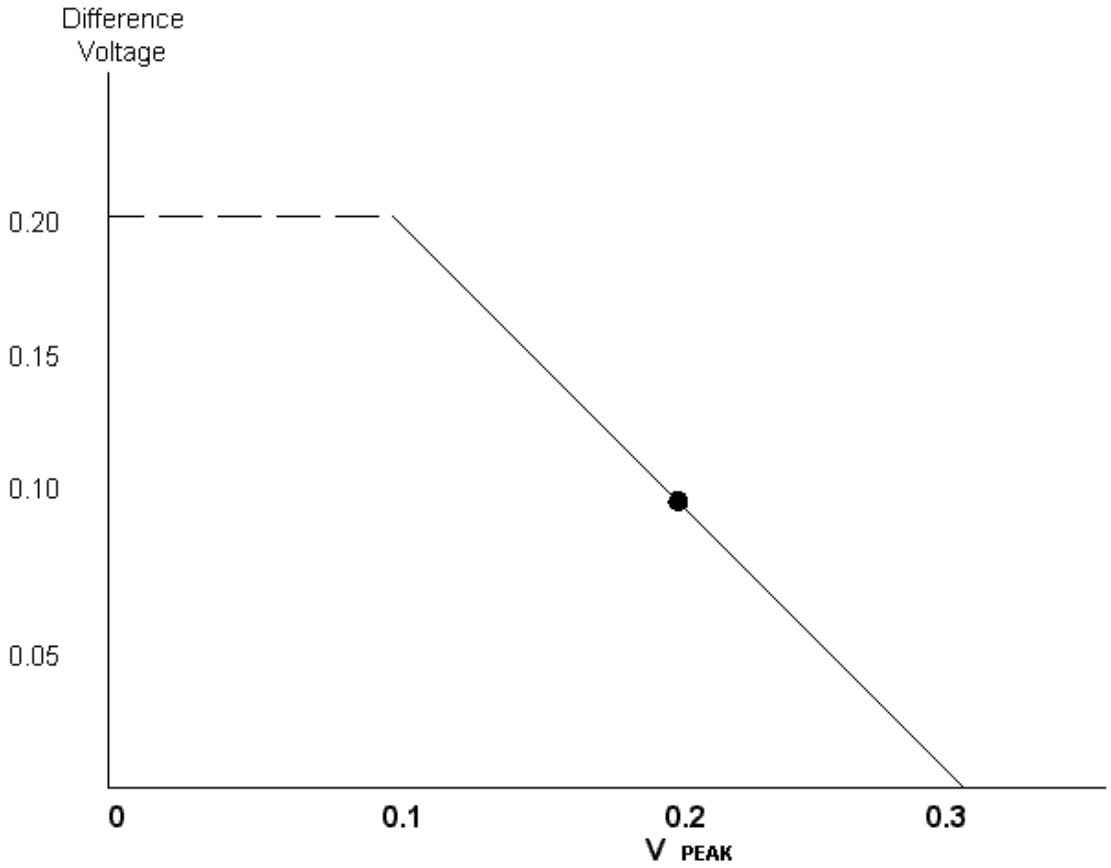
$$V_{I(PEAK)} = \frac{(3.0/2) - 0.25}{4.217} - 0 - 80mV$$

$$= 216\ mV$$

This sets the peak to peak (2X peak) input voltage limit at 432 mV.

Of course, the $V_{I(OFFSET)}$ term may vary based on the receiver interface. When the receiver provides the DC offset as an output voltage level the interface is simplified. All that is required is to connect this receiver output to the TLV5590 DC OFFSET terminal. In this case a designer should review the receiver specs to ensure the difference between the DC component of the receiver outputs (DC offset and Audio Out) is not large enough to cause clipping. The graph in Figure 8 gives the allowable difference as a function of peak input.

Figure 8. Peak Input vs. DC Offset Difference



For the most common case where the receiver does not provide a DC output, the designer must provide a reference voltage for the TLV5590 DC OFFSET input. To do so:

1) Carefully select a reference that equals the nominal DC component of the receiver's Audio Out signal.

2) Verify the difference between the maximum DC component of the Audio Out and the selected reference does not exceed allowable limits shown in Figure 8

Since the TLV5590 SIG and DC OFFSET inputs form a differential pair, the input at SIG must be scaled based on the difference between the DC component at SIG and DC OFFSET level. There is a tradeoff between the dynamic range of the input signal and the DC reference tolerance. Because of the fixed ratio thresholds and internal gain of the TLV5590 there is an optimum operating point for a 3.0 volt system. This nominal operating point is shown in Figure 8 at a peak input signal of 200 mV. This nominal value allows a 100 mV tolerance for the reference input at DC OFFSET.

Recommendations

- Scale the receiver audio output to obtain a nominal peak voltage of 200 mV (400 mV_{PP}) at the SIG terminal.
- Design the reference voltage level at the DC OFFSET terminal to equal the scaled DC component of the receiver audio output.
- Ensure this difference between the reference and DC component of the input signal will not exceed 100 mV.