Evaluation Board Documentation

TRF2050 Fractional-N / Integer-N Synthesizer

APPLICATION BRIEF: SWRA005B

Wireless Communications Business Unit

Digital Signal Processing Solutions
September 1998

TEXAS INSTRUMENTS

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Abstract

This document describes the TRF2050 evaluation board and associated software. The TRF2050 evaluation board is comprised of a multi-layer printed circuit board. The following are included to aid in the assessment of this device:

- The TRF2050 Functional Block Diagram
- The TRF2050 Evaluation Board Mechanical Outline
- The Evaluation Board Schematic
- The Evaluation Board Part List

The voltage regulators, external power, serial interface, and the external reference are explained in detail to ensure functionality of the TRF2050 evaluation board.

A DOS based software driver is supplied with the evaluation board. Once the program is executed the program screen is divided into four main sections:

- Main Loop
- Auxiliary Loop
- Device
- Editing Parameters

Common coaxial and multi-conductor connectors allow different types of external test equipment to be used with the TRF2050 evaluation board such as the following:

- The IBM Personal Computer or similar with parallel printer port
- Linear, single output power supply
- 20 MHz stable signal source for reference clock input
- Spectrum analyzer.

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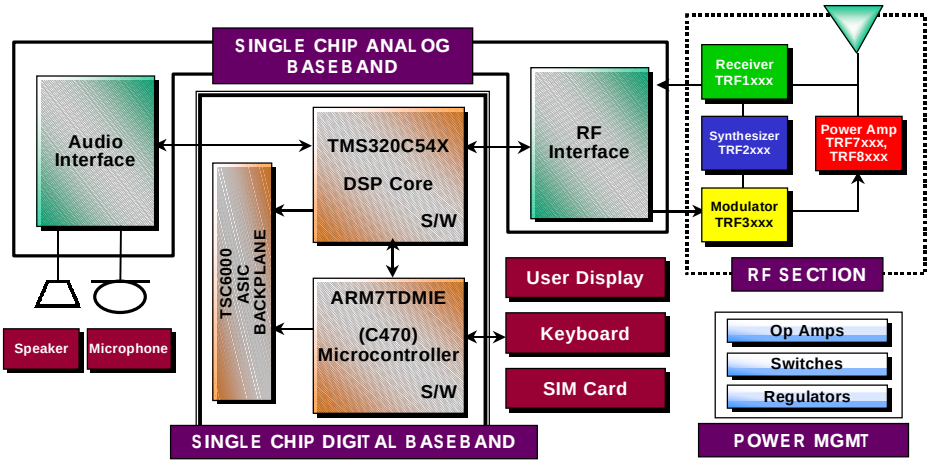

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Related Documentation

The following list specifies product names, part numbers, and literature numbers of corresponding TI documentation.

- LOW-VOLTAGE 1.2 GHz FRACTIONAL-N INTEGER-N SYNTHESIZER, Literature number SLWS030A

World Wide Web

Our World Wide Web site at www.ti.com contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

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1. Introduction

This document briefly describes the TRF2050 evaluation board and associated software. The combination of the evaluation board and software provides a means to fully exercise the TRF2050 device using common bench test equipment.

Common coaxial and multi-conductor connectors are provided on the eval board for hookup to external test equipment such as the following:

IBM Personal Computer or similar with parallel printer port,

Linear, single output power supply,

20 MHz stable signal source for reference clock input,

and Spectrum analyzer.

With the above test equipment, the TRF2050 synthesizers can be operated and characterized.

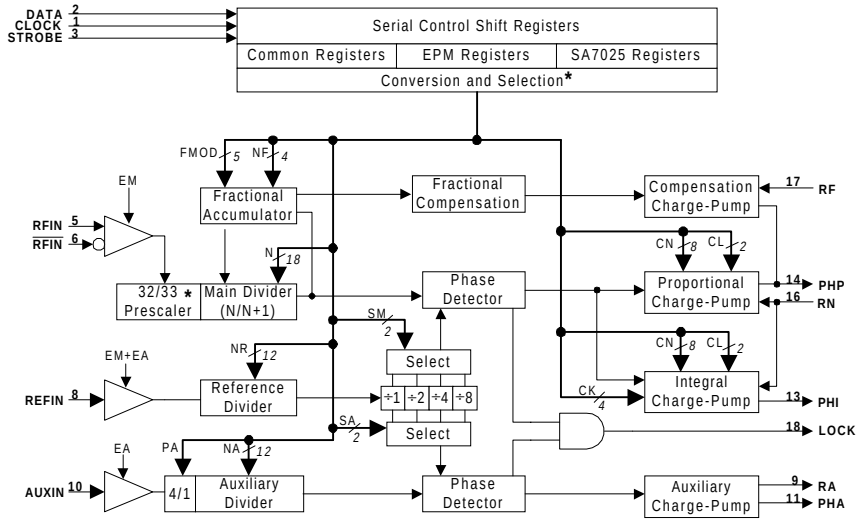
2. Evaluation Board

The TRF2050 evaluation board comprises of a multi-layer printed circuit board, TRF2050 device, main channel and auxiliary channel VCOs, opto-isolated serial interface, voltage regulation, SMA connectors, and necessary peripheral discrete components.

The main channel circuit layout supports a Murata MQE001 series VCO or similar. The auxiliary channel circuit layouts support a Vari-L VCO190-S series VCO or similar.

Figure 1 describes the TRF2050 functional block and related input/output pins of the device. Figure 2 reveals the TRF2050 evaluation board mechanical outline and Figure 3 details the TRF2050 evaluation board schematic.

Figure 1. TRF2050 Functional Block Diagram



Note: Conversion and Selection block provide emulation of SA7025 64/65/72 triple-modulus prescaler operation using the TRF2050 32/33 dual-modulus prescaler.

Figure 2. TRF2050 Evaluation Board Mechanical Outline

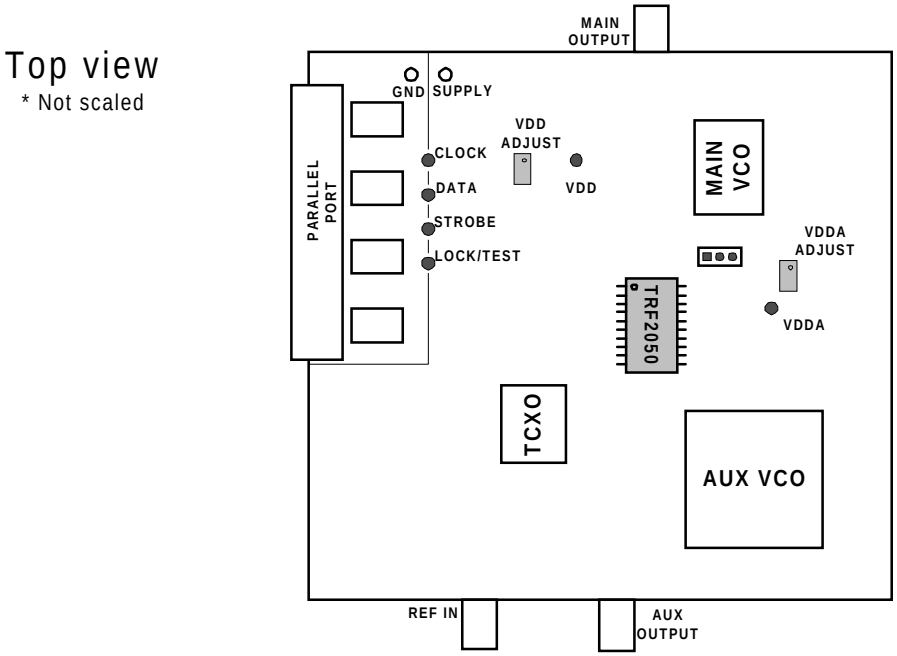
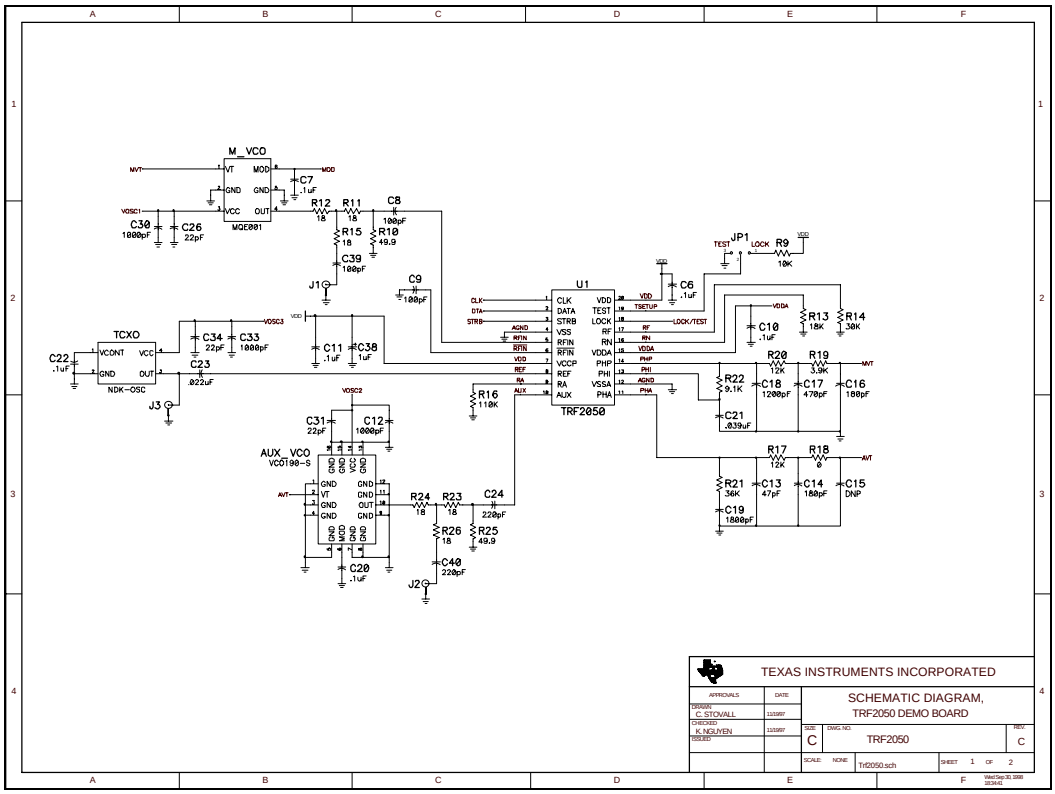


Figure 3. Evaluation Board Schematic



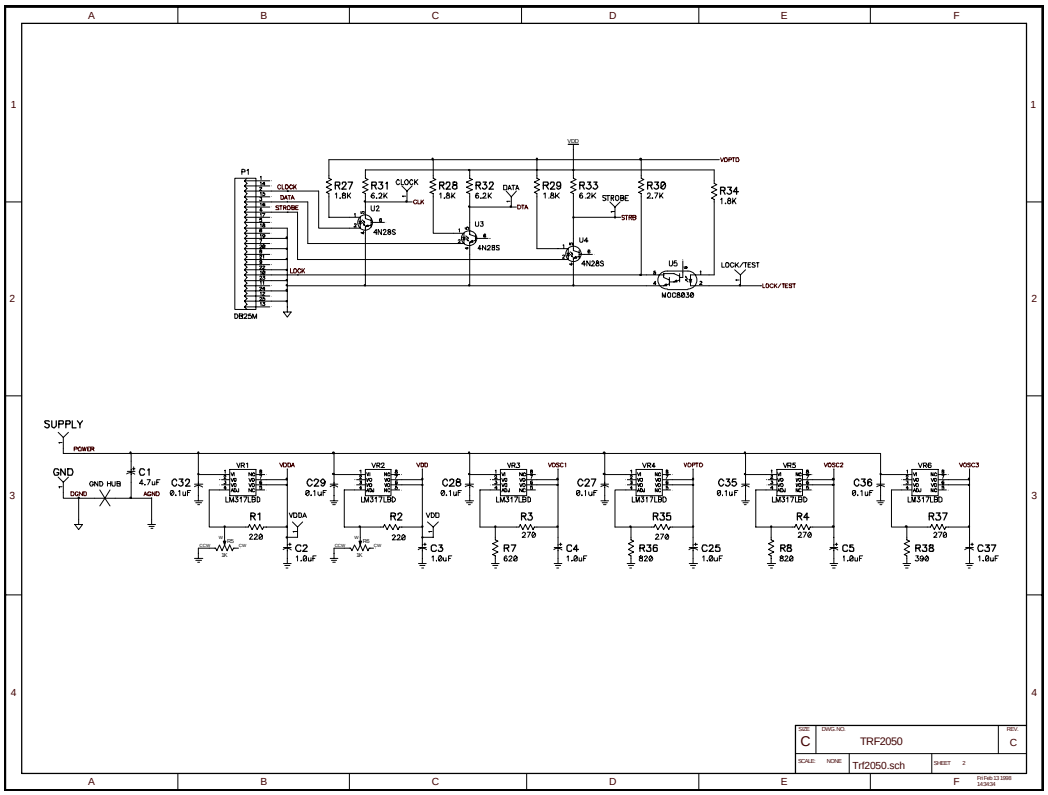


Table 1. Evaluation Board Part List

REF DESIGNATOR	VALUE	SIZE	QTY	MANU P/N	MANUFACTURER
C1	4.7 uF	"A" 3.2x1.6	1	TA010TCM Series	VENKEL
C2,3,4,5,25,37,38	1.0 uF	"A" 3.2x1.6	7	TA025TCM Series	VENKEL
C6,7,10,11,20,35,36	0.1 uF	0603 1.6x.08	7	GRM39Y5V Series	muRATA
C22,27,28,29,32	0.1 uF	0603 1.6x.08	5	GRM39Y5V Series	muRATA
C8,9,39	100.0 pF	0603 1.6x.08	3	GRM39COG Series	muRATA
C13	47 pF	0603 1.6x.08	1	GRM39COG Series	muRATA
C14,16	180.0 pF	0603 1.6x.08	2	C0603COG Series	VENKEL
C15		0603 1.6x.08	1	NOT USED	
C18	1200 pF	0603 1.6x.08	1	GRM39X7R Series	muRATA
C17	470 pF	0603 1.6x.08	1	GRM39X7R Series	muRATA
C12,30,33	1000.0 pF	0603 1.6x.08	3	GRM39X7R Series	muRATA
C19	1800.0 pF	0603 1.6x.08	1	C0603X7R Series	VENKEL
C21	0.039 uF	1210 3.2x2.5	1	ECH-U1H393JB	PANASONIC
C23	0.022 uF	0603 1.6x.08	1	GRM39X7R Series	muRATA
C24,40	220.0 pF	0603 1.6x.08	2	GRM39X7R Series	muRATA
C26,31,34	22.0 pF	0603 1.6x.08	3	GRM39COG Series	muRATA
R1,2	220.0 Ω	0603 1.6x.08	2	ERJ-3GSYJ Series	PANASONIC
R3,4,35,37	270.0 Ω	0603 1.6x.08	4	ERJ-3GSYJ Series	PANASONIC
R8,36	820.0 Ω	0603 1.6x.08	2	ERJ-3GSYJ Series	PANASONIC
R9	10.0 kΩ	0603 1.6x.08	1	ERJ-3GSYJ Series	PANASONIC
R10,25	49.9 Ω	0603 1.6x.08	2	ERJ-3EKF49R9	PANASONIC
R11,12,15,23,24,26	18.0 Ω	0603 1.6x.08	6	ERJ-3GSYJ Series	PANASONIC
R13	18.0 kΩ	0603 1.6x.08	1	ERJ-3GSYJ Series	PANASONIC
R14	30.0 kΩ	0603 1.6x.08	1	ERJ-3GSYJ Series	PANASONIC
R16	110.0 kΩ	0603 1.6x.08	1	ERJ-3GSYJ Series	PANASONIC
R17,20	12.0 kΩ	0603 1.6x.08	2	ERJ-3GSYJ Series	PANASONIC
R18	0.0 Ω	0603 1.6x.08	1	CR0603-16W-000J1	VENKEL
R19	3.9 kΩ	0603 1.6x.08	1	ERJ-3GSYJ Series	PANASONIC
R21	36.0 kΩ	0603 1.6x.08	1	ERJ-3GSYJ Series	PANASONIC
R22	9.1 kΩ	0603 1.6x.08	1	ERJ-3GSYJ Series	PANASONIC
R27,28,29,34	1.8 kΩ	0603 1.6x.08	4	ERJ-3GSYJ Series	PANASONIC
R30	2.7 kΩ	0603 1.6x.08	1	ERJ-3GSYJ Series	PANASONIC
R31,32,33	6.2 kΩ	0603 1.6x.08	3	ERJ-3GSYJ Series	PANASONIC

Evaluation Board Part List (cont.)

R5,6	1.0 kΩ	.25" SQUARE	2	3269W001102	BOURNS
R7	620 KΩ	0603 1.6x.08	1	ERJ-3GSYJ Series	PANASONIC
R38	390 Ω	0603 1.6x.08	1	ERJ-3GSYJ Series	PANASONIC
U1	Ω		1	TRF 2050	TEXAS INSTRUMENTS
U2,3,4		730C-04	3	4N28S	MOTOROLA
U5		730C-04	1	MOC8030S	MOTOROLA
VR1,2,3,4,5,6		SO-8	6	LM317LD	NATIONAL SEMICONDUCTOR
P1			1	747238-4	AMP
J1,2,3			3	142-0701-831	EF JOHNSON
TP1-TP8	Assorted		8	TP-105-01 Series	COMPONENTS CORPORATION
MAIN VCO			1	MQE001 Series	MuRata
TCXO			1	TCO-980 Series	TOYOCOM
AUX VCO			1	VCO190-S Series	VARI-L COMPANY

2.1. Voltage Regulators

The on-board regulators provide independent, linear voltage regulation to the TRF2050, the Main VCO, the Auxiliary VCO, and the serial interface opto-couplers. Regulators VR1 (VDDA) and VR2 (VDD) are adjustable using variable resistors R5 and R6 respectively. Regulators VR3 (VOSC1), VR4 (VOPTO), VR5 (VOSC2), and VR6 (VOSC3) are fixed voltage. Tantalum capacitors are used to enhance ripple and noise rejection in the regulators.

The voltage regulators are factory set as follows:

VR1 - 4.8 VDC

VR2 - 4.8 VDC

VR3 - 4.2 VDC

VR4 - 5.0 VDC

VR5 - 5.0 VDC

VR6 - 3.0 VDC

2.2. External Power

External power is connected to the evaluation board at the test points *SUPPLY* and *GND*. It is recommended that a **linear** power supply set between +7Vdc to +9 Vdc is used for external power.

2.3. Serial Interface

A DB25M connector is provided for connection to a standard PC parallel port using a 25-conductor cable. The PC parallel port is used to emulate a synchronous serial data interface consisting of *CLOCK*, *DATA*, and *STROBE*. The *LOCK* signal is fed back to the PC parallel port to indicate synthesizer loop lock status of the TRF2050. The three serial interface signals and the *LOCK* signal are all opto-isolated from the PC parallel port. In this manner, the TRF2050 device may be operated at a supply voltage that is different than the standard +5 VDC voltage level of the PC parallel port.

The serial interface signals are routed to the DB25M connector as follows:

CLOCK - Pin 2

DATA - Pin 3

STROBE - Pin 4

LOCK - Pin 10

2.4. External Reference

An external reference signal will have to be provided at SMA connector J3 (REF_IN) for operation unless a TCXO is factory installed. Typically, a low phase noise, stable, synthesized signal generator such as an HP8665 or similar should be used as an external reference. For typical AMPS/DAMPS applications, a 19.44 MHz signal at -6 dBm is suitable.

3. Software Driver

A DOS based software driver is supplied with the evaluation board. The software is intended for use in a MS-DOS environment. No special memory is required to use the software. Two files are contained on the provided disk: TRF2050.EXE and INIT.CFG. Both of these files should be placed in the same directory on a harddisk or the program may be executed from the disk provided. To execute the program from the disk provided, simply type the following.

A: *Enter*

TRF2050 *Enter*

The program executes from the TRF2050.EXE file. The INIT.CFG file is read by the program to setup the program parameters. The INIT.CFG file may be changed to suit your needs; see **F9 Save File** description.

3.1. Program Screen

The program screen is divided into four main sections: *Main Loop*, *Auxiliary Loop*, and *Device*. The *Main Loop* section displays all of the pertinent parameters concerning the main synthesizer. The *Auxiliary Loop* section displays all of the pertinent parameters concerning the auxiliary synthesizer. The *Device* section displays all of the pertinent parameters concerning the device enables, modes, and reference frequency. And the bottom two lines of the display suggest appropriate keys to use or actions to take based on the user inputs.

3.1.1. Main Loop Section

The main loop section displays the current main synthesizer loop parameters. All parameters displayed in the main loop section can be modified except for *Phase Detector Freq* and *Channel Spacing,* which are informative only. These two parameters are calculated from the reference frequency (*Refrnc Freq*) and reference counter (*Reference Count NR*) parameters in the *Device* section and the fractional modulus (*Frctnl Modulus FMOD*) parameter in the *Main Loop* section.

3.1.1.01. VCO Frequency

The main *VCO Frequency* parameter is not actually a TRF2050 device parameter but may be used to cause the program to automatically find a solution, if possible, for *N* (*EPM* mode only), *NM1-NM3* (*SA7025* mode only), and *NF* based on the entered *VCO frequency* parameter and others. The correct reference frequency (*Refrnc Freq)*, reference count (*NR*), and fractional modulus (*FMOD*) should be entered before using the *VCO Frequency* parameter to calculate a channel solution.

3.1.1.02. Prescaler (Prsclr PR)

The *PR* field selects the desired main synthesizer prescaler configuration when the device is operated in *SA7025* mode. The choices are:

PR = 1	64/65 modulus prescaler,
PR = 2	64/65/72 modulus prescaler.

When the device is operated in *EPM* mode, the *PR* field is not programmable and the prescaler is configured as a 32/33 modulus prescaler.

3.1.1.03. Fractional Numerator (Frctnl Numerator NF)

The *NF* field selects the numerator value for the fractional accumulator circuit of the main synthesizer. This value can be manually programmed to any valid desired value. *NF* is also automatically updated when the *VCO Frequency* field is used to enter the desired main synthesizer channel frequency or when the *FMOD* field is changed.

3.1.1.04. Fractional Modulus (Frctnl Modulus FMOD)

The *FMOD* field selects the desired main synthesizer fractional accumulator denominator modulo value. The valid choices based on the operation mode of the TRF2050 are as follows:

FMOD = 0	modulo-5	*SA7025* mode,
FMOD = 1	modulo-8	*SA7025* mode,
FMOD = 1-16	modulo-1-16	*EPM* mode.

When the *FMOD* field is changed, the routine to calculate the proper main synthesizer channel coefficients is called.

3.1.1.05. Main Charge Pump Current (Main Chrgpmp I CN)

The *CN* field selects the main synthesizer charge pump current gain coefficient.

3.1.1.06. Reference Select SM (Rfrnc Select SM)

The *SM* field selects the main synthesizer reference postscaler select as follows:

SM = 0 Reference/1,

SM = 1 Reference/2,

SM = 2 Reference/4,

SM = 3 Reference/8.

3.1.1.07. NM1-3 (SA7025 mode)

The *NM1-3* fields can be programmed manually to any valid number. These fields are also automatically updated when the *VCO Frequency* field is used to enter the desired main synthesizer channel frequency or when the *FMOD* field is changed.

3.1.1.08. N (EPM mode)

The *N* field can be programmed manually to any valid number. This field is also automatically updated when the *VCO Frequency* field is used to enter the desired main synthesizer channel frequency or when the *FMOD* field is changed.

3.1.1.09. Proportional Charge Pump Current (Prprtnl Chrgpmp I CL)

The *CL* field selects the main synthesizer speed-up mode, proportional charge pump current gain coefficient.

3.1.1.10. Integral Charge Pump Current (Intgrl Chrgpmp I CK)

The *CK* field selects the main synthesizer speed-up mode, integral charge pump current gain coefficient.

3.1.1.11. Chargepump Polarity(Chrgpmp Plrty MCP) (EPM mode)

The *MCP* field selects the main synthesizer charge pump current polarity when in *EPM* mode as follows:

MCP = 0 positive polarity,

MCP = 1 negative polarity.

3.1.1.12. Strobe Pulsewidth (Strobe PWth) (SA7025 mode)

The *Strobe PWth* field may be used to vary the pulse width of the serial interface *STROBE* signal. This feature is used to regulate speed-up mode when operating the device in *SA7025* Mode. A value of approximately 7500-9500 for *Strobe Pwth* provides for a 600us *STROBE* pulse width which will vary based on the microprocessor speed of the PC executing the program.

3.1.1.13. Speedup Time G (EPM mode)

The *G* field selects the duration of speedup mode when in *EPM* mode. The duration of speedup mode is determined as detailed in table 2 below.

Table 2: Speedup Mode Duration

G Value	$Duration_{EPM}$
0-14	$[(G+1) * NR * SM * 16] / f_{REFIN}$
15	$< (NR * SM) / (f_{REFIN} / 2)$; which is less than ½ a phase detector cycle.

3.1.2. Auxiliary Loop Section

The auxiliary loop section displays the current auxiliary loop parameters. All parameters displayed in the auxiliary loop section can be modified except for *Phase Detector Freq*. This parameter is calculated from the reference frequency (*Refrnc Freq*) and reference counter (*Reference Count NR*) parameters in the Device section.

3.1.2.01. VCO Frequency

The auxiliary *VCO Frequency* parameter is not actually a TRF2050 device parameter but may be used to cause the program to automatically find a solution, if possible, for *NA* based on the entered VCO frequency parameter and others. The correct reference frequency (*Refrnc Freq)* and reference count (*NR*) should be entered before using the *VCO Frequency* parameter to calculate a channel solution.

3.1.2.02. Reference Select (Refrnc Sel SA)

The *SA* field selects the auxiliary synthesizer reference postscaler select as follows:

SA = 0 Reference/1,

SA = 1 Reference/2,

SA = 2 Reference/4,

SA = 3 Reference/8.

3.1.2.03. Chargepump Polarity (Chrgpmp Plrty ACP) (EPM mode)

The *ACP* field selects the auxiliary synthesizer charge pump current polarity when in *EPM* mode as follows:

ACP = 0 positive polarity,

ACP = 1 negative polarity.

3.1.3. Device Section

The device section displays the current device parameters. All parameters displayed in the device section can be modified except *Synthesizer Status* which is a read-back from the *Lock* terminal on the TRF2050 device.

3.1.3.01. Main Divider Enable EM

The *EM* field enables/disables the main synthesizer as follows:

EM = 0 disabled,

EM = 1 enabled.

3.1.3.02. Auxiliary Divider Enable EA

The *EA* field enables/disables the main synthesizer as follows:

EA = 0 disabled,

EA = 1 enabled.

3.1.3.03. Device Mode ALT

The device mode parameter selects the fundamental operating mode of the TRF2050. The TRF2050 main synthesizer will emulate an SA7025 in *SA7025* mode and has additional features in *Enhanced Performance Mode (EPM*). Note changes in the main loop section when switching device modes.

ALT = 0 *SA7025* mode,

ALT = 1 *EPM* mode.

3.1.3.04. Device Test T

The device test *T* field is used to select between the four test mode parameters of the device and should be set to zero for normal lock detect operation.

When the Tsetup pin is tied to ground, the T word selects the output of the Lock/Test pin:

T	output
00	Buffered Accumulator out
01	Buffered Aux divider out
10	Buffered Main divider out
11	Buffered Reference divider out

The test modes can be used to verify proper main divider, reference divider, auxiliary divider, and accumulator operation.

3.1.3.05. Reference Frequency (Refrnc Freq)

The external reference frequency used with the evaluation board should be entered in this location in order that other parameters such as phase detector reference frequency and channel spacing can be properly calculated and displayed.

3.1.3.06. Reference Count NR

The *NR* field selects the division ratio of the reference frequency counter.

3.1.3.07. A-word Mode Long

The *Long* field selects between two A-word bit-length programming schemes as follows:

Long = 0 A-word = 24 bits,

Long = 1 A-word = 32 bits.

The *Long* A word allows the uses to change both *CN* and the main loop frequency.

3.1.3.08. Synthesizer Status

The *Synthesizer Status* is a read-back only field that reflects the current status of the Lock terminal.

3.1.4. Editing parameters

To edit any one of the program parameters displayed, the user first selects an appropriate function key (described below) to select a section of the display such as the Main Loop section. The arrow *(←, ↑, →, ↓)* and Tabulation (*TAB*) keys are used to move the cursor to the parameter to be edited. Once the cursor is located at the proper location, press *Enter* (or *Return*) to select the parameter. Next, enter the new value and press Enter again. Once all of the parameters within a particular section of the display have been edited as desired, press the Escape (*ESC*) key to return to the main menu.

For example, to edit the *Strobe Pwth* parameter in the *Main Loop* section from the main menu when in *SA7025* mode, the following keystrokes are performed:

1) F1 to select the Main Loop section
2) → to move to the right column
3) ↓ to move down the right column
4) ↓ to move down the right column
5) ↓ to move down the right column
6) ↓ to move down the right column
7) ↓ to move down the right column
8) Enter to select the Strobe Pwth field
9) Data enter the desired data such as 9500
10) Enter to complete the field edit
11) ESC to leave the Main Loop section and return to the main menu

3.1.4.01. Function Keys

Function keys are used to select sections of the display for editing purposes or to perform a program function as follows:

F1: Edit PLL #1 - Selects the M*ain Loop* section of the display for editing.

F2: Edit PLL #2 - Selects the *Auxiliary Loop* section of the display for editing.

F4: Edit Device - Selects the *Device* section of the display for editing.

F5: View Bit Map - Used to view the current multi-word bitmap.

F7: Select Port - Used to select the PC parallel port. This function “looks” at the ROM BIOS to find all parallel ports. Follow the directions to select a particular port if more than one is found.

F8: Load File - Used to load a configuration file to reset the program parameters to a user specified condition. This function will look for the entered file on the same disk and in the same directory from which the program is executing. Any existing, allowable DOS name can be used. The INIT.CFG file may also be loaded using this function to restore to original program configuration.

F9: Save File - Used to save a configuration file containing the current program parameters to a user specified file. This function will write the program parameters to the specified file name on the same disk and in the same directory from which the program is executing. Any allowable DOS name can be used. The INIT.CFG file may also be re-written using this function to change the boot program configuration.

F10: Send to Device - Used to program the TRF2050 device. When F10 is selected, the current bitmap is displayed and the user enters the letter (A, B, C, D, E) of the word to be sent to the TRF2050. The default sequence of D, C, B, and A in order can be sent to the TRF2050 by simply pressing *Enter* without first selecting a letter.

3.1.4.02. Quitting the Program

CTL-Q: Quit - The Control *(Ctrl)* key is depressed and held while the *Q* key is pressed to exit the program and return to DOS.

4. Switching Speed Measurements

Figures 4 and 5 illustrate the measured switching speed of the TRF2050 EVM board utilizing the speed-up mode. It should be noted that the TRF2050 should not be allowed to remain in speedup mode long enough to acquire phase lock. If this occurs, the circuit will momentarily break lock when transitioning from speedup to normal mode due to the integral charge pumps shutting off and the proportional charge pumps changing their current gain setting. Based on this, the optimal value of G should be characterized for any given application and should also vary proportionally with the magnitude of the frequency delta.

The measurements were taken using an HP89441A Vector Signal Analyzer with the strobe line used as a trigger.

The software settings are as follows:

CN = 64

Mode = EPM

FMOD = 8

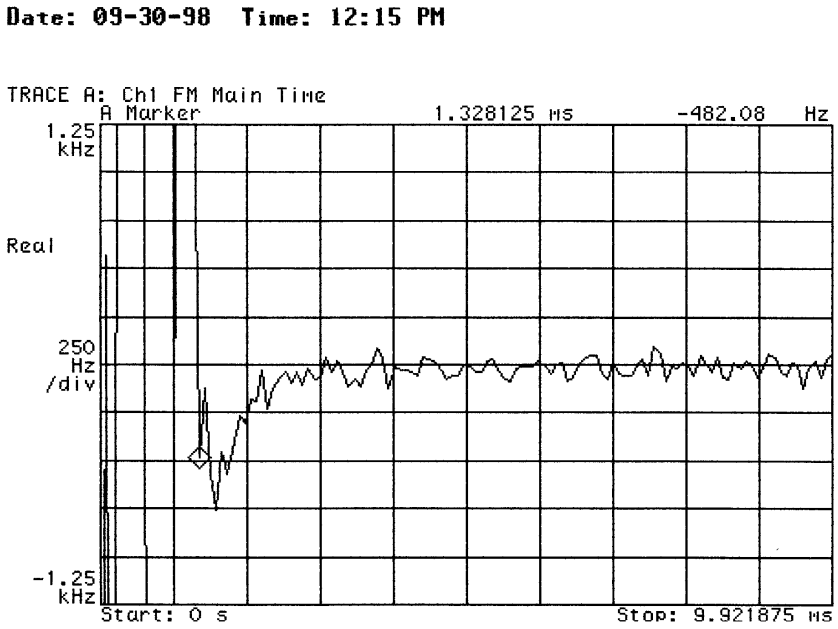
CL = 1

CK = 3

Phase Detector Frequency = 240 kHz

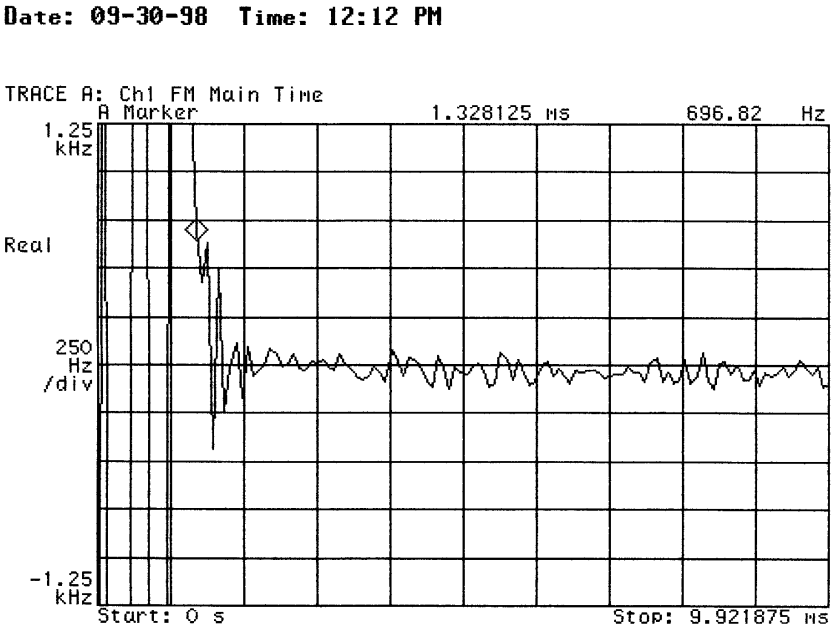
(Note: The value of G is specific to each switching measurement.)

Figure 4. Low to High Switching Time



(914.19 MHz to 939.15 MHz within 1 kHz, G = 7)

Figure 5. High to Low Switching Time



(939.15 MHz to 914.19 MHz within 1 kHz, G = 10)

5. Special Notes

Note that the *FMOD* field in the *Main Loop* section of the screen will have to be modified when switching between *SA7025* and *EPM* modes. The user should also re-enter the desired *VCO Frequency* in the *Main Loop* section after switching between *SA7025* and *EPM* modes and after correctly setting the *FMOD* field to ensure that the *NM1-NM3 (SA7025)* and *N (EPM)* parameter calculations are current.

Evaluation Board Disclaimer

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