- **PCI Bus Power Management Interface Specification 1.0 Compliant**
- **ACPI 1.0 Compliant**
- **Fully Compatible With the Intel™ 430TX (Mobile Triton II) Chipset**
- **Packaged in 208-Pin TQFP**
- **PCI Local Bus Specification Revision 2.1 Compliant**
- **1995 PC Card™ Standard Compliant**
- **3.3-V Core Logic With Universal PCI Interfaces Compatible With 3.3-V and 5-V PCI Signaling Environments**
- **Mix-and-Match 5-V/3.3-V PC Card16 Cards and 3.3-V CardBus Cards**
- **Supports Two PC Card or CardBus Slots With Hot Insertion and Removal**
- **Uses Serial Interface to TI™ TPS2202/2206 Dual-Slot PC Card Power Switch**
- **Supports Burst Transfers to Maximize Data Throughput**
- **Supports Parallel PCI Interrupts, Parallel ISA IRQ and Parallel PCI Interrupts, Serial ISA IRQ With Parallel PCI Interrupts, and Serial ISA IRQ and PCI Interrupts**
- **Serial EEPROM Interface for Loading Subsystem ID and Subsystem Vendor ID**
- **Pipelined Architecture Allows Greater Than 130M-Bytes-Per-Second Throughput From CardBus to PCI and From PCI to CardBus**
- **Supports Up to Five General-Purpose I/Os**
- **Programmable Output Select for $\overline{\text{CLKRUN}}$**
- **Multifunction PCI Device With Separate Configuration Space for Each Socket**
- **Five PCI Memory Windows and Two I/O Windows Available for Each PC Card16 Socket**
- **Two I/O Windows and Two Memory Windows Available to Each CardBus Socket**
- **Exchangeable Card Architecture (ExCA) Compatible Registers Are Mapped in Memory and I/O Space**
- **Intel 82365SL-DF Register Compatible**
- **Supports Distributed DMA (DDMA) and PC/PCI DMA**
- **Supports 16-Bit DMA on Both PC Card Sockets**
- **Supports Ring Indicate, $\overline{\text{SUSPEND}}$, PCI $\overline{\text{CLKRUN}}$, and CardBus $\overline{\text{CCLKRUN}}$**
- **LED Activity Pins**
- **Supports PCI Bus Lock ($\overline{\text{LOCK}}$)**
- **Advanced Submicron, Low-Power CMOS Technology**
- **For the Complete Data Sheet for PCI1220, Please See Literature #SCPS016**

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TEXAS INSTRUMENTS
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description

The TI PCI1220 is a high-performance PCI-to-PC Card controller that supports two independent PC Card sockets compliant with the 1995 PC Card Standard. The PCI1220 provides a rich feature set that makes it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The 1995 PC Card Standard retains the 16-bit PC Card specification defined in PCMCIA Release 2.1, and defines the new 32-bit PC Card, CardBus, capable of full 32-bit data transfers at 33 MHz. The PCI1220 supports any combination of 16-bit and CardBus PC Cards in the two sockets, powered at 5 V or 3.3 V, as required.

The PCI1220 is compliant with the PCI Local Bus Specification 2.1, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during 16-bit PC Card direct memory access (DMA) transfers or CardBus PC Card bridging transactions. The PCI1220 is also compliant with the latest *PCI Bus Power Management Interface Specification*.

All card signals are internally buffered to allow hot insertion and removal without external buffering. The PCI1220 is register compatible with the Intel 82365SL-DF ExCA controller. The PCI1220 internal data path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and a pipeline architecture provide an unsurpassed performance level with sustained bursting. The PCI1220 can also be programmed to accept fast posted writes to improve system-bus utilization.

Multiple system-interrupt signaling options are provided, including: parallel PCI, parallel ISA, serialized ISA, and serialized PCI. Furthermore, general-purpose inputs and outputs are provided for the board designer to implement sideband functions. Many other features are designed into the PCI1220, such as socket activity light-emitting diode (LED) outputs, and are discussed in detail throughout the design specification.

An advanced complementary metal-oxide semiconductor (CMOS) process is used to achieve low system-power consumption while operating at PCI clock rates up to 33 MHz. Several low-power modes enable the host power management system to further reduce power consumption.

Unused PCI1220 inputs must be pulled up using a 43 kΩ resistor.

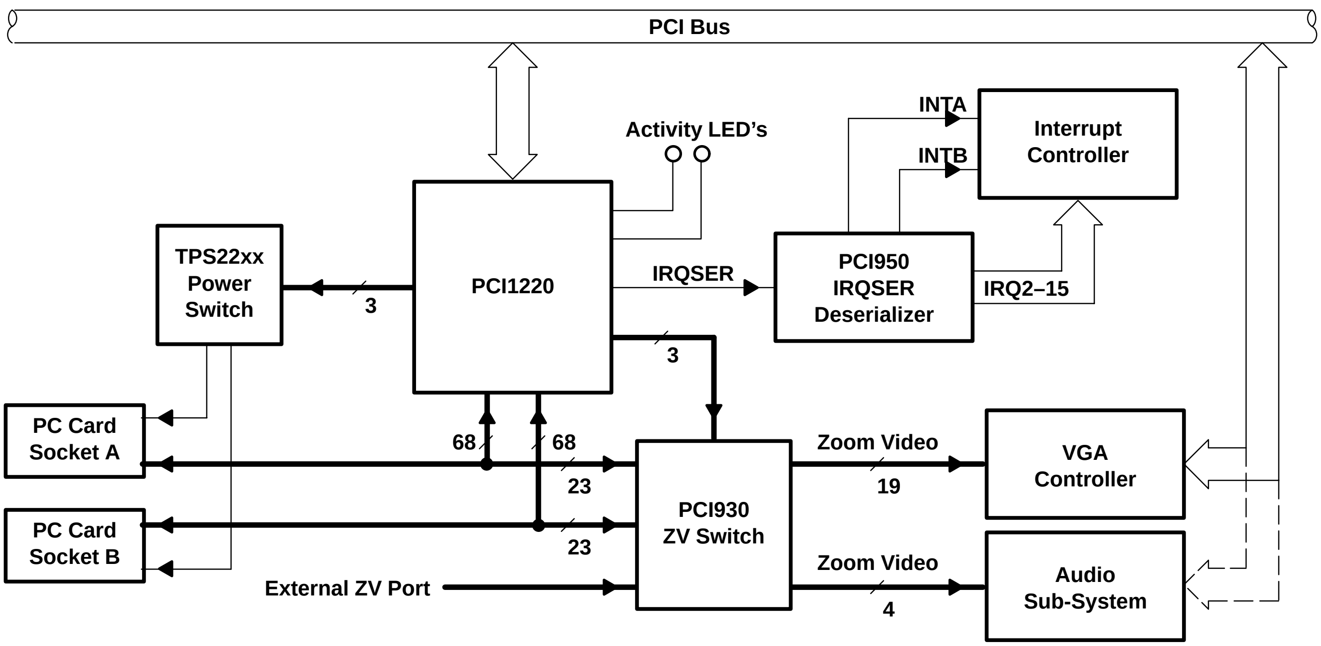
system block diagram

A simplified system block diagram using the PCI1220 is provided below. The PCI950 IRQ deseralizer and the PCI930 zoomed video (ZV) switch are optional functions that can be used when the system requires that capability.

The PCI interface includes all address/data and control signals for PCI protocol. The 68-pin PC Card interface includes all address/data and control signals for CardBus and 16-bit (R2) protocols. When zoomed video (ZV) is enabled (in 16-bit PC Card mode) 23 of the 68 signals are redefined to support the ZV protocol.

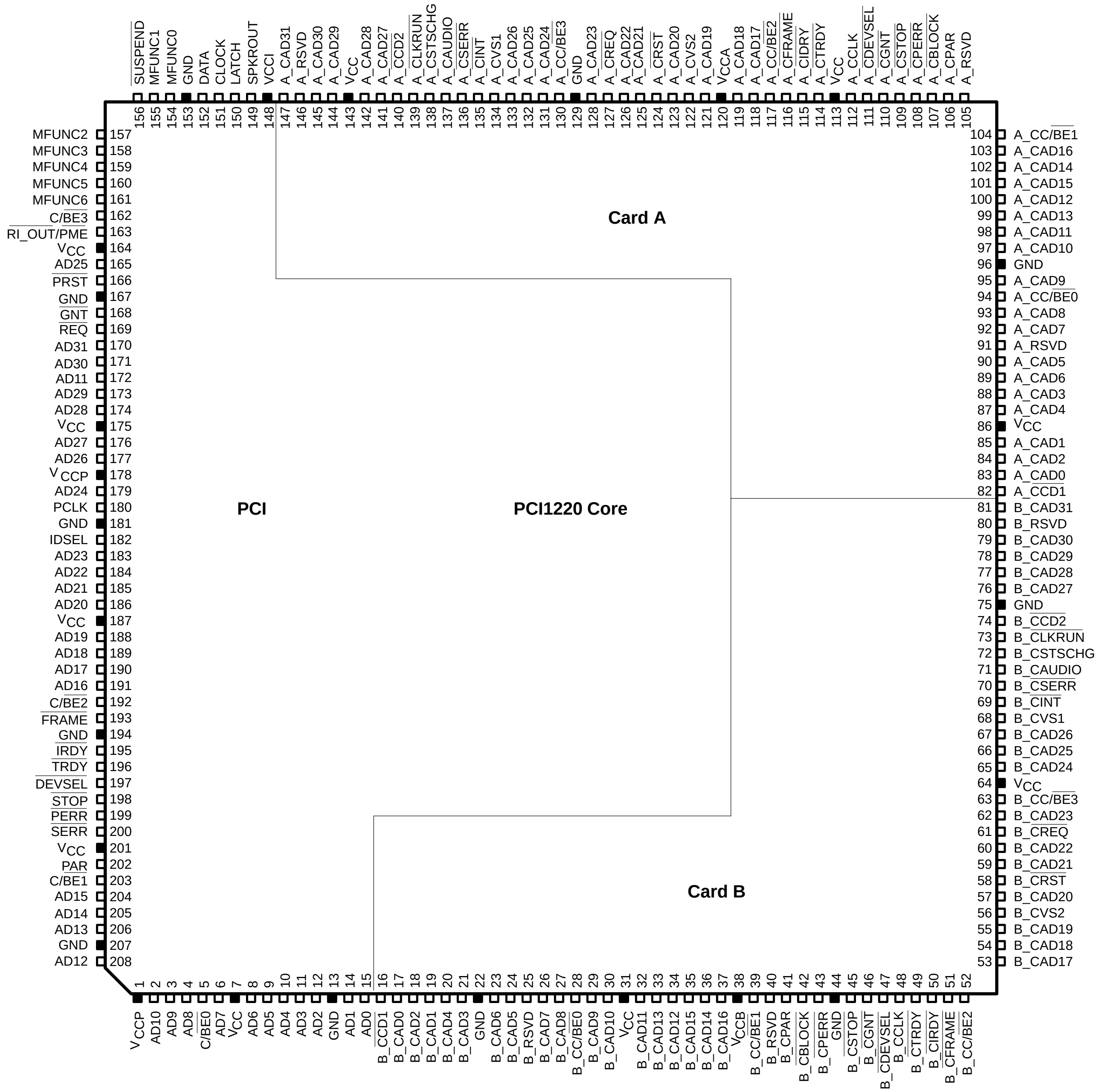
The interrupt interface includes terminals for parallel PCI, parallel ISA, and serialized PCI and ISA signaling. Other miscellaneous system interface terminals are available on the PCI1220 that include:

- Programmable multifunction terminals
- SUSPEND, RI_OUT/PME (power management control signal)
- SPKROUT.



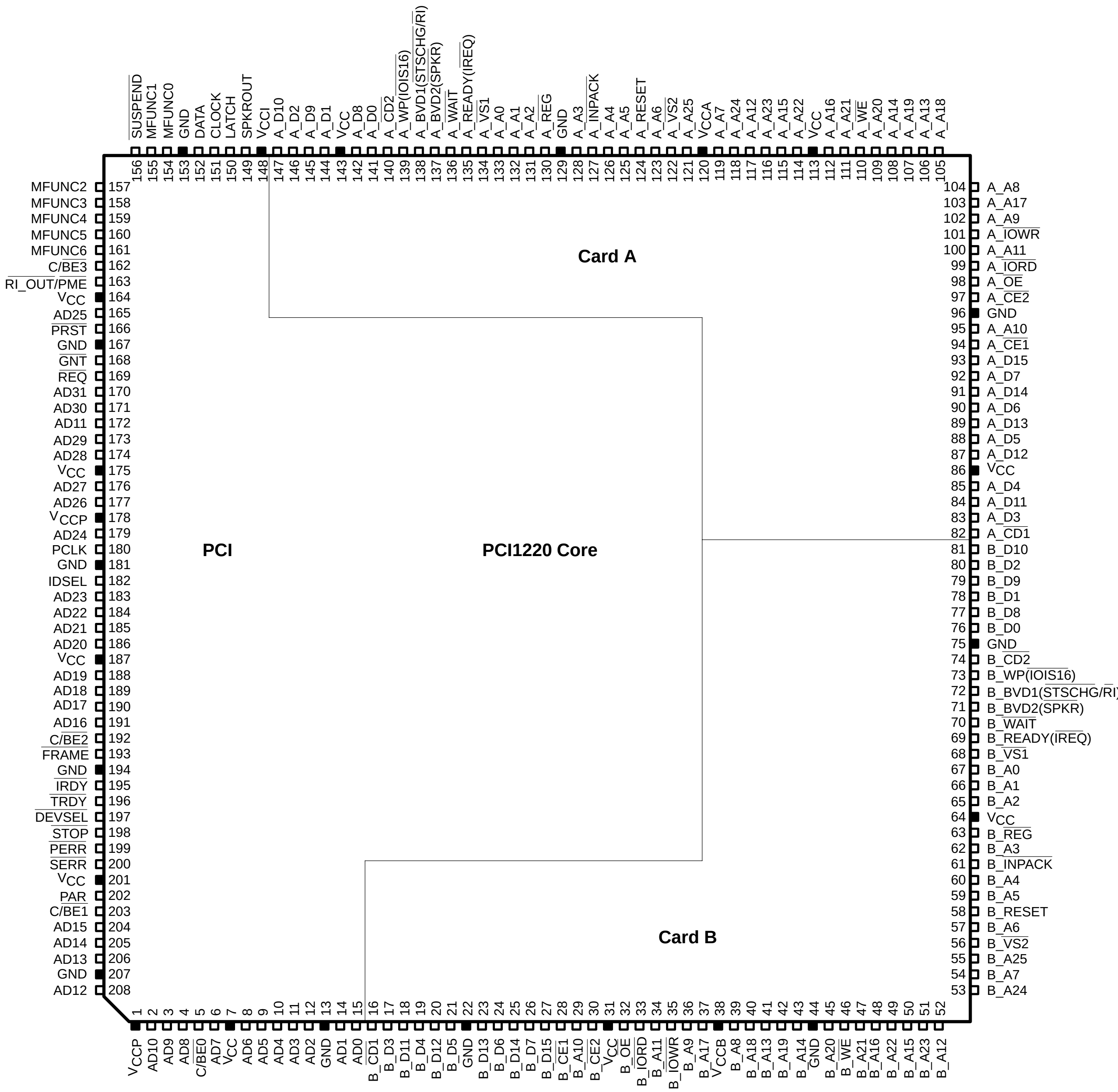
NOTE: The PC Card interface is 68 pins for CardBus and 16-bit PC Cards. In zoomed-video mode 23 pins are used for routing the zoomed video signals too the VGA controller.

terminal assignments



PCI-to-CardBus Pin Diagram

terminal assignments (continued)



PCI-to-PC Card (16-Bit) Diagram

Terminal Functions

The terminals are grouped in tables by functionality, such as PCI system function, power-supply function, etc. The terminal numbers are also listed for convenient reference.

power supply

TERMINAL NAME	TERMINAL NO.	FUNCTION
GND	13, 22, 44, 75, 96, 129, 153, 167, 181, 194, 207	Device ground terminals
V_{CC}	7, 31, 64, 86, 113, 143, 164, 175, 187, 201	Power supply terminal for core logic (3.3 V)
V_{CCA}	120	Rail power input for PC Card A interface. Indicates Card A signaling environment, 5 V or 3.3 V.
V_{CCB}	38	Rail power input for PC Card B interface. Indicates Card B signaling environment, 5 V or 3.3 V.
V_{CCI}	148	Rail power input for interrupt subsystem interface and miscellaneous I/O. (5 V or 3.3 V)
V_{CCP}	1, 178	Rail power input for PCI signaling (5 V or 3.3 V)

PC Card power switch

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
CLOCK	151	I/O	3–Line Power Switch Clock. Information on the DATA line is sampled at the rising edge of CLOCK. CLOCK defaults to an input, but can be changed to a PCI1220 output by using the P2CCLK bit in the System Control Register. The TPS2206 defines the maximum frequency of this signal to be 2MHz. If a system design defines this terminal an output, then this terminal requires an external pullup resister. The frequency of the PCI1220 output CLOCK is derived from dividing the PCI CLK by 36.
DATA	152	O	3–Line Power Switch Data. DATA is used to serially communicate socket power control information to the power switch.
LATCH	150	O	3–Line Power Switch Latch. LATCH is asserted by the PCI1220 to indicate to the PC Card power switch that the data on the DATA line is valid. When a pulldown resitor is implemented on this terminal, the MFUNC4 and MFUNC1 terminals provide the serial EEPROM SCL and SDA interface.

PCI system

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
PCLK	180	I	PCI bus clock. PCLK provides timing for all transactions on the PCI bus. All PCI signals are sampled at the rising edge of PCLK.
$\overline{\text{PRST}}$	166	I	PCI reset. When the PCI bus reset is asserted, $\overline{\text{PRST}}$ causes the PCI1220 to place all output buffers in a high-impedance state and reset all internal registers. When $\overline{\text{PRST}}$ is asserted, the device is completely nonfunctional. After $\overline{\text{PRST}}$ is deasserted, the PCI1220 is in its default state. When the $\overline{\text{SUSPEND}}$ and $\overline{\text{PRST}}$ are asserted, the device is protected from the $\overline{\text{PRST}}$ clearing the internal registers. All outputs are placed in a high-impedance state, but the contents of the registers are preserved.

Terminal Functions (Continued)

PCI address and data

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
AD31	170	I/O	PCI address/data bus. These signals make up the multiplexed PCI address and data bus on the primary interface. During the address phase of a primary bus PCI cycle, AD31–AD0 contain a 32-bit address or other destination information. During the data phase, AD31–AD0 contain data.
AD30	171		
AD29	173		
AD28	174		
AD27	176		
AD26	177		
AD25	165		
AD24	179		
AD23	183		
AD22	184		
AD21	185		
AD20	186		
AD19	188		
AD18	189		
AD17	190		
AD16	191		
AD15	204		
AD14	205		
AD13	206		
AD12	208		
AD11	172		
AD10	2		
AD9	3		
AD8	4		
AD7	6		
AD6	8		
AD5	9		
AD4	10		
AD3	11		
AD2	12		
AD1	14		
AD0	15		
C/BE3 C/BE2 C/BE1 C/BE0	162 192 203 5	I/O	PCI bus commands and byte enables. These signals are multiplexed on the same PCI terminals. During the address phase of a primary bus PCI cycle, C/BE3–C/BE0 define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. C/BE0 applies to byte 0 (AD7–AD0), C/BE1 applies to byte 1 (AD15–AD8), C/BE2 applies to byte 2 (AD23–AD16), and C/BE3 applies to byte 3 (AD31–AD24).
PAR	202	I/O	PCI bus parity. In all PCI bus read and write cycles, the PCI1220 calculates even parity across the AD31–AD0 and C/BE3–C/BE0 buses. As an initiator during PCI cycles, the PCI1220 outputs this parity indicator with a one-PCLK delay. As a target during PCI cycles, the calculated parity is compared to the initiator's parity indicator. A compare error results in the assertion of a parity error (PERR).

Terminal Functions (Continued)

PCI interface control

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
$\overline{\text{DEVSEL}}$	197	I/O	PCI device select. The PCI1220 asserts $\overline{\text{DEVSEL}}$ to claim a PCI cycle as the target device. As a PCI initiator on the bus, the PCI1220 monitors $\overline{\text{DEVSEL}}$ until a target responds. If no target responds before timeout occurs, the PCI1220 terminates the cycle with an initiator abort.
$\overline{\text{FRAME}}$	193	I/O	PCI cycle frame. $\overline{\text{FRAME}}$ is driven by the initiator of a bus cycle. $\overline{\text{FRAME}}$ is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When $\overline{\text{FRAME}}$ is deasserted, the PCI bus transaction is in the final data phase.
$\overline{\text{GNT}}$	168	I	PCI bus grant. $\overline{\text{GNT}}$ is driven by the PCI bus arbiter to grant the PCI1220 access to the PCI bus after the current data transaction has completed. $\overline{\text{GNT}}$ may or may not follow a PCI bus request, depending on the PCI bus parking algorithm.
IDSEL	182	I	Initialization device select. IDSEL selects the PCI1220 during configuration space accesses. IDSEL can be connected to one of the upper 24 PCI address lines on the PCI bus.
$\overline{\text{IRDY}}$	195	I/O	PCI initiator ready. $\overline{\text{IRDY}}$ indicates the PCI bus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of PCLK where both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted. Until $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are both sampled asserted, wait states are inserted.
$\overline{\text{PERR}}$	199	I/O	PCI parity error indicator. $\overline{\text{PERR}}$ is driven by a PCI device to indicate that calculated parity does not match PAR when $\overline{\text{PERR}}$ is enabled through bit 6 of the command register.
$\overline{\text{REQ}}$	169	O	PCI bus request. $\overline{\text{REQ}}$ is asserted by the PCI1220 to request access to the PCI bus as an initiator.
$\overline{\text{SERR}}$	200	O	PCI system error. $\overline{\text{SERR}}$ is an output that is pulsed from the PCI1220 when enabled through the command register indicating a system error has occurred. The PCI1220 need not be the target of the PCI cycle to assert this signal. When $\overline{\text{SERR}}$ is enabled in the control register, this signal also pulses, indicating that an address parity error has occurred on a CardBus interface.
$\overline{\text{STOP}}$	198	I/O	PCI cycle stop signal. $\overline{\text{STOP}}$ is driven by a PCI target to request the initiator to stop the current PCI bus transaction. $\overline{\text{STOP}}$ is used for target disconnects and is commonly asserted by target devices that do not support burst data transfers.
$\overline{\text{TRDY}}$	196	I/O	PCI target ready. $\overline{\text{TRDY}}$ indicates the primary bus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of PCLK when both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted. Until both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted, wait states are inserted.

Terminal Functions (Continued)

multifunction and miscellaneous pins

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
MFUNC6	161	I/O	Multifunction Terminal 6. MFUNC6 can be configured as a PCI CLKRUN or a parallel IRQ.
MFUNC5	160	I/O	Multifunction Terminal 5. MFUNC5 can be configured as PC/PCI DMA Grant, GPI4, GPO4, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE, or a parallel IRQ.
MFUNC4	159	I/O	Multifunction Terminal 4. MFUNC4 can be configured as PCI LOCK, GPI3, GPO3, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE, or a parallel IRQ. Serial Clock (SCL). When the serial bus mode is implemented by pulling the LATCH terminal low, the MFUNC4 terminal provides the SCL signaling. The two pin serial interface is used to load the subsystem identification and other register defaults from an EEPROM after a PCI reset.
MFUNC3	158	I/O	Multifunction Terminal 3. MFUNC3 can be configured as a parallel IRQ or the serialized interrupt signal IRQSER.
MFUNC2	157	I/O	Multifunction Terminal 2. MFUNC2 can be configured as PC/PCI DMA Request, GPI2, GPO2, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE, or a parallel IRQ.
MFUNC1	155	I/O	Multifunction Terminal 1. MFUNC1 can be configured as parallel PCI interrupt INTB, GPI1, GPO1, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE, or a parallel IRQ. Serial Data (SDA). When the serial bus mode is implemented by pulling the LATCH terminal low, the MFUNC1 terminal provides the SDA signaling. The two pin serial interface is used to load the subsystem identification and other register defaults from an EEPROM after a PCI reset.
MFUNC0	154	I/O	Multifunction Terminal 0. MFUNC0 can be configured as parallel PCI interrupt INTA, GPI0, GPO0, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE, or a parallel IRQ.
RI_OUT/PME	163	O	Ring Indicate Output and Power Management Event. When configured by the *Card Control Register* as PME, this terminal is used to indicate that a power management event is occuring. If the ring indicate function is enabled by the *Card Control Register*, the ring indicate signal is output on this terminal.
SUSPEND	156	I	Suspend. SUSPEND is used to protect the internal registers from clearing when the PRST signal is asserted.
SPKROUT	149	O	Speaker output. SPKROUT is the output to the host system that can carry SPKR or CAUDIO through the PCI1220 from the PC Card interface. SPKROUT is driven as the exclusive-OR combination of card SPKR//CAUDIO inputs.

Terminal Functions (Continued)

16-bit PC Card address and data (slots A and B)

TERMINAL NAME	NO. SLOT A†	NO. SLOT B‡	I/O TYPE	FUNCTION
A25	121	55	O	PC Card address. 16-bit PC Card address lines. A25 is the most-significant bit.
A24	118	53		
A23	116	51		
A22	114	49		
A21	111	47		
A20	109	45		
A19	107	42		
A18	105	40		
A17	103	37		
A16	112	48		
A15	115	50		
A14	108	43		
A13	106	41		
A12	117	52		
A11	100	34		
A10	95	29		
A9	102	36		
A8	104	39		
A7	119	54		
A6	123	57		
A5	125	59		
A4	126	60		
A3	128	62		
A2	131	65		
A1	132	66		
A0	133	67		
D15	93	27	I/O	PC Card data. 16-bit PC Card data lines. D15 is the most-significant bit.
D14	91	25		
D13	89	23		
D12	87	20		
D11	84	18		
D10	147	81		
D9	145	79		
D8	142	77		
D7	92	26		
D6	90	24		
D5	88	21		
D4	85	19		
D3	83	17		
D2	146	80		
D1	144	78		
D0	141	76		

† Terminal name for slot A is preceded with A_. For example, the full name for terminal 121 is A_A25.
‡ Terminal name for slot B is preceded with B_. For example, the full name for terminal 55 is B_A25.

Terminal Functions (Continued)

16-bit PC Card interface control (slots A and B)

TERMINAL NAME	NO. SLOT A†	NO. SLOT B‡	I/O TYPE	FUNCTION
BVD1 (STSCHG/RI)	138	72	I	Battery voltage detect 1. BVD1 is generated by 16-bit memory PC Cards that include batteries. BVD1 is used with BVD2 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are kept high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and should be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. Status change. STSCHG is used to alert the system to a change in the READY, write protect, or battery voltage dead condition of a 16-bit I/O PC Card. Ring indicate. RI is used by 16-bit modem cards to indicate a ring detection.
BVD2 (SPKR)	137	71	I	Battery voltage detect 2. BVD2 is generated by 16-bit memory PC Cards that include batteries. BVD2 is used with BVD1 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and should be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. Speaker. SPKR is an optional binary audio signal available only when the card and socket have been configured for the 16-bit I/O interface. The audio signals from cards A and B are combined by the PCI1220 and are output on SPKROUT. DMA request. BVD2 can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. The PC Card asserts BVD2 to indicate a request for a DMA operation.
CD1 CD2	82 140	16 74	I	PC Card detect 1 and PC Card detect 2. CD1 and CD2 are internally connected to ground on the PC Card. When a PC Card is inserted into a socket, CD1 and CD2 are pulled low. For signal status, see *interface status register.*
CE1 CE2	94 97	28 30	O	Card enable 1 and card enable 2. CE1 and CE2 enable even- and odd-numbered address bytes. CE1 enables even-numbered address bytes, and CE2 enables odd-numbered address bytes.
INPACK	127	61	I	Input acknowledge. INPACK is asserted by the PC Card when it can respond to an I/O read cycle at the current address. DMA request. INPACK can be used as the DMA request signal during DMA operations from a 16-bit PC Card that supports DMA. If used as a strobe, the PC Card asserts this signal to indicate a request for a DMA operation.
IORD	99	33	O	I/O read. IORD is asserted by the PCI1220 to enable 16-bit I/O PC Card data output during host I/O read cycles. DMA write. IORD is used as the DMA write strobe during DMA operations from a 16-bit PC Card that supports DMA. The PCI1220 asserts IORD during DMA transfers from the PC Card to host memory.
IOWR	101	35	O	I/O write. IOWR is driven low by the PCI1220 to strobe write data into 16-bit I/O PC Cards during host I/O write cycles. DMA read. IOWR is used as the DMA write strobe during DMA operations from a 16-bit PC Card that supports DMA. The PCI1220 asserts IOWR during transfers from host memory to the PC Card.
OE	98	32	O	Output enable. OE is driven low by the PCI1220 to enable 16-bit memory PC Card data output during host memory read cycles. DMA terminal count. OE is used as terminal count (TC) during DMA operations to a 16-bit PC Card that supports DMA. The PCI1220 asserts OE to indicate TC for a DMA write operation.

† Terminal name for slot A is preceded with A_. For example, the full name for terminal 127 is A_INPACK.
‡ Terminal name for slot B is preceded with B_. For example, the full name for terminal 61 is B_INPACK.

Terminal Functions (Continued)

16-bit PC Card interface control (slots A and B) (continued)

TERMINAL NAME	NUMBER SLOT A†	NUMBER SLOT B‡	I/O TYPE	FUNCTION
READY (IREQ)	135	69	I	Ready. The ready function is provided by READY when the 16-bit PC Card and the host socket are configured for the memory-only interface. READY is driven low by the 16-bit memory PC Cards to indicate that the memory card circuits are busy processing a previous write command. READY is driven high when the 16-bit memory PC Card is ready to accept a new data transfer command. Interrupt request. IREQ is asserted by a 16-bit I/O PC Card to indicate to the host that a device on the 16-bit I /O PC Card requires service by the host software. IREQ is high (deasserted) when no interrupt is requested.
REG	130	63	O	Attribute memory select. REG remains high for all common memory accesses. When REG is asserted, access is limited to attribute memory (OE or WE active) and to the I/O space (IORD or IOWR active). Attribute memory is a separately accessed section of card memory and is generally used to record card capacity and other configuration and attribute information. DMA acknowledge. REG is used as a DMA acknowledge (DACK) during DMA operations to a 16-bit PC Card that supports DMA. The PCI1220 asserts REG to indicate a DMA operation. REG is used in conjunction with the DMA read (IOWR) or DMA write (IORD) strobes to transfer data.
RESET	124	58	O	PC Card reset. RESET forces a hard reset to a 16-bit PC Card.
WAIT	136	70	I	Bus cycle wait. WAIT is driven by a 16-bit PC Card to delay the completion of (i.e., extend) the memory or I/O cycle in progress.
WE	110	46	O	Write enable. WE is used to strobe memory write data into 16-bit memory PC Cards. WE is also used for memory PC Cards that employ programmable memory technologies. DMA terminal count. WE is used as TC during DMA operations to a 16-bit PC Card that supports DMA. The PC1220 asserts WE to indicate TC for a DMA read operation.
WP (IOIS16)	139	73	I	Write protect. WP applies to 16-bit memory PC Cards. WP reflects the status of the write-protect switch on 16-bit memory PC Cards. For 16-bit I/O cards, WP is used for the 16-bit port (IOIS16) function. I/O is 16 bits. IOIS16 applies to 16-bit I/O PC Cards. IOIS16 is asserted by the 16-bit PC Card when the address on the bus corresponds to an address to which the 16-bit PC Card responds, and the I/O port that is addressed is capable of 16-bit accesses. DMA request. WP can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. If used, the PC Card asserts WP to indicate a request for a DMA operation.
VS1 VS2	134 122	68 56	I/O	Voltage sense 1 and voltage sense 2. VS1 and VS2, when used in conjunction with each other, determine the operating voltage of the 16-bit PC Card.

† Terminal name for slot A is preceded with A_. For example, the full name for terminal 110 is A_WE.
‡ Terminal name for slot B is preceded with B_. For example, the full name for terminal 46 is B_WE.

Terminal Functions (Continued)

CardBus PC Card interface system (slots A and B)

TERMINAL			I/O TYPE	FUNCTION
NAME	NO. SLOT A†	NO. SLOT B‡		
CCLK	112	48	O	CardBus PC Card clock. CCLK provides synchronous timing for all transactions on the CardBus interface. All signals except $\overline{\text{CRST}}$, $\overline{\text{CCLKRUN}}$, $\overline{\text{CINT}}$, CSTSCHG, CAUDIO, $\overline{\text{CCD2:1}}$, and CVS2–CVS1 are sampled on the rising edge of CCLK, and all timing parameters are defined with the rising edge of this signal. CCLK operates at the PCI bus clock frequency, but it can be stopped in the low state or slowed down for power savings.
$\overline{\text{CCLKRUN}}$	139	73	O	CardBus PC Card clock run. $\overline{\text{CCLKRUN}}$ is used by a CardBus PC Card to request an increase in the CCLK frequency, and by the PCI1220 to indicate that the CCLK frequency is going to be decreased.
$\overline{\text{CRST}}$	124	58	I/O	CardBus PC Card reset. $\overline{\text{CRST}}$ is used to bring CardBus PC Card-specific registers, sequencers, and signals to a known state. When $\overline{\text{CRST}}$ is asserted, all CardBus PC Card signals must be 3-stated, and the PCI1220 drives these signals to a valid logic level. Assertion can be asynchronous to CCLK, but deassertion must be synchronous to CCLK.

† Terminal name for slot A is preceded with A_. For example, the full name for terminal 112 is A_CCLK.
‡ Terminal name for slot B is preceded with B_. For example, the full name for terminal 48 is B_CCLK.

Terminal Functions (Continued)

CardBus PC Card address and data (slots A and B)

TERMINAL NAME	NO. SLOT A†	NO. SLOT B‡	I/O TYPE	FUNCTION
CAD31	147	81	I/O	PC Card address and data. These signals make up the multiplexed CardBus address and data bus on the CardBus interface. During the address phase of a CardBus cycle, CAD31–CAD0 contain a 32-bit address. During the data phase of a CardBus cycle, CAD31–CAD0 contain data. CAD31 is the most-significant bit.
CAD30	145	79		
CAD29	144	78		
CAD28	142	77		
CAD27	141	76		
CAD26	133	67		
CAD25	132	66		
CAD24	131	65		
CAD23	128	62		
CAD22	126	60		
CAD21	125	59		
CAD20	123	57		
CAD19	121	55		
CAD18	119	54		
CAD17	118	53		
CAD16	103	37		
CAD15	101	35		
CAD14	102	36		
CAD13	99	33		
CAD12	100	34		
CAD11	98	32		
CAD10	97	30		
CAD9	95	29		
CAD8	93	27		
CAD7	92	26		
CAD6	89	23		
CAD5	90	24		
CAD4	87	20		
CAD3	88	21		
CAD2	84	18		
CAD1	85	19		
CAD0	83	17		
CC/$\overline{BE3}$	130	63	I/O	CardBus bus commands and byte enables. CC/$\overline{BE3}$–CC/$\overline{BE0}$ are multiplexed on the same CardBus terminals. During the address phase of a CardBus cycle, CC/$\overline{BE3}$–CC/$\overline{BE0}$ defines the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. CC/$\overline{BE0}$ applies to byte 0 (CAD7–CAD0), CC/$\overline{BE1}$ applies to byte 1 (CAD15–CAD8), CC/$\overline{BE2}$ applies to byte 2 (CAD23–CAD8), and CC/$\overline{BE3}$ applies to byte 3 (CAD31–CAD24).
CC/$\overline{BE2}$	117	52		
CC/$\overline{BE1}$	104	39		
CC/$\overline{BE0}$	94	28		
CPAR	106	41	I/O	CardBus parity. In all CardBus read and write cycles, the PCI1220 calculates even parity across the CAD and CC/$\overline{BE}$ buses. As an initiator during CardBus cycles, the PCI1220 outputs CPAR with a one-CCLK delay. As a target during CardBus cycles, the calculated parity is compared to the initiator's parity indicator; a compare error results in a parity error assertion.

† Terminal name for slot A is preceded with A_. For example, the full name for terminal 106 is A_CPAR.
‡ Terminal name for slot B is preceded with B_. For example, the full name for terminal 41 is B_CPAR.

Terminal Functions (Continued)

CardBus PC Card interface control (slots A and B)

TERMINAL NAME	NO. SLOT A†	NO. SLOT B‡	I/O TYPE	FUNCTION
CAUDIO	137	71	I	CardBus audio. CAUDIO is a digital input signal from a PC Card to the system speaker. The PCI1220 supports the binary audio mode and outputs a binary signal from the card to SPKROUT.
CBLOCK	107	42	I/O	CardBus lock. CBLOCK is used to gain exclusive access to a target.
CCD1 CCD2	82 140	16 74	I	CardBus detect 1 and CardBus detect 2. CCD1 and CCD2 are used in conjunction with CVS1 and CVS2 to identify card insertion and interrogate cards to determine the operating voltage and card type.
CDEVSEL	111	47	I/O	CardBus device select. The PCI1220 asserts CDEVSEL to claim a CardBus cycle as the target device. As a CardBus initiator on the bus, the PCI1220 monitors CDEVSEL until a target responds. If no target responds before timeout occurs, the PCI1220 terminates the cycle with an initiator abort.
CFRAME	116	51	I/O	CardBus cycle frame. CFRAME is driven by the initiator of a CardBus bus cycle. CFRAME is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When CFRAME is deasserted, the CardBus bus transaction is in the final data phase.
CGNT	110	46	I	CardBus bus grant. CGNT is driven by the PCI1220 to grant a CardBus PC Card access to the CardBus bus after the current data transaction has been completed.
CINT	135	69	I	CardBus interrupt. CINT is asserted low by a CardBus PC Card to request interrupt servicing from the host.
CIRDY	115	50	I/O	CardBus initiator ready. CIRDY indicates the CardBus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of CCLK when both CIRDY and CTRDY are asserted. Until CIRDY and CTRDY are both sampled asserted, wait states are inserted.
CPERR	108	43	I/O	CardBus parity error. CPERR is used to report parity errors during CardBus transactions, except during special cycles. It is driven low by a target two clocks following that data when a parity error is detected.
CREQ	127	61	I	CardBus request. CREQ indicates to the arbiter that the CardBus PC Card desires use of the CardBus bus as an initiator.
CSERR	136	70	I	CardBus system error. CSERR reports address parity errors and other system errors that could lead to catastrophic results. CSERR is driven by the card synchronous to CCLK, but deasserted by a weak pullup, and may take several CCLK periods. The PCI1220 can report CSERR to the system by assertion of SERR on the PCI interface.
CSTOP	109	45	I/O	CardBus stop. CSTOP is driven by a CardBus target to request the initiator to stop the current CardBus transaction. CSTOP is used for target disconnects, and is commonly asserted by target devices that do not support burst data transfers.
CSTSCHG	138	72	I	CardBus status change. CSTSCHG is used to alert the system to a change in the card's status, and is used as a wake-up mechanism.
CTRDY	114	49	I/O	CardBus target ready. CTRDY indicates the CardBus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of CCLK, when both CIRDY and CTRDY are asserted; until this time, wait states are inserted.
CVS1 CVS2	134 122	68 56	I/O	CardBus voltage sense 1 and CardBus voltage sense 2. CVS1 and CVS2 are used in conjunction with CCD1 and CCD2 to identify card insertion and interrogate cards to determine the operating voltage and card type.

† Terminal name for slot A is preceded with A_. For example, the full name for terminal 137 is A_CAUDIO.
‡ Terminal name for slot B is preceded with B_. For example, the full name for terminal 71 is B_CAUDIO.

absolute maximum ratings over operating temperature ranges (unless otherwise noted)†

Supply voltage range, V_{CC}		–0.5 V to 4.6 V
Supply voltage range, V_{CCP}, V_{CCA}, V_{CCB}, V_{CCI}		–0.5 V to 6 V
Input voltage range, V_I:	PCI	–0.5 V to V_{CCP} + 0.5 V
	Card A	–0.5 to V_{CCA} + 0.5 V
	Card B	–0.5 to V_{CCB} + 0.5 V
	MISC	–0.5 to V_{CCI} + 0.5 V
	Fail safe	–0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O:	PCI	–0.5 V to V_{CCP} + 0.5 V
	Card A	–0.5 to V_{CCA} + 0.5 V
	Card B	–0.5 to V_{CCB} + 0.5 V
	MISC	–0.5 to V_{CCI} + 0.5 V
	Fail safe	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)		±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 2)		±20 mA
Storage temperature range, T_{stg}		–65°C to 150°C
Virtual junction temperature, T_J		150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Applies for external input and bidirectional buffers. $V_I > V_{CC}$ does not apply to fail-safe terminals. PCI terminals are measured with respect to V_{CCP} instead of V_{CC}. PC Card terminals are measured with respect to V_{CCA} or V_{CCB}. Miscellaneous signals are measured with respect to V_{CCI}. The limit specified applies for a dc condition.

2. Applies for external output and bidirectional buffers. $V_O > V_{CC}$ does not apply to fail-safe terminals. PCI terminals are measured with respect to V_{CCP} instead of V_{CC}. PC Card terminals are measured with respect to V_{CCA} or V_{CCB}. Miscellaneous signals are measured with respect to V_{CCI}. The limit specified applies for a dc condition.

recommended operating conditions (see Note 3)

			OPERATION	MIN	NOM	MAX	UNIT
V_{CC}	Core voltage	Commercial	3.3 V	3	3.3	3.6	V
V_{CCP}	PCI I/O voltage	Commercial	3.3 V	3	3.3	3.6	V
			5 V	4.75	5	5.25	
$V_{CC(A/B)}$	PC Card I/O voltage	Commercial	3.3 V	3	3.3	3.6	V
			5 V	4.75	5	5.25	
V_{CCI}	Miscellaneous I/O voltage	Commercial	3.3 V	3	3.3	3.6	V
			5 V	4.75	5	5.25	
V_{IH}†	High-level input voltage	PCI	3.3 V	0.5 V_{CCP}		V_{CCP}	V
			5 V	2		V_{CCP}	
		PC Card	3.3 V	0.475 $V_{CCA/B}$		$V_{CCA/B}$	
			5 V	2.4		$V_{CCA/B}$	
		MISC‡		2		V_{CCI}	
		Fail safe§		2		V_{CC}	
V_{IL}†	Low-level input voltage	PCI	3.3 V	0		0.3 V_{CCP}	V
			5 V	0		0.8	
		PC Card	3.3 V	0		0.325 $V_{CCA/B}$	
			5 V	0		0.8	
		MISC‡		0		0.8	
		Fail safe§		0		0.8	
V_I	Input voltage	PCI		0		V_{CCP}	V
		PC Card		0		$V_{CCA/B}$	
		MISC‡		0		V_{CCI}	
		Fail safe§		0		V_{CC}	
V_O¶	Output voltage	PCI		0		V_{CCP}	V
		PC Card		0		$V_{CCA/B}$	
		MISC‡		0		V_{CCI}	
		Fail safe§		0		V_{CC}	
t_t	Input transition time (t_r and t_f)	PCI and PC Card		1		4	ns
		ZV, miscellaneous, and fail safe		0		6	
T_A	Operating ambient temperature range			0	25	70	°C
T_J#	Virtual junction temperature			0	25	115	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

† Applies to external inputs and bidirectional buffers without hysteresis

‡ Miscellaneous pins are 149, 150, 151, 152, 154, 155, 156, 157, 158, 159, 161, 163 ($\overline{\text{SUSPEND}}$, SPKROUT, $\overline{\text{RI\_OUT}}$, multifunction terminals (MFUNC0–6), and power switch control pins).

§ Fail-safe pins are 16, 56, 68, 74, 82, 122, 134, and 140 (card detect and voltage sense pins).

¶ Applies to external output buffers

These junction temperatures reflect simulation conditions. The customer is responsible for verifying junction temperature.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		PINS	OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	PCI	3.3 V	I_{OH} = –0.5 mA	0.9 V_{CC}		V
			5 V	I_{OH} = –2 mA	2.4		
		PC Card	3.3 V	I_{OH} = –0.15 mA	0.9 V_{CC}		
			5 V	I_{OH} = –0.15 mA	2.4		
		MISC		I_{OH} = –4 mA	V_{CC}–0.6		
		ZV		I_{OH} = –4 mA	V_{CC}–0.6		
V_{OL}	Low-level output voltage	PCI	3.3 V	I_{OL} = 1.5 mA		0.1 V_{CC}	V
			5 V	I_{OL} = 6 mA		0.55	
		PC Card	3.3 V	I_{OL} = 0.7 mA		0.1 V_{CC}	
			5 V	I_{OL} = 0.7 mA		0.55	
		MISC		I_{OL} = 4 mA		0.5	
		$\overline{SERR}$		I_{OL} = 12 mA		0.5	
I_{OZL}	3-state output, high-impedance state current	Output pins	3.6 V	$V_I = V_{CC}$		–1	µA
			5.25 V	$V_I = V_{CC}$		–1	
I_{OZH}	3-state output, high-impedance state current	Output pins	3.6 V	$V_I = V_{CC}$†		10	µA
			5.25 V	$V_I = V_{CC}$†		25	
I_{IL}	Low-level input current	Input pins		V_I = GND		–1	µA
		I/O pins		V_I = GND		–10	
I_{IH}	High-level input current	Input pins	3.6 V	$V_I = V_{CC}$‡		10	µA
			5.25 V	$V_I = V_{CC}$‡		20	
		I/O pins	3.6 V	$V_I = V_{CC}$‡		10	
			5.25 V	$V_I = V_{CC}$‡		25	
		Fail-safe pins	3.6 V	$V_I = V_{CC}$		10	

† For PCI pins, $V_I = V_{CCP}$. For PC Card pins, $V_I = V_{CC(A/B)}$. For miscellaneous pins, $V_I = V_{CCI}$
‡ For I/O pins, input leakage (I_{IL} and I_{IH}) includes I_{OZ} leakage of the disabled output.

PCI clock/reset timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1 and Figure 2)

PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
t_c	Cycle time, PCLK	t_{cyc}		30		ns
t_{wH}	Pulse duration, PCLK high	t_{high}		11		ns
t_{wL}	Pulse duration, PCLK low	t_{low}		11		ns
$\Delta v/\Delta t$	Slew rate, PCLK	t_r, t_f		1	4	V/ns
t_w	Pulse duration, RSTIN	t_{rst}		1		ms
t_{su}	Setup time, PCLK active at end of $\overline{\text{RSTIN}}$	$t_{rst\text{-}clk}$		100		µs

PCI timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 1 thru Figure 4 and Note 4)

PARAMETER			ALTERNATE SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd}	Propagation delay time, See Note 5	PCLK-to-shared signal valid delay time	t_{val}	C_L = 50 pF		11	ns
		PCLK-to-shared signal invalid delay time	t_{inv}		2		
t_{en}	Enable time, high impedance-to-active delay time from PCLK		t_{on}		2		ns
t_{dis}	Disable time, active-to-high impedance delay time from PCLK		t_{off}			28	ns
t_{su}	Setup time before PCLK valid		t_{su}		7		ns
t_h	Hold time after PCLK high		t_h		0		ns

NOTES: 4. PCI shared signals are AD31–0, C/$\overline{\text{BE3–0}}$, $\overline{\text{FRAME}}$, $\overline{\text{TRDY}}$, $\overline{\text{IRDY}}$, $\overline{\text{STOP}}$, IDSEL, $\overline{\text{DEVSEL}}$, and PAR.
5. This data sheet uses the following conventions to describe time (t) intervals. The format is t_A, where *subscript A* indicates the type of dynamic parameter being represented. One of the following is used: t_{pd} = propagation delay time, t_d = delay time, t_{su} = setup time, and t_h = hold time.

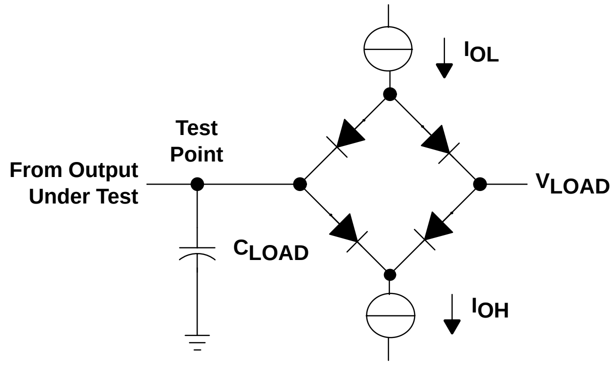
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT PARAMETERS

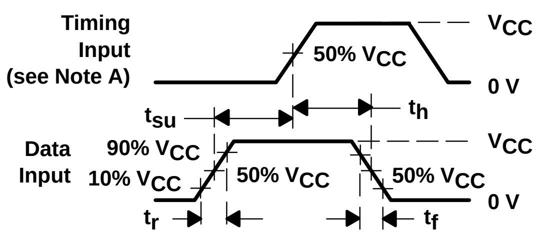
TIMING PARAMETER		C_{LOAD}† (pF)	I_{OL} (mA)	I_{OH} (mA)	V_{LOAD} (V)
t_{en}	t_{PZH}	50	8	–8	0
	t_{PZL}				3
t_{dis}	t_{PHZ}	50	8	–8	1.5
	t_{PLZ}				
t_{pd}		50	8	–8	‡

† C_{LOAD} includes the typical load-circuit distributed capacitance

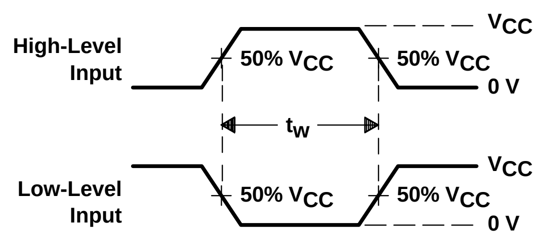
‡ $\frac{V_{LOAD} - V_{OL}}{I_{OL}} = 50\ \Omega$, where $V_{OL} = 0.6$ V, $I_{OL} = 8$ mA



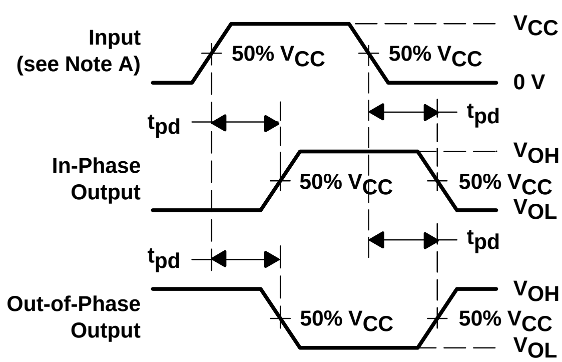
LOAD CIRCUIT



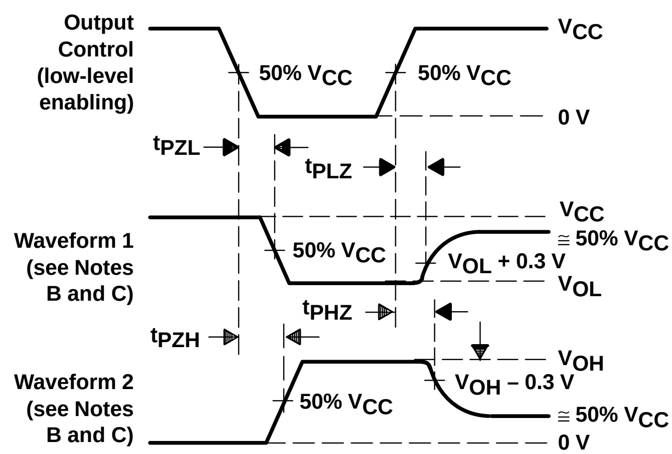
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
A. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by pulse generators having the following characteristics: PRR = 1 MHz, $Z_O = 50\ \Omega$, $t_r = 6$ ns.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. For t_{PLZ} and t_{PHZ}, V_{OL} and V_{OH} are measured values.

Figure 1. Load Circuit and Voltage Waveforms

PCI BUS PARAMETER MEASUREMENT INFORMATION

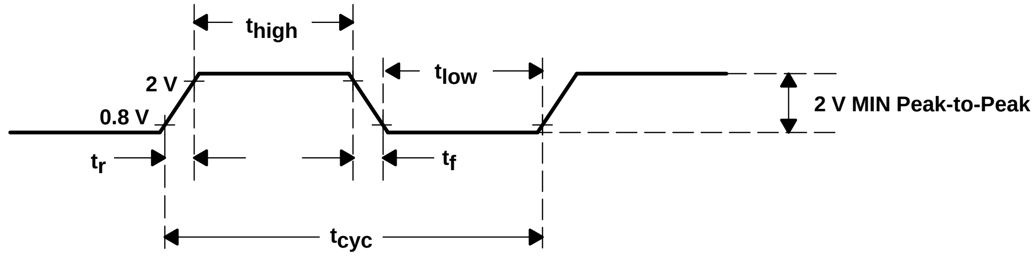


Figure 2. PCLK Timing Waveform

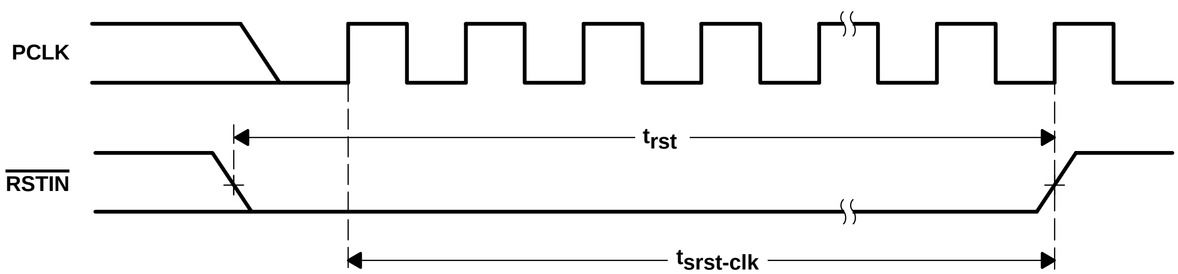


Figure 3. RSTIN Timing Waveforms

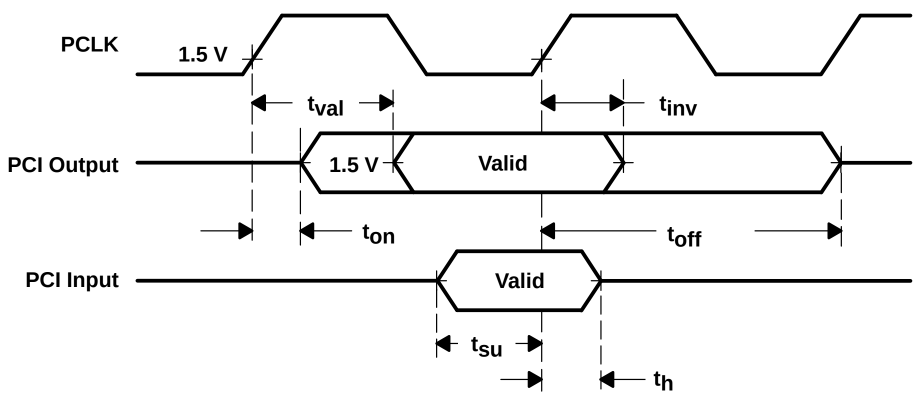


Figure 4. Shared Signals Timing Waveforms

PC Card cycle timing

The PC Card cycle timing is controlled by the wait-state bits in the Intel 82365SL-DF compatible memory and I/O window registers. The PC Card cycle generator uses the PCI clock to generate the correct card address setup and hold times and the PC Card command active (low) interval. This allows the cycle generator to output PC Card cycles that are as close to the Intel 82365SL-DF timing as possible while always slightly exceeding the Intel 82365SL-DF values. This ensures compatibility with existing software and maximizes throughput.

The PC Card address setup and hold times are a function of the wait-state bits. Table 1 shows address setup time in PCLK cycles and nanoseconds for I/O and memory cycles. Table 2 and Table 3 show command active time in PCLK cycles and nanoseconds for I/O and memory cycles. Table 4 shows address hold time in PCLK cycles and nanoseconds for I/O and memory cycles.

Table 1. PC Card Address Setup Time, $t_{su(A)}$, 8-Bit and 16-Bit PCI Cycles

WAIT-STATE BITS			TS1 – 0 = 01 (PCLK/ns)
I/O			3/90
Memory	WS1	0	2/60
Memory	WS1	1	4/120

Table 2. PC Card Command Active Time, $t_{c(A)}$, 8-Bit PCI Cycles

WAIT-STATE BITS			TS1 – 0 = 01 (PCLK/ns)
	WS	ZWS	
I/O	0	0	19/570
	1	X	23/690
	0	1	7/210
Memory	00	0	19/570
	01	X	23/690
	10	X	23/690
	11	X	23/690
	00	1	7/210

Table 3. PC Card Command Active Time, $t_{c(A)}$, 16-Bit PCI Cycles

WAIT-STATE BITS			TS1 – 0 = 01 (PCLK/ns)
	WS	ZWS	
I/O	0	0	7/210
	1	X	11/330
	0	1	N/A
Memory	00	0	9/270
	01	X	13/390
	10	X	17/510
	11	X	23/630
	00	1	5/150

Table 4. PC Card Address Hold Time, $t_{h(A)}$, 8-Bit and 16-Bit PCI Cycles

WAIT-STATE BITS			TS1 – 0 = 01 (PCLK/ns)
I/O			2/60
Memory	WS1	0	2/60
Memory	WS1	1	3/90

timing requirements over recommended ranges of supply voltage and operating free-air temperature, memory cycles (for 100-ns common memory) (see Note 5 and Figure 5)

		ALTERNATE SYMBOL	MIN	MAX	UNIT
t_{su}	Setup time, CE1 and CE2 before WE/OE low	T1	60		ns
t_{su}	Setup time, CA25–CA0 before WE/OE low	T2	$t_{su(A)}$+2PCLK		ns
t_{su}	Setup time, REG before WE/OE low	T3	90		ns
t_{pd}	Propagation delay time, WE/OE low to WAIT low	T4			ns
t_w	Pulse duration, WE/OE low	T5	200		ns
t_h	Hold time, WE/OE low after WAIT high	T6			ns
t_h	Hold time, CE1 and CE2 after WE/OE high	T7	120		ns
t_{su}	Setup time (read), CDATA15–CDATA0 valid before OE high	T8			ns
t_h	Hold time (read), CDATA15–CDATA0 valid after OE high	T9	0		ns
t_h	Hold time, CA25–CA0 and REG after WE/OE high	T10	$t_{h(A)}$+1PCLK		ns
t_{su}	Setup time (write), CDATA15–CDATA0 valid before WE low	T11	60		ns
t_h	Hold time (write), CDATA15–CDATA0 valid after WE low	T12	240		ns

NOTE 6: These times are dependent on the register settings associated with ISA wait states and data size. They are also dependent on cycle type (read/write, memory/I/O) and WAIT from PC Card. The times listed here represent absolute minimums (the times that would be observed if programmed for zero wait state, 16-bit cycles) with a 33-MHz PCI clock.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, I/O cycles (see Figure 6)

		ALTERNATE SYMBOL	MIN	MAX	UNIT
t_{su}	Setup time, REG before IORD/IOWR low	T13	60		ns
t_{su}	Setup time, CE1 and CE2 before IORD/IOWR low	T14	60		ns
t_{su}	Setup time, CA25–CA0 valid before IORD/IOWR low	T15	$t_{su(A)}$+2PCLK		ns
t_{pd}	Propagation delay time, IOIS16 low after CA25–CA0 valid	T16		35	ns
t_{pd}	Propagation delay time, IORD low to WAIT low	T17	35		ns
t_w	Pulse duration, IORD/IOWR low	T18	T_{cA}		ns
t_h	Hold time, IORD low after WAIT high	T19			ns
t_h	Hold time, REG low after IORD high	T20	0		ns
t_h	Hold time, CE1 and CE2 after IORD/IOWR high	T21	120		ns
t_h	Hold time, CA25–CA0 after IORD/IOWR high	T22	$t_{h(A)}$+1PCLK		ns
t_{su}	Setup time (read), CDATA15–CDATA0 valid before IORD high	T23	10		ns
t_h	Hold time (read), CDATA15–CDATA0 valid after IORD high	T24	0		ns
t_{su}	Setup time (write), CDATA15–CDATA0 valid before IOWR low	T25	90		ns
t_h	Hold time (write), CDATA15–CDATA0 valid after IOWR high	T26	90		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, miscellaneous (see Figure 7)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
t_{pd}	Propagation delay time	BVD2 low to SPKROUT low	T27		30	ns
		BVD2 high to SPKROUT high			30	
		$\overline{\text{IREQ}}$ to IRQ15–IRQ3	T28		30	
		$\overline{\text{STSCHG}}$ to IRQ15–IRQ3			30	

PC Card PARAMETER MEASUREMENT INFORMATION

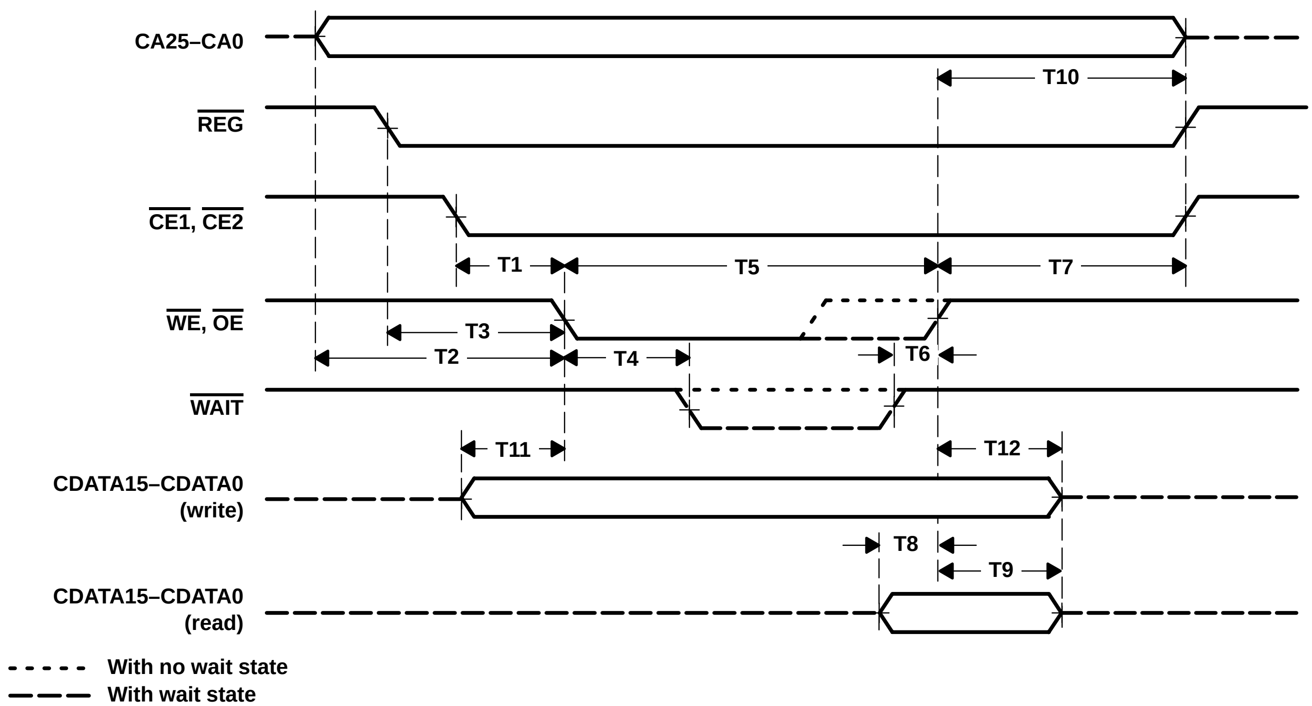


Figure 5. PC Card Memory Cycle

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PC Card PARAMETER MEASUREMENT INFORMATION

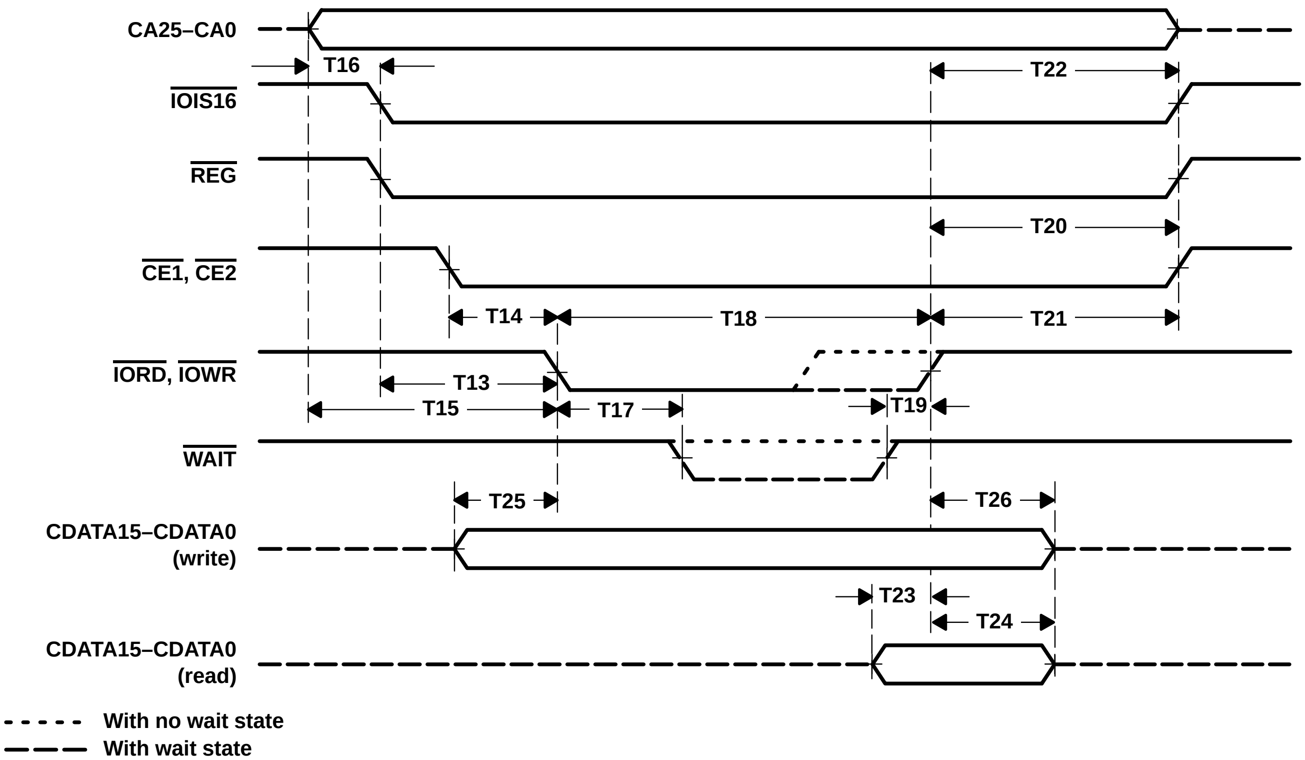


Figure 6. PC Card I/O Cycle

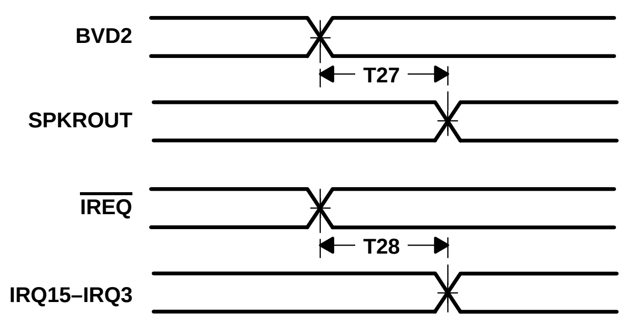
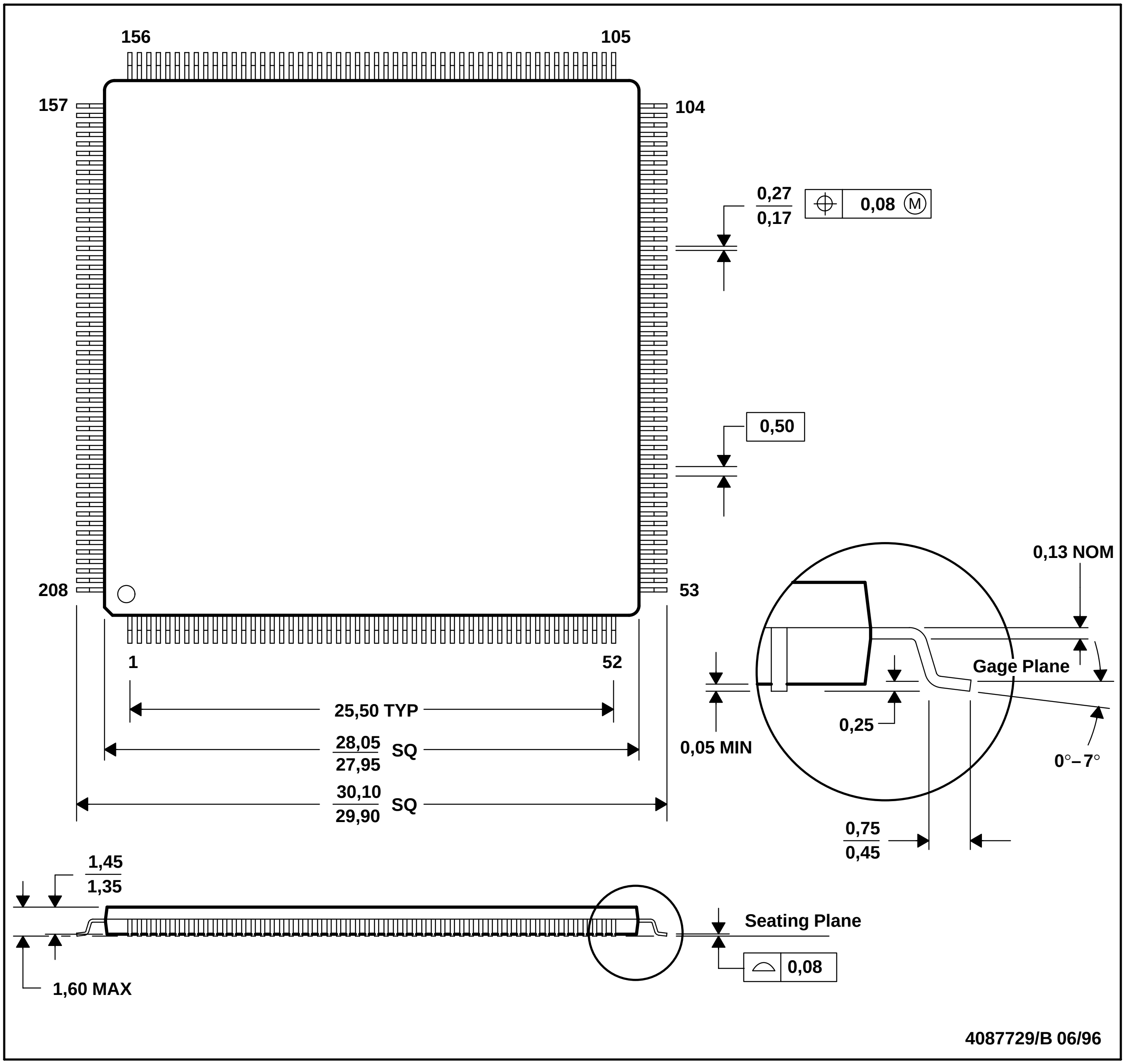


Figure 7. Miscellaneous PC Card Delay Times

MECHANICAL DATA

PDV (S-PQFP-G208) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136