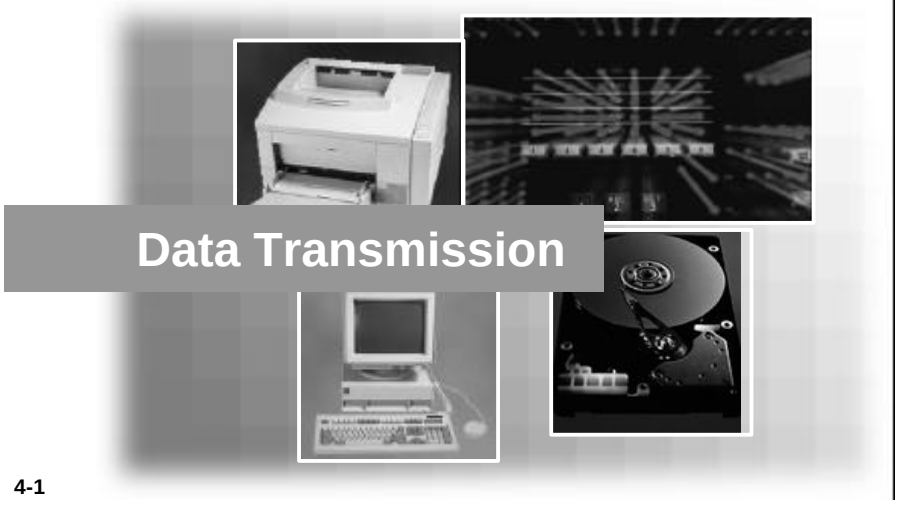

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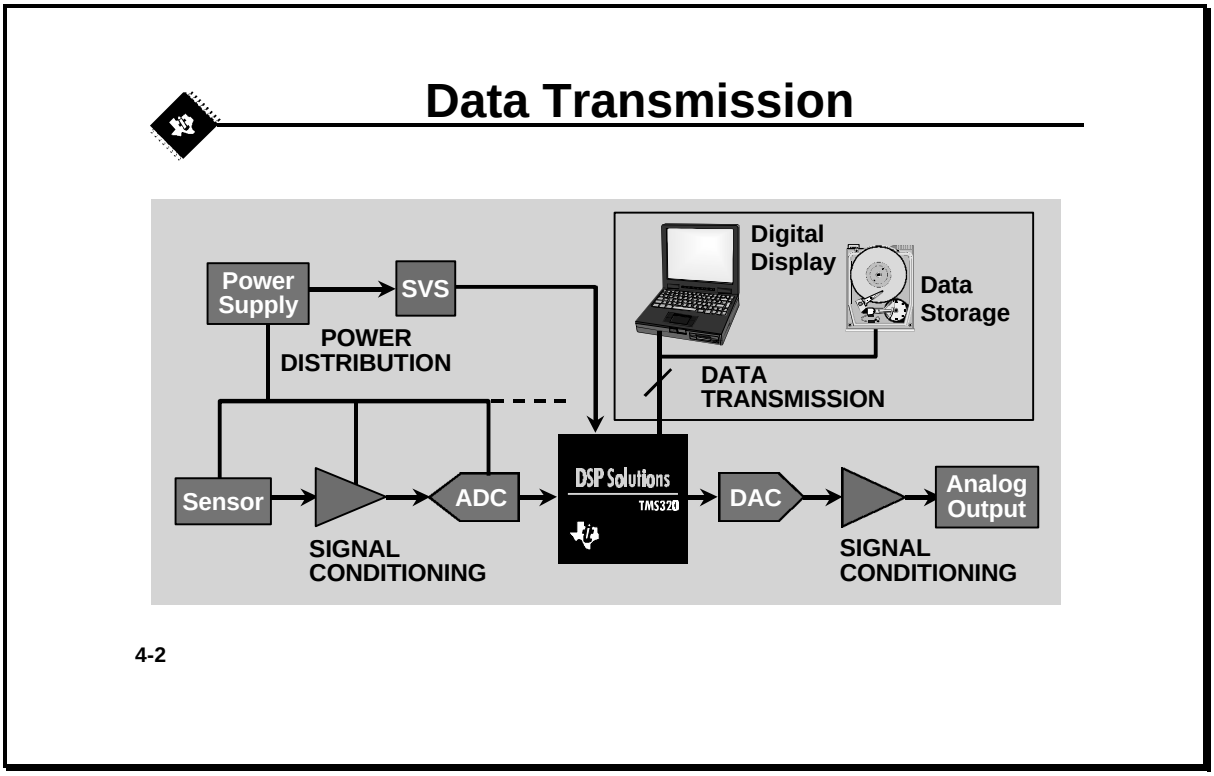
Table of Contents

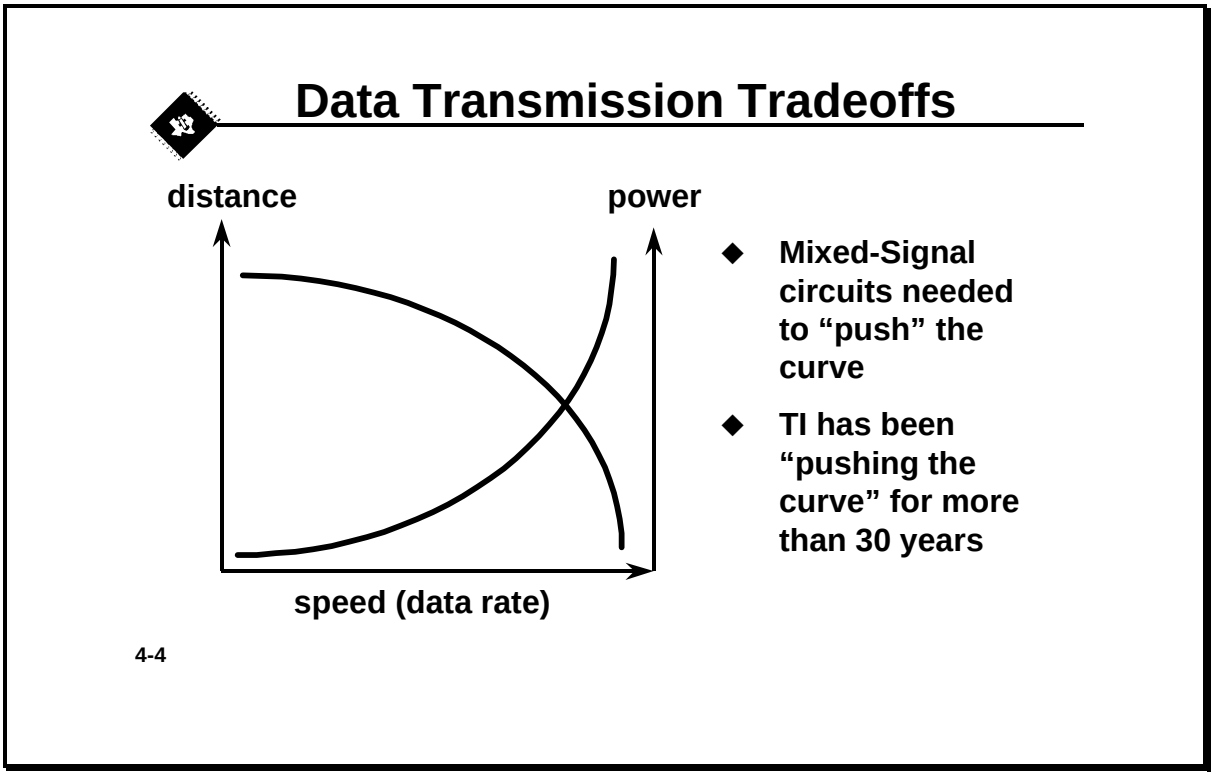


What is Data Transmission?

Data Transmission as part of Texas Instruments' Mixed-Signal Product portfolio is concerned with the standards involving transmitting data at relatively high speeds down long line lengths, the considerations for which are primarily of an analog more than a digital nature.

TI has been a leading supplier of data transmission products for many years and is continually providing innovation for new fields. Although the following presentation is limited to the more common interface standards, TI actively is involved in many new emerging standards and markets such as 1394 and PCI bus.

With considerable expertise in design, product definition, and a range of technologies, TI is the ideal choice for supplying your data transmission product requirements. In this section of the seminar we will review the different ANSI standards that exist and we will introduce the new ANSI/TIA/EIA-644 standard, otherwise known as LVDS.



Data transmission tradeoffs

The challenge to the designers of data transmission circuits is to balance the tradeoffs between speed, power, and distance. These tradeoffs lead to the need for specialized ICs and technologies. Traditionally, the robustness of bipolar technologies has been utilized; however, the additional need for low power consumption and high levels of integration no longer makes this attractive. Semiconductor (SC) manufacturers now have to develop their technologies to accommodate these requirements. TI has introduced its proprietary LinBiCMOS™ technology, which combines the robustness of bipolar together with the power consumption and integration afforded by CMOS. The results of these technologies are very specialized and reliable products that are able to withstand the harsh environment unique to data transmission products.

Why Follow Standards?

- Interchangeability of equipment and components
  - Lowers component cost through economies of scale and competition
- Reduced risk and cycle times
  - Design “by committee” of industry experts is generally very robust
  - Standards live for decades

4-5

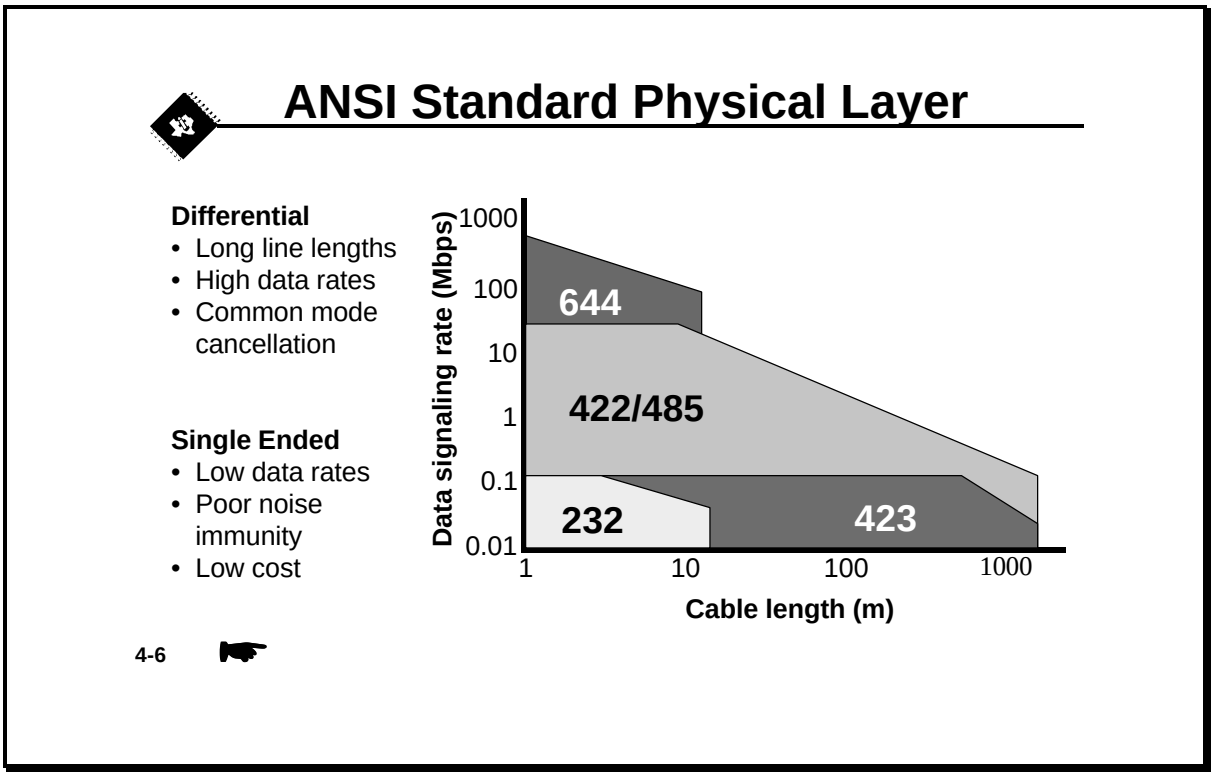
Why follow standards?

Data Transmission Standards evolved for two main reasons: from the need to transmit data reliably over long distances and to provide a standard interface to facilitate communication between equipment from different suppliers.

Semiconductor manufacturers know what specifications to comply with to make catalog devices fully compatible with the standard and enable devices adhering to the standard to communicate. Users then know how to configure the system so the equipment may communicate (cable lengths, signaling rates, etc.).

Since the devices are designed according to a standard, there is lower design risk and a shorter cycle time for the system. The devices are also catalog parts, meaning they are released devices available for purchase today. Catalog components enjoy economies of scale over proprietary devices since everyone in the industry can purchase the devices and through collectively larger volumes, cause lower costs.

ANSI Standards



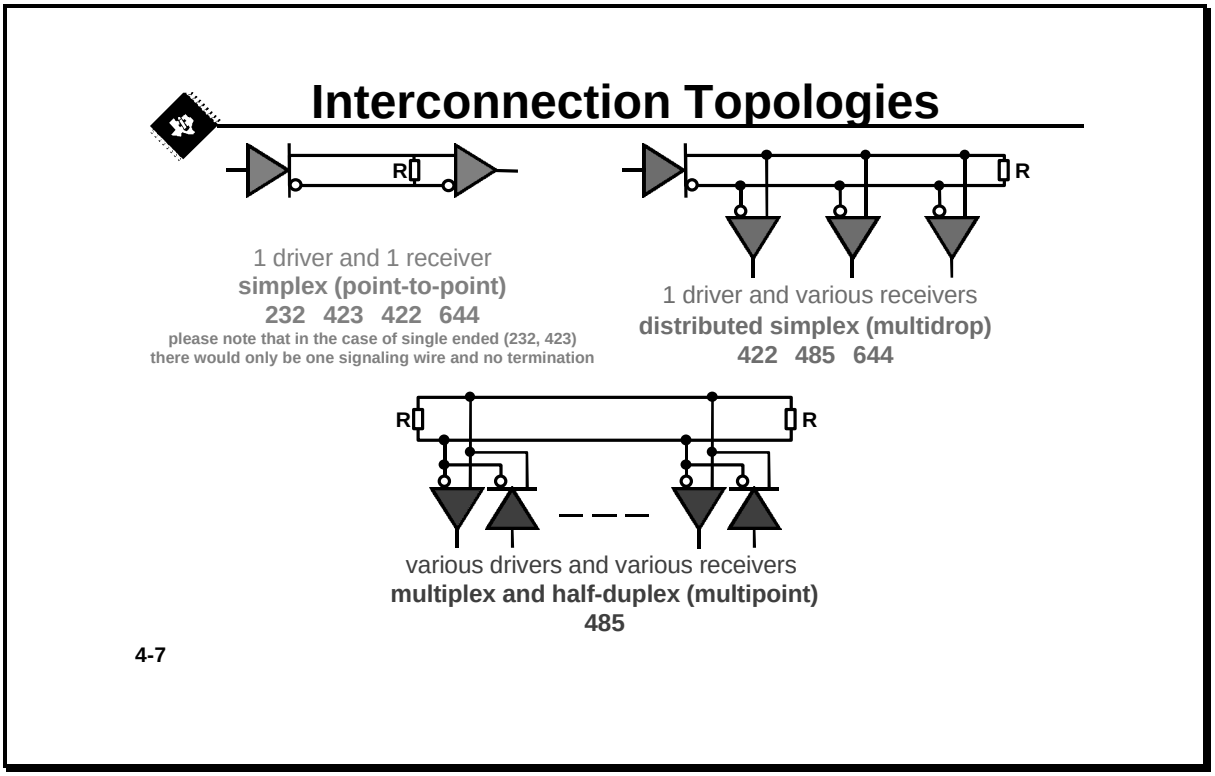
ANSI standard physical layer

The American National Standard Institution (ANSI) standards cover a wide range of signaling rates and distances. One of the first questions designers must ask themselves when choosing a data transmission standard is how far? and how fast? The above figure shows a general guideline of each transmission standard when comparing data signaling rates and line lengths.

Basically, these standards may be divided into two transmission categories: 1) single-ended (232,423) and 2) differential (422, 485, 644), each one having its advantages and disadvantages.

The advantages of single-ended transmission are simplicity and low cost of implementation. A single-ended system requires one line per signal making it a cost-effective solution for low signaling rates and short distances. The main disadvantage of the single-ended solution is its poor noise immunity. Because the ground wire forms part of the system, transient voltages or shifts in voltage potential may be induced, leading to signal degradation. Crosstalk is also a major concern, especially at high frequencies. These problems will normally limit the distance and speed of reliable operation for a single-ended link.

At high data rates, on long lines or under noisy conditions, differential data transmission has an advantage over single-ended because it is more immune to noise interference. A differential transmission involves using two signal-carrying wires between the driver and the receiver. Any noise induced on one of the lines will also be induced on the other. The receiver is only concerned with the difference between these two signals, and any noise coupled onto the two wires appears as common-mode noise and is rejected. This is true in cases of crosstalk from neighboring signal lines. It is also true for noise from other noise sources as long as the common-mode voltage does not go beyond the common-mode range of the receiver. The common-mode rejection of the receiver eliminates also to a certain degree noise caused by a ground voltage difference between the driver and the receiver. All these advantages come with some drawbacks. Due to the more complex circuit technique required to achieve the high performance these circuits may have a higher cost. Furthermore the high data rate requires well-defined line impedance and a correct line termination to avoid line reflections. Also twisted pair cable instead of inexpensive multi-core cables need to be used.



ANSI standard parameters

ANSI Standard Parameters

Parameter	TIA/EIA 232-F	TIA/EIA 423-A	TIA/EIA 422-B	TIA/EIA 485-A	TIA/EIA 644 (LVDS)
Mode of Operation	Single-Ended	Single-Ended	Differential	Differential	Differential
Transmission Modes	Simplex	Simplex	Simplex, Distributed simplex (multidrop)	Half-Duplex, Multiplex (multipoint)	Simplex, Distributed Simplex (multidrop)
Maximum Cable Length (m)	20	1200	1200	1200	30
Maximum Data Rate (bps)	20 k	120 k	10 M	50 M	655 M
Maximum Ground Offset Voltage (V)	± 3	± 3	± 7	-7 to 12	± 1
Minimum Driver Output Levels (V)	± 5	± 3.6	± 2	± 1.5	± 0.247
Driver Load (Ω)	3 k to 7 k	450 (Min)	100 (Min)	60 (Min)	100
Driver Slew Rate	30 V/μs (Max.)	NA	NA	NA	~ 2.3 V/ηs
Receiver Sensitivity (V)	± 3	± 200 m	± 200 m	± 200 m	± 100 m

4-8

TIA/EIA-232-F

TIA/EIA-232-F (232) is defined in the ANSI specification as "The Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange". The standard employs a single ended serial-transmission scheme and outlines the set of rules for exchanging data between computer equipment, ie., a computer terminal, which is classified as a type of data terminal equipment (DTE), and a modem, which is a type of data communication equipment (DCE). The standard has evolved over the years with the latest revision 'F' released in 1997. The standard is now known as TIA/EIA-232-F, with TIA standing for the Telecommunications Industry Association and EIA standing for the Electronic Industries Association.

As with previous revisions of the standard the maximum data rate is defined as 20 kilobits per second (kbps) although there are now a number of software applications that push this data rate above 200 kbps, well outside the standard. The maximum line length for a 232 connection is defined in terms of load capacitance. The maximum load capacitance is specified as 2500 pF, which indicates the uses of standard cables between 15 and 20 meters long. Line length and signaling rates are limited, as the standard employs single-ended communication that is prone to external factors.

TIA/EIA-422-B and TIA/EIA-485A

TIA/EIA-422-B (422) specifies a balanced transmission circuit whose maximum line length is undefined but is nominally 1.2 km for 24-AWG cable, based on 6-dB signal attenuation. The maximum signaling rate also is undefined but is specified by the relationship of signal rise time to bit time, which is influenced by the line driver, the line length, and the line loading. In the majority of applications, it is the line length that is the limiting factor on signaling rate due to signal dispersion. TIA/EIA-485-A (485) is primarily an upgrade to the 422 standard which allows half-duplex and multiplex transmission modes. It specifies only the electrical layer of the transmission scheme, and hardware such as the connector is left to the user to define.

TIA/EIA 644

TIA/EIA-664 (644) was developed by the TR30.2 committee of the TIA to address the demand for ever-increasing signaling rates and lower power consumption. It is similar to 422 in that it is a balanced signaling scheme for simplex or distributed simplex circuits. It differs in the common-mode voltage range and driver output levels, both of which reduce the maximum transmission distance relative to 422 but allow higher signaling rates, lower power, and lower EMI.

Low Voltage Differential Signaling (LVDS)

LVDS

- **L**ow **V**oltage **D**ifferential **S**ignaling
- Signaling method used for high-speed, low-power transmission of binary data over copper.
- Intended application if for baseband data transmission over controlled impedance media of approximately 100 Ω, where the transmission media may be printed circuits board (PCB) traces, backplanes, or cables.
- Standards include
  - ANSI TIA/EIA-644
  - IEEE 1596.3

4-10

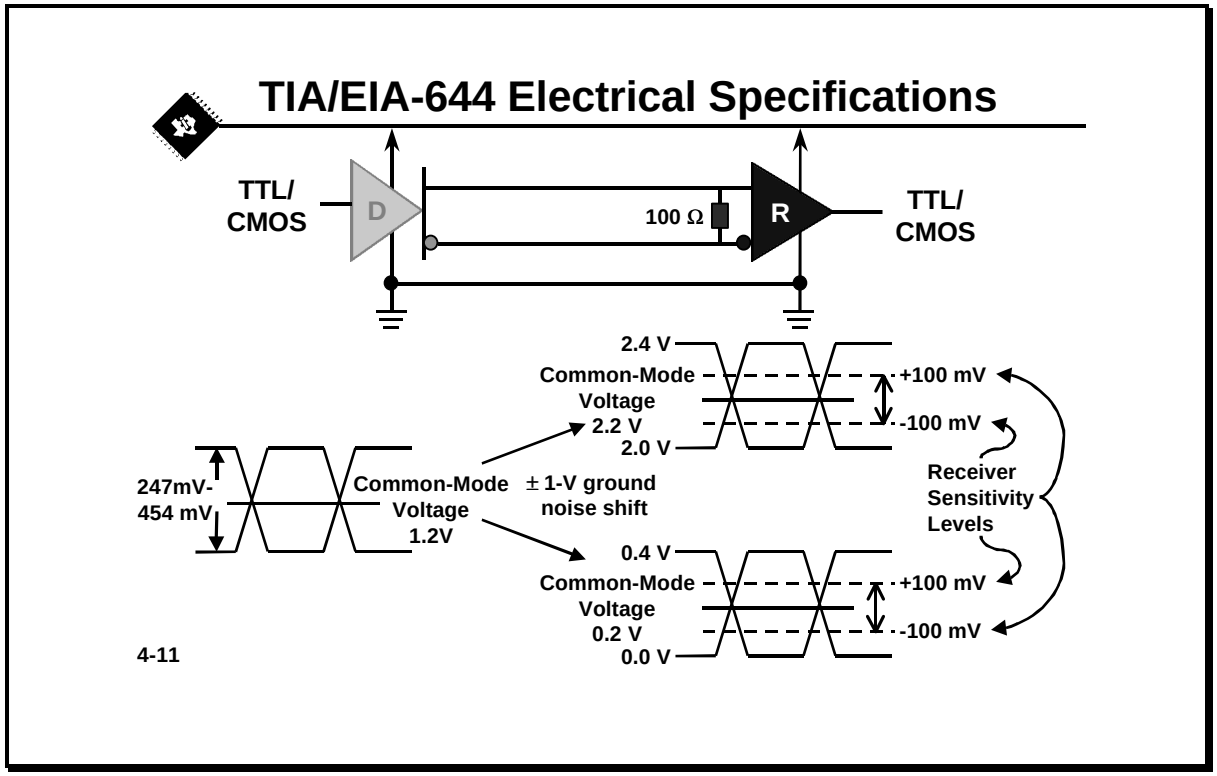
LVDS Definition

Low voltage differential signaling (LVDS) technology is redefining data transmission at the physical layer interface where many of the critical bottlenecks occur in any application that requires high bandwidths. LVDS brings high speeds, low power and low EMI to today's and tomorrow's networking, telecommunications and multimedia applications. It is the most promising technology for this physical layer interface.

Two new standards define LVDS, ANSI TIA/EIA-644 and IEEE 1596.3-1996. The standard TIA/EIA-644 "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits", provides a general-purpose interface for signaling rates as high as 655Mbps (megabits per second). The standard specifies the electrical characteristics of the driver and receiver, along with minimum media specifications and fail-safe operation of the receiver under fault condition. It does not define functional specifications such as the hardware nor protocols. The IEEE's 1596.3-1996 "IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)" specifies signaling levels (electrical specifications) for the physical-layer interface and also defines signal encoding that allows transfer of SCI packet over data paths. The standards are compatible and may communicate at the electrical level. The former standard is

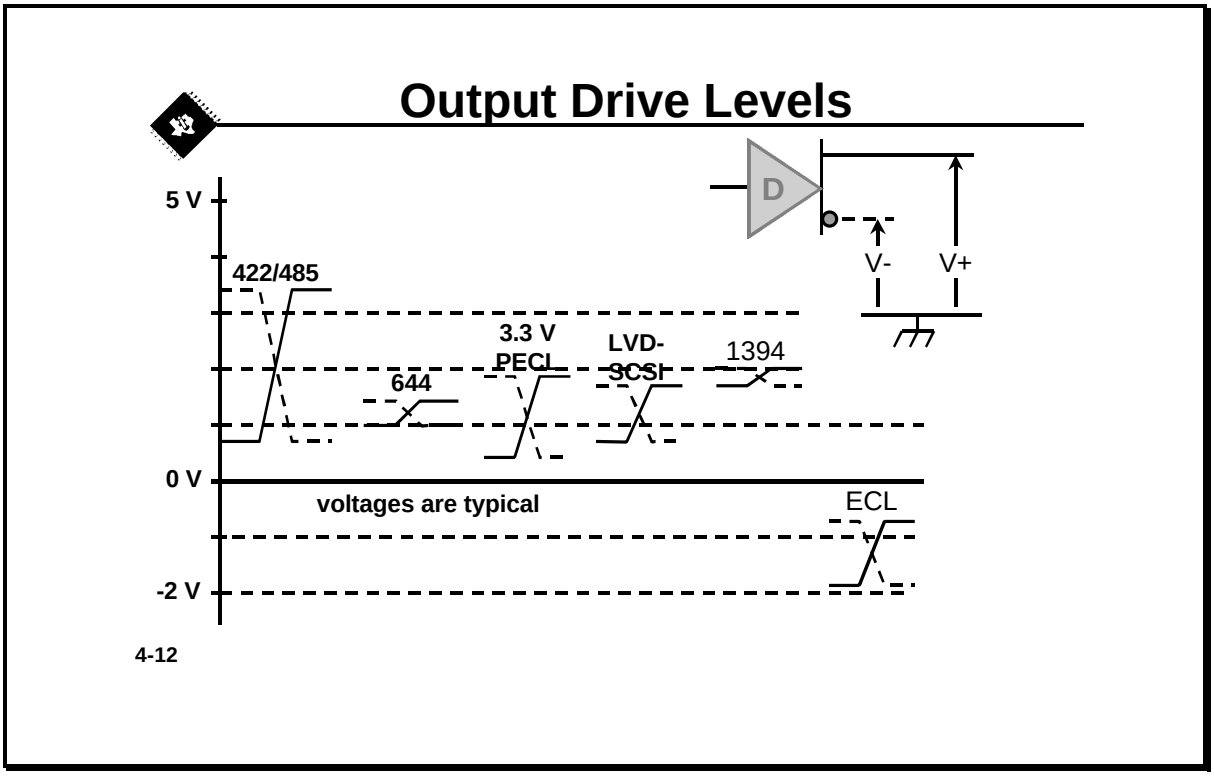
the more generic and popular of the two, and is the basis of the rest of this presentation and the standard TI's LVDS products meet and exceed.

TIA/EIA-644



Electrical Specifications

The LVDS driver accepts TTL/CMOS input levels and transforms them using current-mode drivers to deliver a differential output in the range of 247 mV to 454 mV with a typical offset voltage of 1.2 V relative to ground. The transmission line must be terminated and matched to its impedance to complete the current loop and to terminate high speed signaling. At the end of the line, the receiver is capable of detecting signals as low as ± 100 mV with as much as ± 1-V ground noise. The recommended voltage applied to the receiver is between ground and 2.4 V with a common mode range of 0.2 V to 2.2 V.



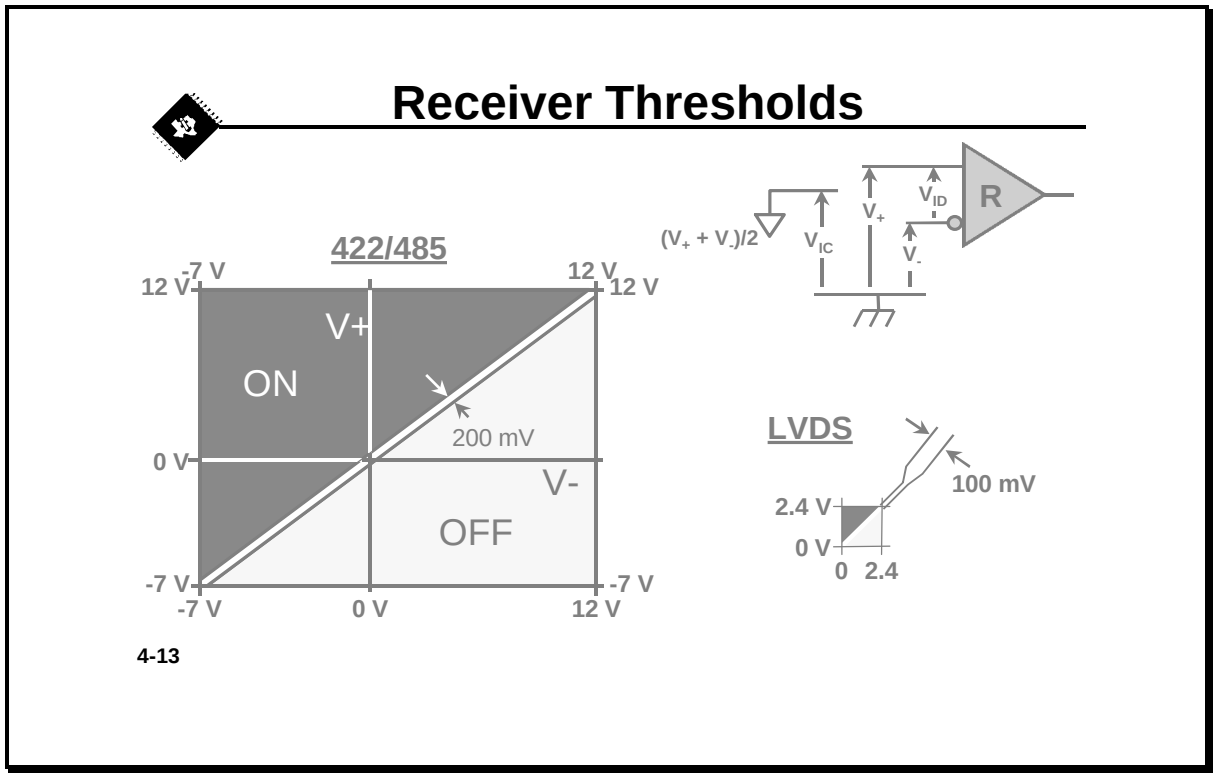
Above is a detailed comparison of output drive levels between TIA/EIA-644 and other technologies for driving 100 ohm and lower line impedance. As may be noted LVDS has one of the lowest offset voltage and lowest voltage swings. In order to transmit data over a long distance 422 and 485 need large voltage swings. PECL and ECL are both consider “power-hungry’” technologies by today’s standards and ECL has the disadvantage of needing to use multiple supplies. LVD-SCSI is the proposed standard of 1142-D SCSI Parallel Interface-2 (SPI-2) and has all the benefits of LVDS for multiplex applications.

EMI

LVDS offers low electromagnetic interference (EMI) due to its low-voltage signaling and differential data transmission. The typical 350-mV low-voltage signaling has switching currents much lower than CMOS/TTL and thus offers less radiation of EMI. Of greater importance is that the balanced differential lines have equal but opposite signals. The concentric magnetic fields radiated by each of the two conductors react with one another, bending toward each other and, ultimately, cancel a significant portion of the EMI emissions each of the two lines would generate on their own.

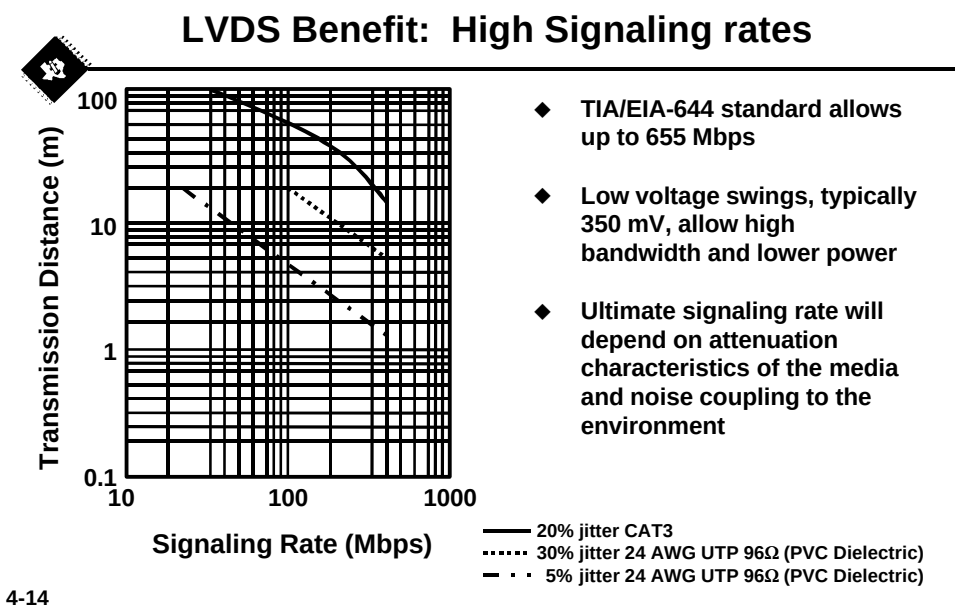
There are many design considerations that need to be implemented to reduce EMI. For example, signal traces must be as close to each other as possible and matched in length and there should only be one path for return current between the host controller and the target controller PCBs.

More on EMI testing may be found in TI's application note "Reducing EMI with Low Voltage Differential Signaling".



Above are the LVDS receiver thresholds compared to 422/485. The threshold on 422/485 is needed for transmitting over long distances in noisy environments and thus is quite large. In order to reduce power and have high signaling rates, LVDS standard specifies a common-mode range of ±1 V with a 1.2-V offset. Meaning the receiver threshold varies from 0 to 2.4 V. Although this range may not sound very large, it offers twice the noise margins of others reduced-swing interface standards such as BTL and GTL. Furthermore, LVDS has a receiver sensitivity of 100 mV, which offers better signal reliability as compared to 422/485's 200 mV.

LVDS Benefits



TIA/EIA-644 specifies drivers and receivers capable of operating at data signaling rates up to 655Mbps, and a theoretical maximum limit is calculated at 1.923 gbps. LVDS greatly exceeds the signaling rate capabilities of former differential standards like 485 and 422. And although PECL and ECL devices are also capable of high data rates, they can consume up to 10 times more the power than LVDS.

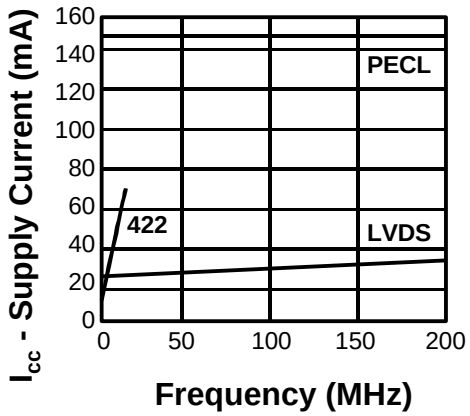
Since the differential transmission in LVDS greatly reduces noise, lower signaling swings may be used. Without the use of lower signaling swings, data rates could not be raised. The less a voltage level must change, the faster it can achieve the desired state. The LVDS signals change a maximum of 454 mV and a minimum of 247 mV, centered at 1.2 V with respect to the driver ground. These swings are several times lower than traditional TTL/CMOS swings.

LVDS devices may be used in PCB traces, backplanes, or cable environments. Since neither standard specifies a transmission media, any of the copper transmission-media options may be used. Each application has its own set of requirements, and the ultimate rate and distance of LVDS data transfer will be dependent on the attenuation characteristics of the media and the noise coupling to the environment.

The graph shown above plots different signaling rates vs. distance according to cables used when transmitting LVDS signals. Balanced cables are recommended over unbalanced cables due to their noise reduction and thus better signaling quality. As expected, on the graph it may be noted that UTP

cables have a lower performance than CAT3 cable. At high signaling rates it becomes imperative to use high quality cable such as CAT3 or CAT5.

LVDS Benefit: Low Power



- Current-mode driver -- more power efficient than the previous voltage-mode drivers
- Low voltage swings of 350 mV
- Power consumption is relatively independent of frequency (Icc vs Frequency plot)
- Ability to operate independently from the power supply voltage

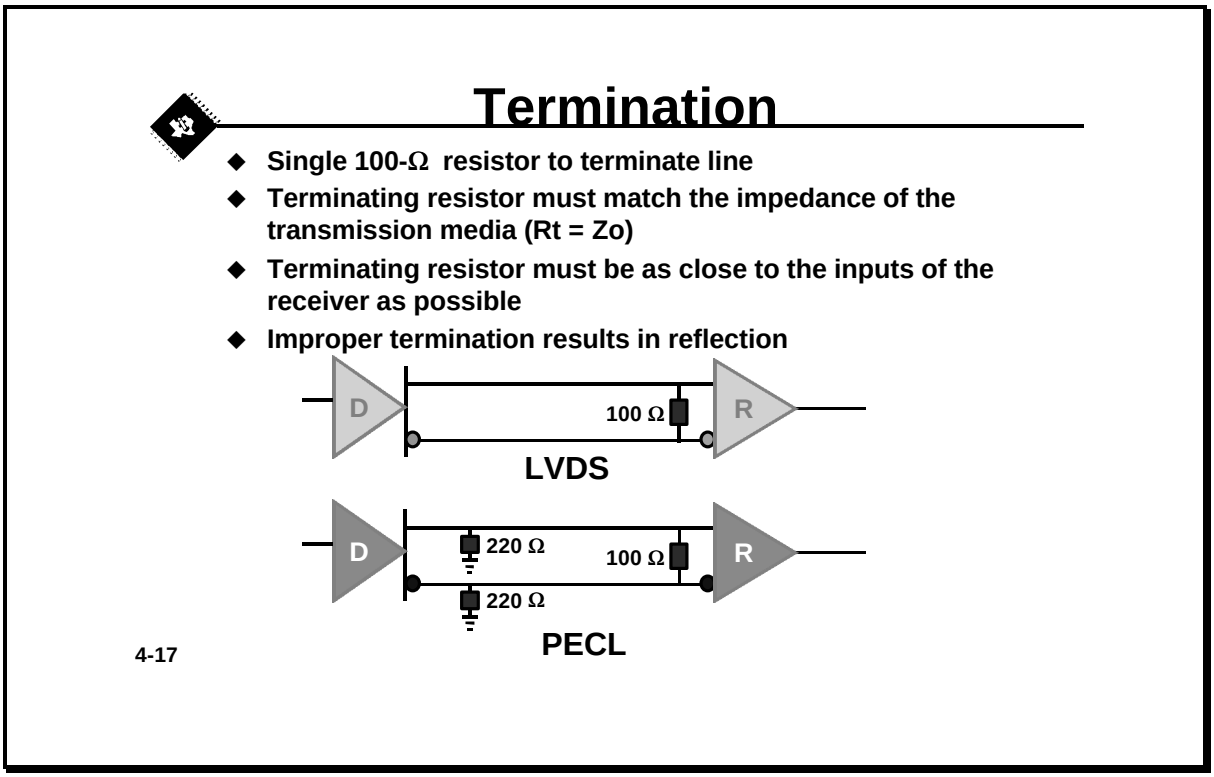
4-15

Current-mode drivers and low voltage swings allow LVDS to have low power. Since LVDS is a differential transmission, noise is reduced. This allows for low voltage swings (350 mV typical) to be used which reduce power dissipation. Current-mode drivers are more power efficient than voltage-mode drivers as previously used in other standards. The current-mode drivers produce a constant current, which allows power consumption to be relatively independent of frequency. Meaning, driver power consumption remains almost constant as operating frequency increases.

The graph above shows LVDS supply current compared to PECL and 422. As you can see the LVDS driver I_{CC} is about 1/8 that of PECL and as the frequency increases, it is also evidently lower than 422. The lower voltage of LVDS and its current-mode drivers greatly reduce power and, as shown on the graph, the I_{CC} of LVDS remains virtually flat over the frequency range.

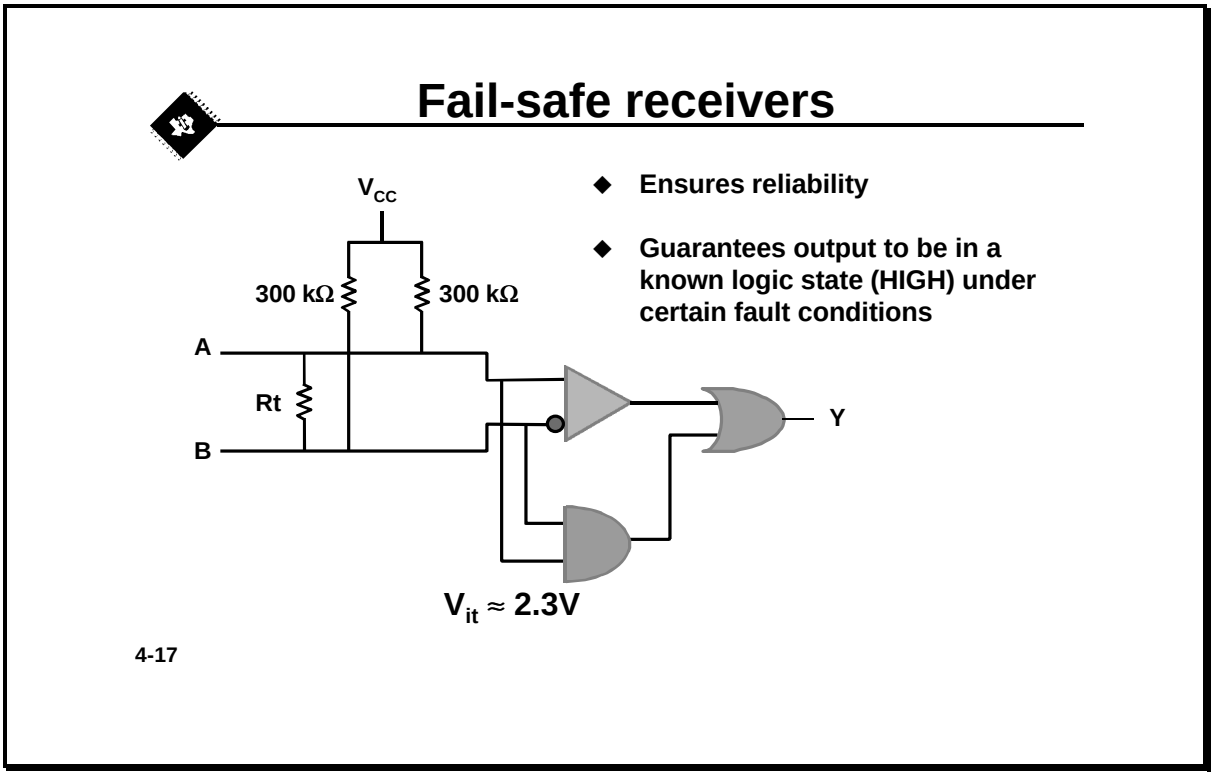
Another characteristic of LVDS is its independence of power supply. Neither of the standards specify power-supply voltages. The supply voltage may be 5 V, 3.3 V, and even go as low as 2.7 V since the differential signal centers at 1.2 V. LVDS may be used at lower supply voltages while still maintaining the same signaling levels and performance. This feature facilitates design for systems that may be moving to lower voltages in the near future.

Designing with LVDS



Termination at the far end of the interconnect from the transmitter is mandatory. A termination resistor matched to the impedance of the transmission media (±10%) prevents reflections that cause noise. Ideally, Rt=Zo. The value of the resistor is recommended to be between 90 Ω to 132 Ω. The resistor should be located within 2 cm of the LVDS receiver. Stub lengths greater than 2 cm will cause the propagating signal to bounce off the high impedance end of the stubs and degrade the signal. Proper terminations not only avoid reflection problems, but also reduce unwanted electromagnetic emissions.

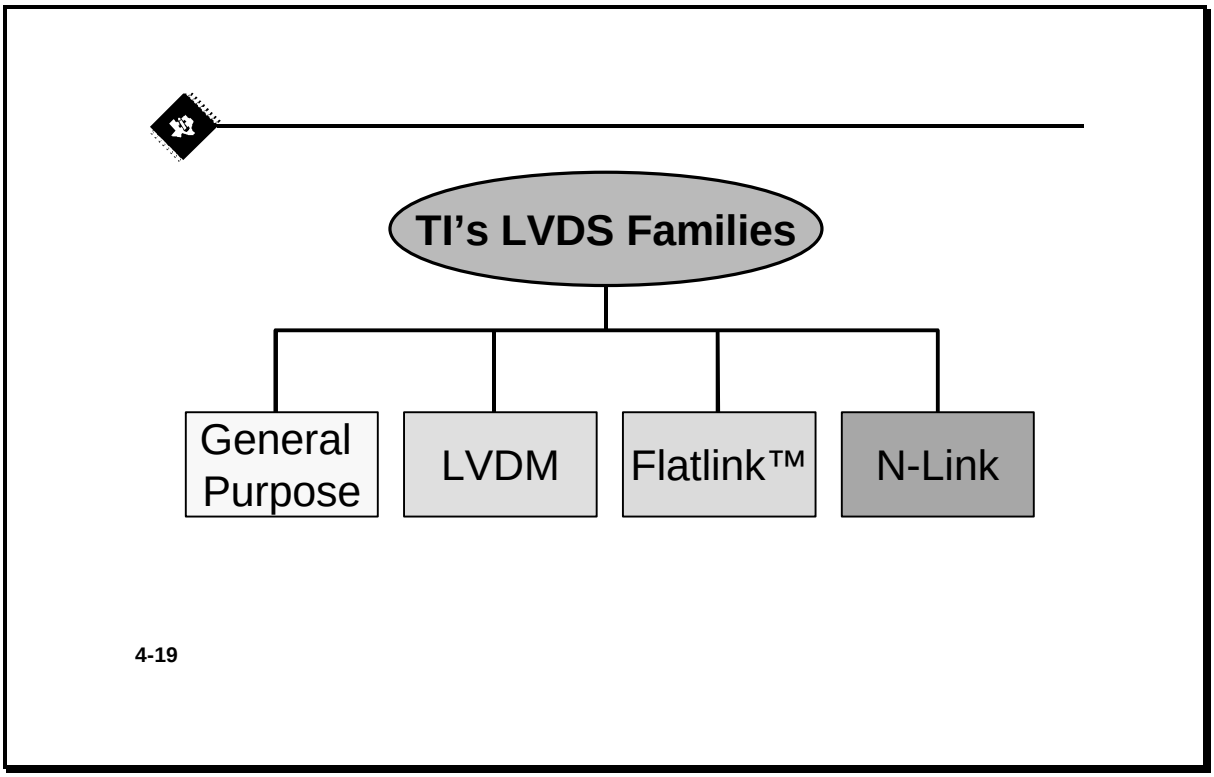
The simplicity of the LVDS termination scheme makes it easy to implement in most applications. ECL and PECL require more complex terminations than the single resistor solution for LVDS. PECL drivers use two 220-Ω pull-down resistors at the outputs of the driver and a 100-Ω resistor at the input of the receiver. LVDS simplifies the layout and lowers the cost by terminating the line with a single 100-Ω resistor.



One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receivers are like most differential line receivers, in that, its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV when within its input common-mode voltage range. This situation occurs when there is little or no input current to the receiver from the data line itself, known as open circuit. This may happen when the driver is in a high-impedance state or the cable is disconnected. The LVDS receiver is different in how it handles the open-input circuit situation however.

When the system is in open-circuit, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-kW resistors as shown above. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage. It is only under these conditions that the output of the receiver will be valid with less than a 100mV differential input voltage magnitude. The presence of the termination resistor, R_t, does not affect the fail-safe function as long as it connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pull-up currents from the receiver and the fail-safe feature.

LVDS Products



TI has four LVDS families that support various configurations and applications. The General-purpose, Flatlink and N-Link families meet or exceed TIA/EIA 644, the LVDM family offers all of the LVDS benefits in multiplex and half-duplex applications (note: multipoint application was not covered in 644, the standard for multipoint LVDS is currently being written and TI takes part in that committee).

General-Purpose:

As the name implies these are general-purpose drivers, receivers, and drivers/receivers which follow popular, industry footprints. TI offers a variety of configurations of these devices to help designers have the most cost-effective solution to their LVDS needs. This family is characterized for signaling rates up to 400 Mbps, 3.3-V power supply, and ESD greater than 8 kV.

LVDM:

The LVDS family allows for multiplex and half-duplex interconnections. Although this family is not under the 644 standard it offers all of the LVDS benefits. TI takes part in the committee that is working on the development of this new standard. This family requires higher output currents, more sensitive receivers, and termination at both ends of the transmission line (~50 Ω each). The devices may be used to implement any type of multipoint parallel differential bus including proprietary buses, backplane systems, and direct board-to-board connections.

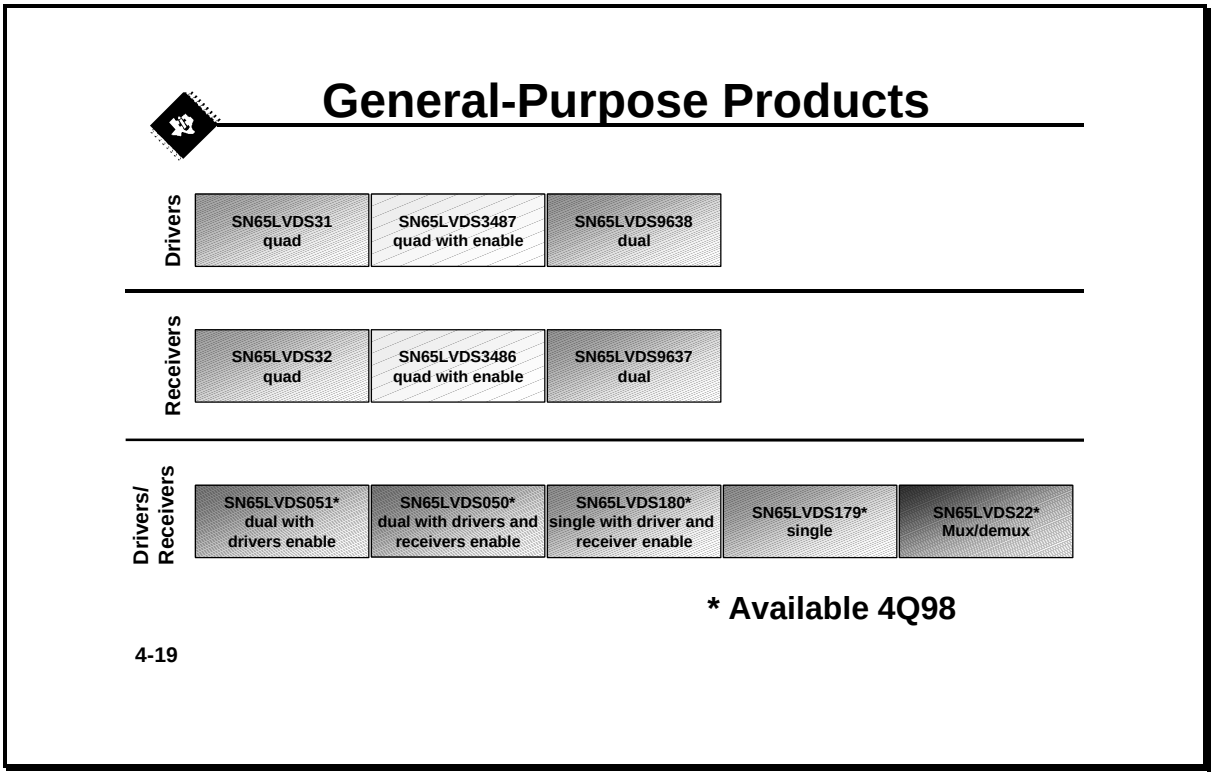
Under this family there exist the LVD-SCSI transceivers which are SPI-2 compliant transceivers (SN75LVDM976/977).

Flatlink:

Flatlink devices are PLL based transmitters and receivers with a throughput of 1.3 - 1.8 Gbps and a serialization of 28:4 and 21:3. Flatlink was developed to transfer data and control signals from portable computer video display processors to flat-panel displays.

N-Link:

N-Link is TI's newest LVDS family, which supports the needs of networking and telecom equipment developers. N-link devices, like Flatlink, are PLL based transmitters and receivers with a throughput of 1.3 - 1.8 Gbps and serialization of 28:4 and 21:3.



The above devices all fall under the category of general -purpose LVDS products. All devices meet or exceed TIA/EIA-644 and have some general characteristic in common. For example, all devices in the general-purpose category are single 3.3-V supply voltages and have a minimum of 8 kV ESD on the bus pins. These features, and all those shown on the slide, provide substantial benefits that enhance a system's performance resulting in total system cost savings.

The General-purpose products may be used in simplex and distributed simplex interconnections. The simplex interconnection is the preferred solution. Signal quality is superior in this uncomplicated configuration since no stubs or discontinuity in impedance are present. In distributed simplex configuration up to 17 receivers with no common-mode termination and up to 36 receivers with common-mode termination may be tied to the bus. The stubs between the line and each receiver must be kept to a minimum (<7 mm) since at high signaling rates they may act as transmission lines creating reflections and they may also cause an impedance discontinuity. A terminating resistor must only be placed at the end of the transmission line as shown above. Multiple terminating receivers would attenuate the signal since they would present a low impedance load to the driver.

SN65LVDS31/32-16-pin quad driver and receiver are the first general-purpose devices TI released. They follow the popular pin-out (footprint) of AM26LS31 and AM26LS32.

SN65LVDS3486/87-16-pin quad driver and receiver which feature an enabling scheme whereby only two of the four drivers or receivers may be enabled at a time instead of requiring that all four lines are enabled simultaneously as is the case with the ‘LVDS31/32.

SN65LVDS9637/9638-8-pin dual driver and receiver have the same innovative characteristics as the quad drivers and receivers. These devices follow the industry’s standard pin-configuration of μA9638 and μA9637 for easy flow-through interconnections.

SN65LVDS179/180-each has a single driver/receiver. The ‘LVDS179 comes in an efficient 8-pin package. The ‘LVDS180 feature an enabling scheme which allows the device to be used as a single driver, or as a single receiver, or as a driver/receiver; it is in a 14-pin package.

SN65LVDS050/051- both devices contain two drivers and two receivers. The ‘LVDS050 has an enabling scheme that allows the designer to operate only the drivers, or only the receivers, or all the drivers/receivers. The ‘LVDS051 has an enabling scheme for the drivers only. The designer can choose to operate both drivers or only one driver. Both devices are 16-pin packages

SN65LVDS22-It’s a dual 2:1 mux or 1:2 splitter with LVDS inputs and outputs. The receiver outputs can be switched to either driver or both drivers through multiplexer control signals. This characteristic allows the flexibility to perform splitter or signal routing functions with a single device. This product solves many of the designer’s headaches of muxing and splitting signals in a one-chip LVDS solution. The ‘LVDS22 is also available with twice the output current to accommodate multipoint applications and it is designated the SN65LVDM22 featured in the next slide.

General-Purpose Products Features

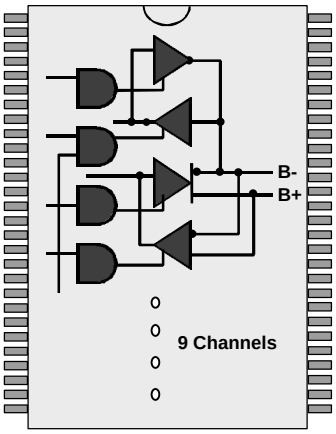
- **Signaling rates up to 400 Mbps**
- **Low-power**
  - **25 mW/driver at 400 Mbps**
  - **60 mW/receiver at 400 Mbps**
- **ESD protection exceeds 8 kV (HBM) on bus pins**
- **Single 3.3-V power supply**
- **5-V tolerance on LVTTL pins of drivers/receivers**

4-21

LVDM Product:

SN75LVDM976 and SN75LVDM977

- 9 channel dual-mode SCSI transceiver
- Supports single-ended and LVD-SCSI
- Up to 40 Mxfers/s
- ‘LVDM976 -- CMOS
- ‘LVDM977 -- TTL



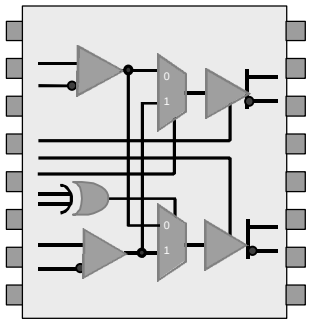
4-22

TI’s LVDM products are the ultimate solution to multiplex and half-duplex interconnections. These products enable bi-directional connections while still enjoying all the LVDS benefits. Their application usually includes any type of multipoint differential bus including proprietary buses, backplane systems and direct board-to-board connections.

The SN75LVDM976/977 were the first discrete transceivers in the industry to support both single-ended and LVD signaling. These devices allow designers to upgrade their small computer system interface (SCSI) peripheral devices and other products like SCSI host bus adapters to the faster data transfer rates and longer bus segments of LVD-SCSI while still maintain compatibility with existing single-ended signaling. The LVDM976/977 has all of the benefits of LVDS such as significant power reduction and low EMI. They are available in TSSOP packaging with 20-mil lead pitch, which reduces the board area and follows the popular pin-out of its predecessor SN75976A.

LVDM Product: SN65LVDM22

- Dual mutliplexed LVDS repeater
- Performs splitter or signal routing functions
- Single 3.3-V power supply
- Up to 400 Mbps
- Available 4Q98



4-23

The SN65LVDM22 is a dual 2:1 mux or 1:2 splitter with LVDS inputs and outputs. The receiver outputs can be switched to either driver or both drivers through multiplexer control signals. This characteristic allows the flexibility to perform splitter or signal routing functions with a single device. This product solves many of the designer's headaches of muxing and splitting signals in a one-chip LVDS solution. The 'LVDM22 has twice the output current than the SN65LVDS22 (general-purpose LVDS) in order to support multipoint applications.

Device available 4Q98

Flatlink and N-link Products

Flatlink

Device	Description	Throughput (MHz)	Clock Trigger	TSSOP Package
SN75LVDS81	28-bit transmitter	68	falling	56-pin
SN75VLDS82	28-bit receiver	68	falling	56-pin
SN75VLDS83	28-bit transmitter	68	selectable	56-pin
SN75VLDS84	21-bit transmitter	68	falling	48-pin
SN75VLDS85	21-bit transmitter	68	rising	48-pin
SN75LVDS86	21-bit receiver	68	falling	48-pin

N-Link

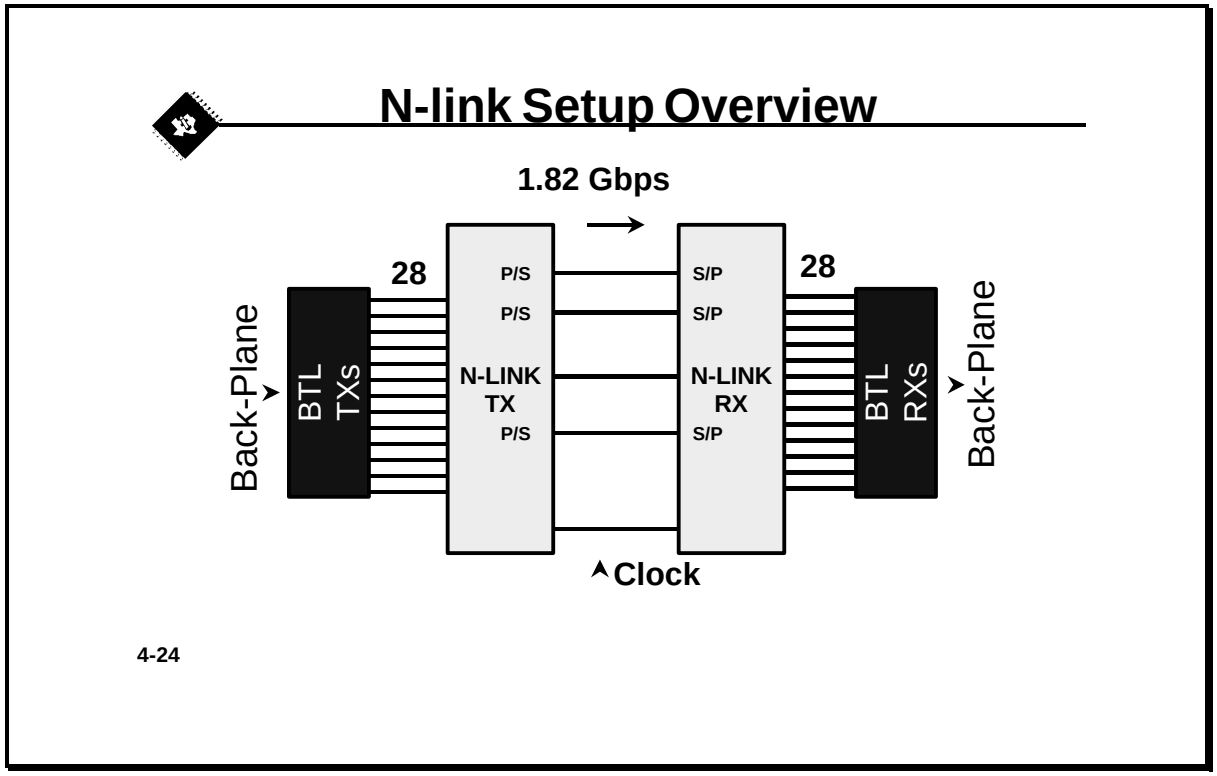
Device	Description	Throughput (MHz)	Clock Trigger	TSSOP Package
SN65LVDS93	28-bit transmitter	68	selectable	56-pin
SN65VLDS94	28-bit receiver	68	rising	56-pin
SN65VLDS95	21-bit transmitter	68	rising	48-pin
SN65VLDS96	21-bit receiver	68	rising	48-pin

4-25

Currently, developers are using proprietary solutions that often require a large number of parallel lines in order to meet their high bandwidth backplane inter-connect requirements. As bandwidth requirements increase over time, these designs will become more complicated. Flatlink and N-Link provide developers with a more elegant solution and a better performance roadmap that does not require a complete re-design to their equipment.

Some of the advantages of Flatlink and N-link include:

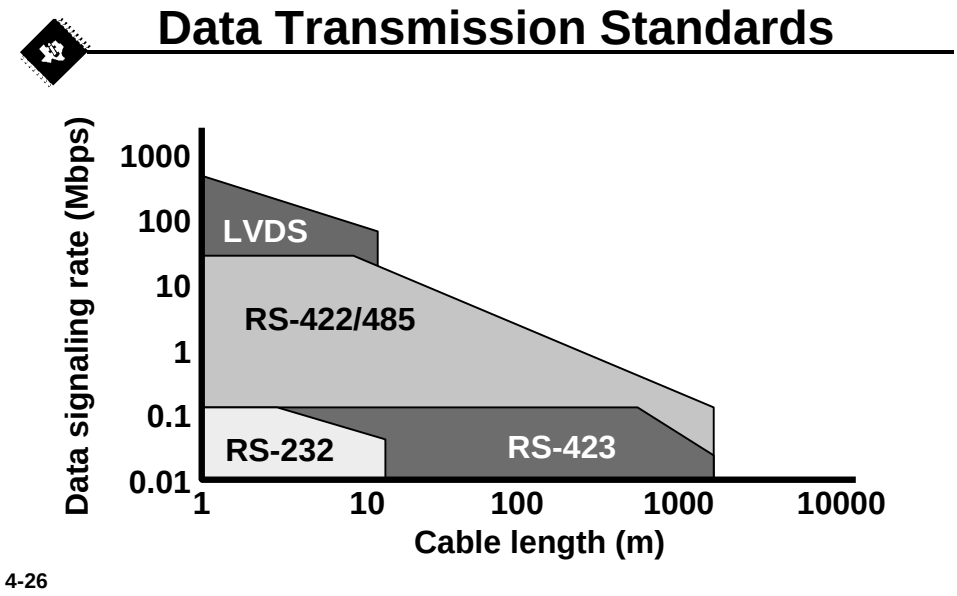
- Substantial reduction in cable size
- No ground referencing needed
- Reduction of EMI
- Overall throughput of 1.82 Gbps
- Power down mode = 1mW
- Simpler design , More cost effective, Faster time to market



N-Link can provide multiple Gbps of throughput in any one direction. The above application can easily be replicated in the opposite direction to provide a full duplex solution running at 1.8 Gbps.

Each of the LVDS lines above actually represent an LVDS balanced twisted pair cable or copper trace pair. This enables N-link to serialize 28 data channels into 4 LVDS balanced pairs for transmission to the receiver; in addition a clock line is also sent to the receiver to synchronize the PLL.

RS-232, 422 and 485 Products



As shown in the beginning of this presentation, besides LVDS there are other standards which TI supports. TI has 30 years of experience in the Data Transmission arena; and it is therefore no wonder that along with its efforts to extend the data transmission capabilities of new technologies like LVDS, it also continues to improve currently implemented transmission specifications such as 232, 422, 485, and others.

The preceding are some more of TI's products offerings in Data Transmission.

TI's 422/485 Technology Selection

	172	173	174	175	176	179	180	184
Bipolar	X	X	X	X	X	X		
ALS	X	X	X		X		X	
LBC	X	X	X	X	X	X	X	X

	Bipolar	ALS	LBC
Power	high	moderate	**LOW**
Max Speed	10 Mbps	**30 Mbps**	12 Mbps
Cost	**LOW**	moderate	higher

4-27

TI's 422/485 family may be easily arranged into 3 sub-categories according to the technology used: 1) Bipolar, 2) Advanced low-power Schottky (ALS), and 3) LinBiCMOS™ (LBC). Depending on the system specifications, one of these sub-categories may well fit the specific system care-abouts. For example, if a designer's concern is low power in a 485 device, s/he would be advice to look into the LBC family of TI's 422/485 products. LinBiCMOS technology has the best features of CMOS and bipolar processes of fast switching speeds, low quiescent power, high voltage breakdowns, voltage or current precision, and stability.

By offering different technologies in 422/485 products, TI aims to provide the most innovative and complete product offering in the industry. This broad selection of products is bound to give the designer the most cost-effective and easy-to-design-with solution for their data transmission needs in 422/485.

TIA/EIA-485 Products

	Driver/ Receiver	Device	Key
Line Drivers	4/0	SN75172	Industry Standard
		SN75174	Industry Standard
		SN75ALS172A	High Speed
		SN75ALS174A	High Speed
		SN75LBC172	Low Power
		SN75LBC174	Low Power
Line Receivers	0/4	SN75173	Industry Standard
		SN75175	Industry Standard
		SN75ALS173	High Speed
		SN75LBC173	Low Power
		SN75LBC175	Low Power

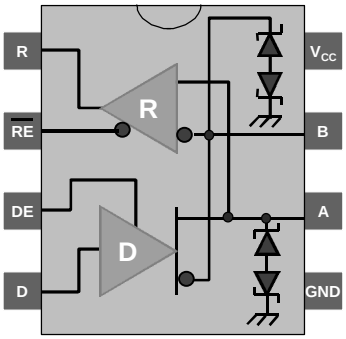
	Driver/ Receiver	Device	Key
Line Transceivers (Drivers / Receivers)	1/1	SN75176A	Reduced Slew-rate
		SN75176B	Industry Standard
		SN75178B	Standard Repeater
		SN75179B	Industry Standard
		SN75ALS176	High Speed
		SN75ALS176A	Very High Speed
		SN75ALS176B	Ultra High Speed
		SN75LBC176	Ultra- Low Power
		SN75LBC179	Low Power
		SN75ALS180	Full Duplex Com
		SN75LBC180	Low Power
		SN75ALS181	Full Duplex Com
		SN75LBC184	Transient Suppression
	2/2	SN751177	High Speed
		SN751178	High Speed
		SN75ALS1177	High Speed
		SN75ALS1178	High Speed
	3/3	SN75ALS170	High Speed
		SN75ALS170A	High Speed, Low power
		SN75ALS171	High Speed
		SN75ALS171A	High Speed, Low power
	9/9	SN75976A1/A2	High Speed
		SN75LBC978	Low Power + WRAP
		SN75LBC968	Active Termination

4-28

Standards, such as 485 and 422, are differential technologies that are used in a broad selection of general-purpose applications, including industrial control, telecommunications, point-of-sale terminals, alarm systems and other environments that are high in electrical interference. TI offers a wide variety of these products which include many combinations of drivers, receivers and transceivers. Among TI's 485 products also exist 9-channel SCSI transceivers, which have taken differential SCSI into a new level of performance. TI's discrete SCSI transceivers such as the SN75976A and the SN75LBC976 offer designers a cost-effective solution to their multipoint applications without having to adhere to expensive ASICs. TI also offers single-ended SCSI transceivers such as the SN75LBC968 and LVD-SCSI transceivers such as the SN75LVDM976/977 (shown previously).

RS-485 Transceiver with Transient Suppression

SN65LBC184 and SN75LBC184



SN65LBC184
SN75LBC184

- **Integrated transient voltage suppression (400-W peak)**
- **15-kV ESD on bus pins (IEC1000-4-2 compliance)**
- **Improved data transmission at 250 Kbps**
- **1/2 unit load -- up to 64 similar devices connected on a bus**
- **Controlled driver slew rates**

4-29

The SN65/75LBC184 is the industry's first '176 standard footprint 485 differential transceiver to offer integrated transient voltage protection up to 400-W peak. The SN65/75LBC184 provides significant protection from large over-voltage transients on the bus pins, which can be caused by secondary effects of a lightning strike or power system switching disturbances.

These devices are well suited for electrically noisy environments requiring large over-voltage and common mode swing protection. The SN75LBC184 and SN65LBC184 provide substantial benefits for improved reliability and enhanced system performance resulting in total system cost savings.

Transient voltage suppression – protection from large noise transients to reduce down time

Integrated solution – on-chip to minimize cost and printed board-space requirement

Controlled driver slew rates – for reduced EMI and improved data transmission at 250 Kbps over longer unterminated cable runs and stub lengths

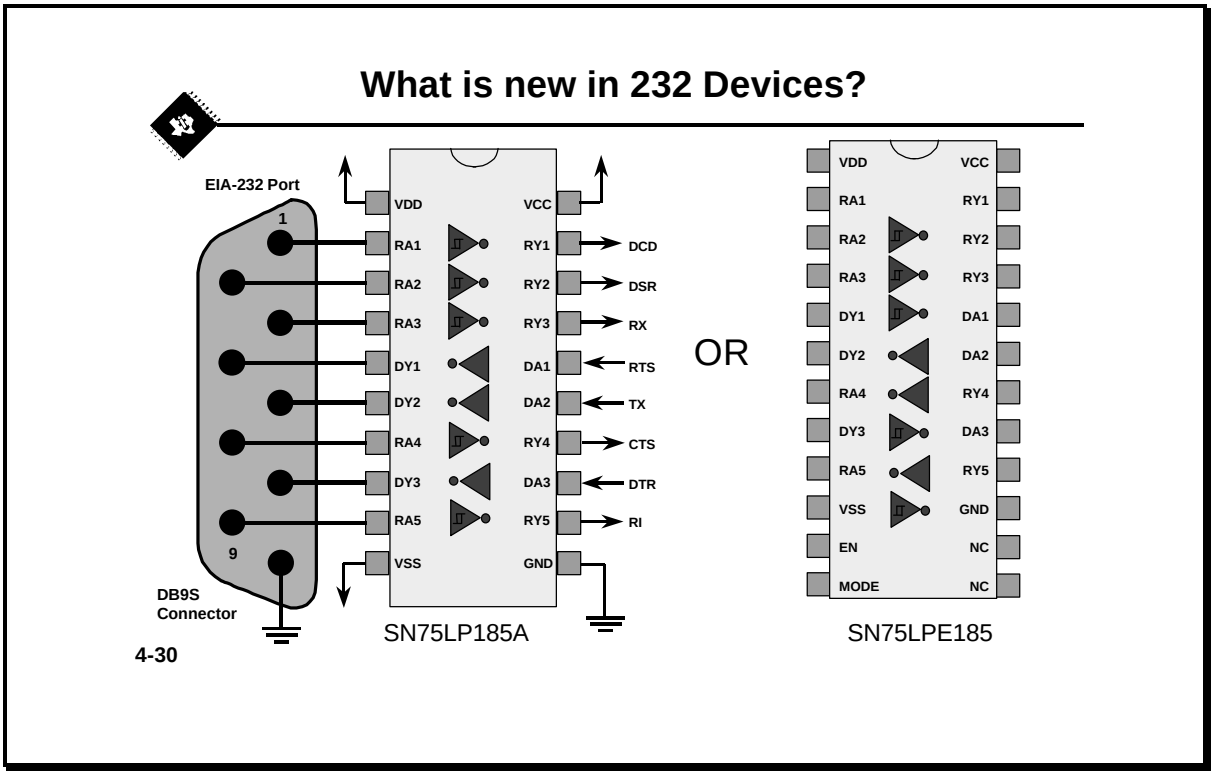
15 kV ESD (HBM)– Improves system's reliability.

Half unit load – for up to 64 similar devices connected on a bus

Compatibility – drop-in replacement of current '176 designs and meets or exceeds EIA RS-485 and ISO/IEC 8482:1993(E) standards.

The SN65/75LBC184 is a cost-effective, footprint- compatible, device delivering a high level of bus protection without the need of external discrete clamping diodes and costly multi-chip modules.

These devices are available in 8-pin DIP and SOIC. The SN65LBC184 is characterized for industrial temperatures (-40° to 80 ° C) while the SN75LBC184 is characterized for commercial temperature (0 ° to 70 ° C)



The SN75LP185A and SN75LPE185 shown above are application specific to the 9-pin DB9S Personal computer Data Terminal Equipment (DTE) serial interface, which effectively is a subset of the full 232 standard. As a semiconductor manufacturer, TI finds that the majority of 232 applications are moving to this interface. Due to the nature of the signals (five receiver and three transmit line), the older established 232 products no longer provide an optimum solution. This interface is now driving the need for single-chip 232 solutions. Additional features such as single-supply operation, higher data-signaling rates, voltage-clamped outputs, increased ESD protection, and power-down modes have evolved from the desirable features to the essential features of today's interface.

The SN75LP185A and SN75LPE185 are one of TI's first products in this new Family of Next Generation 232 devices. These devices are low-power bipolar products containing three drivers and five receivers with 15-kV ESD protection on the bus pins with respect to each other. The pin-out of the'LP185A matches the flow-through design of the industry-standard SN75185 and SN75C185. The 'LPE185 also follows this same flow-through pin-out, but it adds four pins for control signals. The 'LPE185 has flexible control options for power management when the serial power is inactive. The flow-through pin-out of both devices allows easy interconnection of the UART and serial-port connector of the IBM PC/AT and compatible. The 'LP185A and 'LPE185 combine high data rates (250 kbps), high ESD (15 kV HBM), low power (13.95mW), EMI reduction circuitry, relatively low cost, and the power of TI's World Wide sales and distribution network to the deliver the most resourceful 232 product in the market.