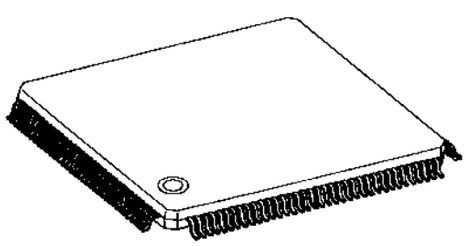
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC90A50F

TENTATIVE

CMOS Image Sensor CAMERA SIGNAL PROCESSING

The TC90A50F realizes digital processing of CIF CMOS Image Sensor CAMERA signals on a single chip.



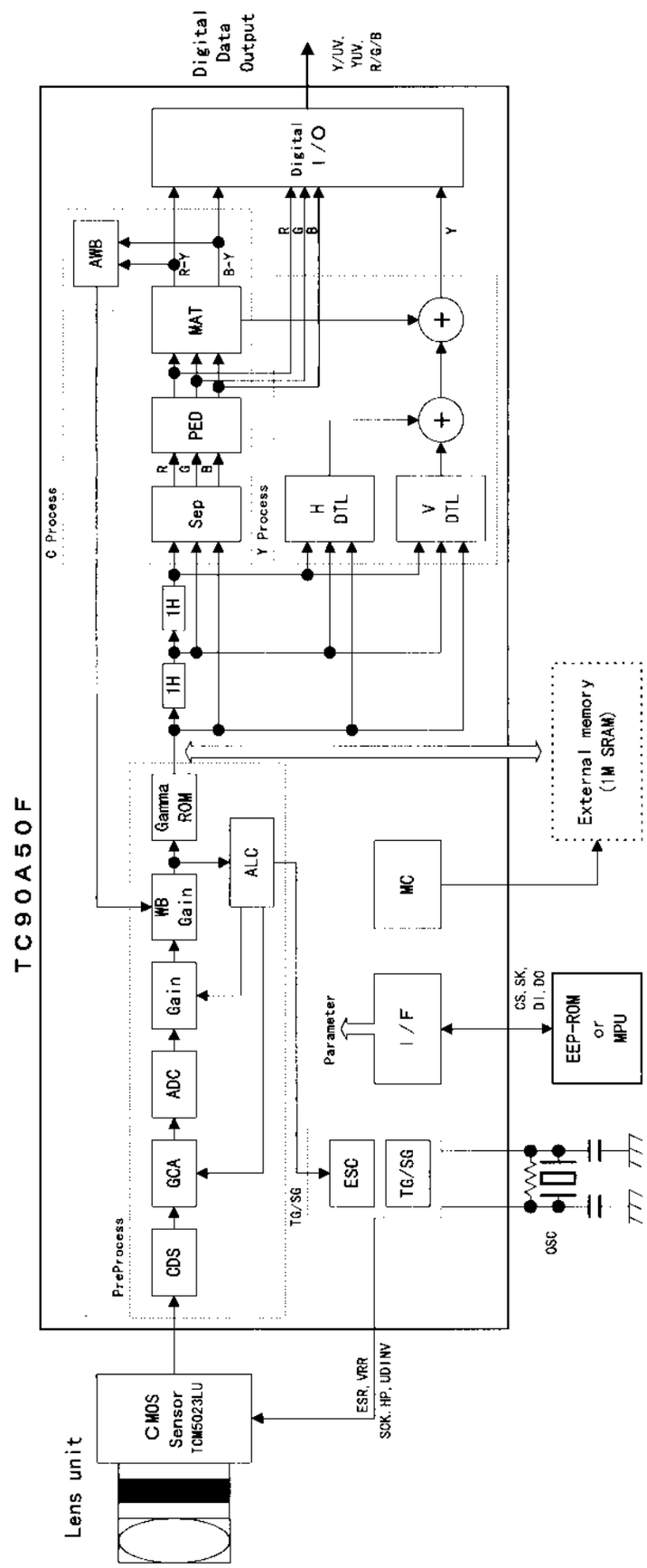
LQFP144-P-2020-0.50A

Weight: 0.891 g (Typ.)

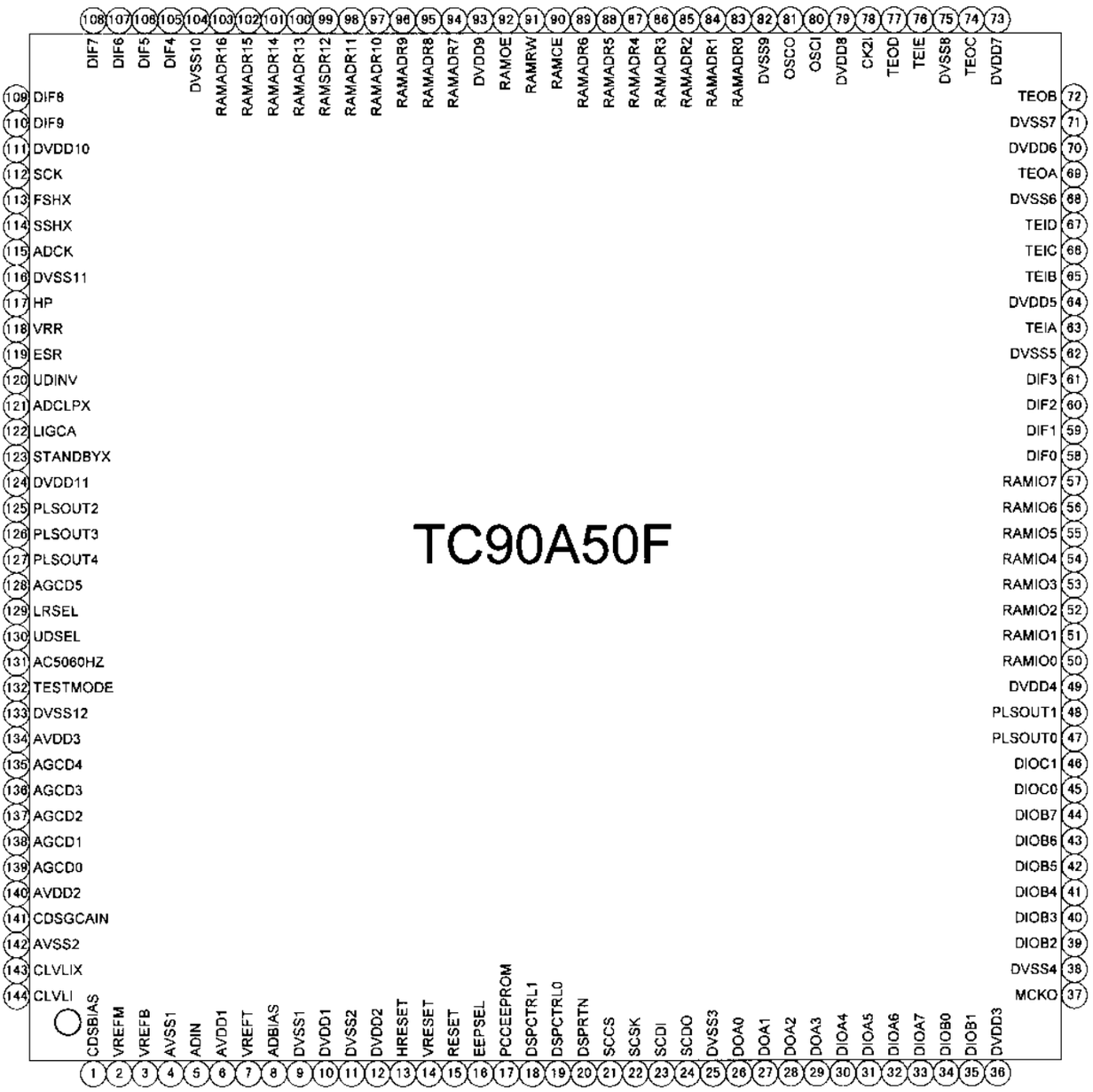
Features

- Built-in CDS(Correlated Double Sampling) system noise reduction circuit
- Built-in Gain control amplifier circuit (+26dB / AGC)
- Built-in 10bit A/D converter
- Built-in CMOS sensor drive pulse generator cicuit/ Sync. pulse generator circuit
- Up and down invert read/Right and left invert read(W/O momory)
- Single oscillator (13.5MHz~27MHz)
- Frame intermittent read(1/2,1/3,1/5,1/9 intermittent)
- Suitable for CIF(352x288) image ,QVGA(320x240) image
- Built-in frame memory control circuit(8bitx375pixelx300line) (Can low speeed read)
- 3-line signal processing based on internal line memories (8bitx375pixelx2line)
- Suitable for CMOS image sensor (TCM5023LU:RGB bayer color filter arry)
- Digital outputs(RGB=6:6:6,8:8:8, YUV=4:2:2, 4:4:4)
- Electronic shutter iris circuit(AES) ,Auto-white balance circuit(AWB) and auto-gain contorol circuit(AGC)
- Can be operated without microcontroller (automatic read circuit make EEPROM set control parameter initial values)
- Control parameters settable by 4-line serial I/F
- Suitable for B/W CMOS sensor(TCM5020LU)
- Single power supply (2.8±0.2V)

BLOCK DIAGRAM



PIN CONNECTION



(NOTE) DVDD1(pin10)、DVDD10(pin111) and DVDD11(pin124) connect to power supply line of sensor.
DVSS1(pin9)、DVSS11(pin116) and DVSS12(pin133) connect to GND line of sensor.

PIN FUNCTIONS

PIN No.	PIN SYMBOL	I/O	FUNCTION
1	CDSBIAS	O	CDS bias pin.
2	VREFM	O	For ADC middle reference voltage. Connect 0.1 μFcapacitor between this pin and GND.
3	VREFB	O	For ADC bottom reference voltage. Connect 0.1 μF capacitor between this pin and GND.
4	AVSS1	—	Internal ADC analog GND 1
5	ADIN	I	Analog input for ADC.
6	AVDD1	—	Internal ADC analog power supply
7	VREFT	O	For ADC top reference voltage. Connect 0.1 μFcapacitor between this pin and GND.
8	ADBIAS	O	For ADC bias voltage. Connect 0.1 μF capacitor between this pin and GND.
9	DVSS1	—	Internal digital GND 1 for sensor
10	DVDD1	—	Internal digital power supply 1 for sensor.
11	DVSS2	—	Internal digital GND 2 for I/O and logic.
12	DVDD2	—	Internal digital power supply 2 for I/O and logic.
13	HRESET	I	MTSG horizontal counter reset pin(detected at fall,always set to high)
14	VRESET	I	MTSG vertical counter reset pin(detected at fall,always set to high)
15	RESET	I	System reset pin(Low:reset).
16	EEPSEL	I	Select read address of EEPROM pin(L:lower area,H:upper area)
17	PCCEEPROM	I	EEPROM automatic read setting(L:OFF H:automatic read)
18	DSPCTRL1	I	Control mode setting pin [1:0] "3":still(with memory) "2":motion
19	DSPCTRL0	I	"1":stand-by "0":sleep
20	DSPRTN	O	Condition of control mode output signal pin
21	SCCS	I/O	Serial I/F pin (chip select)
22	SCSK	I/O	Serial I/F pin(serial clock)
23	SCDI	I/O	Serial I/F pin(data input)
24	SCDO	I/O	Serial I/F pin(data output)
25	DVSS3	—	Internal digital GND 3 for I/O and logic
26	DOA0	O	Digital output(A)
27	DOA1	O	Digital output(A)
28	DOA2	O	Digital output(A)
29	DOA3	O	Digital output(A)
30	DIOA4	I/O	Digital input/output(A)
31	DIOA5	I/O	Digital input/output((A)
32	DIOA6	I/O	Digital input/output((A)
33	DIOA7	I/O	Digital input/output((A)
34	DIOB0	I/O	Digital input/output((B)
35	DIOB1	I/O	Digital input/output((B)
36	DVDD3	—	Internal digital power supply 3 for I/O and logic
37	MCKO	O	Master clock output pin
38	DVSS4	—	Internal digital GND 4 for I/O and logic
39	DIOB2	I/O	Digital input/output((B)
40	DIOB3	I/O	Digital input/output((B)
41	DIOB4	I/O	Digital input/output((B)
42	DIOB5	I/O	Digital input/output((B)
43	DIOB6	I/O	Digital input/output((B)
44	DIOB7	I/O	Digital input/output((B)
45	DIOC0	I/O	Digital input/output((C)
46	DIOC1	I/O	Digital input/output((C)

PIN No.	PIN SYMBOL	I/O	FUNCTION
47	PLSOUT0	O	Sync pulse output pin 0
48	PLSOUT1	O	Sync pulse output pin 1
49	DVDD4	—	Internal digital power supply 4 for I/O and logic
50	RAMIO0	I/O	Frame momory data input/output
51	RAMIO1	I/O	Frame momory data input/output
52	RAMIO2	I/O	Frame momory data input/output
53	RAMIO3	I/O	Frame momory data input/output
54	RAMIO4	I/O	Frame momory data input/output
55	RAMIO5	I/O	Frame momory data input/output
56	RAMIO6	I/O	Frame momory data input/output
57	RAMIO7	I/O	Frame momory data input/output
58	DIF0	I	Test data input(F)
59	DIF1	I	Test data input(F)
60	DIF2	I	Test data input(F)
61	DIF3	I	Test data input(F)
62	DVSS5	—	Internal digital GND 5 for I/O and logic
63	TEIA	I	Test pin(connect DVSS)
64	DVDD5	—	Internal digital power supply 5 for I/O and logic
65	TEIB	I	Test pin(connect DVSS)
66	TEIC	I	Test pin(connect DVSS)
67	TEID	I	Test pin(connect DVSS)
68	DVSS6	—	Internal digital GND 6 for I/O and logic
69	TEOA	O	Test pin(Non-connect)
70	DVDD6	—	Internal digital power supply 6 for I/O and logic
71	DVSS7	—	Internal digital GND 7 for I/O and logic
72	TEOB	O	Test pin(Non-connect)
73	DVDD7	—	Internal digital power supply 7 for I/O and logic
74	TEOC	O	Test pin (Non-connect)
75	DVSS8	—	Intrernal digital GND 8 for I/O and logic
76	TEIE	I	Test pin(connect DVSS)
77	TEOD	O	Test pin(Non-connect)
78	CK2I	I	Clock 2 input pin (for SRAM read)
79	DVDD8	—	Internal digital power supply 8 for I/O and logic
80	OSCI	I	Oscillator inverter inputut pin(Oscillator connecting pin:27MHz)
81	OSCO	O	Oscillator inverter output pin(Oscillator connecting pin:27MHz)
82	DVSS9	—	Internal digital GND 9 for I/O and logic
83	RAMADR0	O	Frame memory address output pin/Digital data output(E)
84	RAMADR1	O	Frame memory address output pin/Digital data output(E)
85	RAMADR2	O	Frame memory address output pin/Digital data output(E)
86	RAMADR3	O	Frame memory address output pin/Digital data output(E)
87	RAMADR4	O	Frame memory address output pin/Digital data output(E)
88	RAMADR5	O	Frame memory address output pin/Digital data output(E)
89	RAMADR6	O	Frame memory address output pin/Digital data output(E)
90	RAMCE	O	Frame memory CE(chip enable) output pin/Digital data output(E)
91	RAMRW	O	Frame memory RW(read/write) output pin/Digital data output(E)
92	RAMOE	O	Frame memory OE(output enable) output pin/Digital data output(E)
93	DVDD9	—	Internal digital power supply 9 for I/O and logic
94	RAMADR7	I/O	Frame memory address output pin/Digital data input/output(G)

PIN No.	PIN SYMBOL	I/O	FUNCTION
95	RAMADR8	I/O	Frame memory address output pin/Digital data input/output((G)
96	RAMADR9	I/O	Frame memory address output pin/Digital data input/output((G)
97	RAMADR10	I/O	Frame memory address output pin/Digital data input/output((G)
98	RAMADR11	I/O	Frame memory address output pin/Digital data input/output((G)
99	RAMADR12	I/O	Frame memory address output pin/Digital data input/output((G)
100	RAMADR13	I/O	Frame memory address output pin/Digital data input/output((G)
101	RAMADR14	I/O	Frame memory address output pin/Digital data input/output((G)
102	RAMADR15	I/O	Frame memory address output pin/Digital data input/output((G)
103	RAMADR16	I/O	Frame memory address output pin/Digital data input/output((G)
104	DVSS10	—	Internal digital GND 10 for I/O and logic
105	DIF4	I	Test data input(F)
106	DIF5	I	Test data input(F)
107	DIF6	I	Test data input(F)
108	DIF7	I	Test data input(F)
109	DIF8	I	Test data input(F)
110	DIF9	I	Test data input(F)
111	DVDD10	—	Internal digital power supply 10 for sensor
112	SCK	O	CMOS sensor clock output pin
113	FSHX	O	External CDS feed-through sampling pulse output pin
114	SSHX	O	External CDS signal sampling pulse output pin
115	ADCK	O	External ADC clock output pin
116	DVSS11	—	Internal digital GND 11 for sensor
117	HP	O	CMOS sensor HP output pin
118	VRR	O	CMOS sensor VRR output pin
119	ESR	O	CMOS sensor ESR output pin
120	UDINV	O	CMOS sensor upside-down setting(connect sensor U/D pin)
121	ADCLPX	O	Pulse output pin
122	LIGCA	O	Pulse output pin
123	STANDBYX	O	Pulse output pin
124	DVDD11	—	Internal digital power supply 11 for sensor
125	PLSOUT2	O	Sync pulse output pin 2
126	PLSOUT3	O	Sync pulse output pin 3
127	PLSOUT4	O	Sync pulse output pin 4
128	AGCD5	O	AGC gain setting pin 5
129	LRSEL	I	Mirror image setteing pin
130	UDSEL	I	Upside-down image setting pin
131	AC5060HZ	I	Comercial freaquency setting for flicker reduction
132	TESTMODE	I	For testing(always set to low)
133	DVSS12	—	Internal digital GND 11 for sensor
134	AVDD3	—	Internal analog power supply 3 for CDS/GCA
135	AGCD4	O	AGC gain setting pin 4
136	AGCD3	O	AGC gain setting pin 3
137	AGCD2	O	AGC gain setting pin 2
138	AGCD1	O	AGC gain setting pin 1
139	AGCD0	O	AGC gain setting pin 0
140	AVDD2	—	Internal analog power supply 2 for CDS/GCA
141	CDSGCAIN	I	Analog input (connect CMOS sensor signal output)
142	AVSS2	—	Internal analg GND 2 for CDS/GCA

PIN No.	PIN SYMBOL	I／O	FUNCTION
143	CLVLIX	O	For FBC(feed-back clamping). Connect 0.47 μ F capacitor between this pin and GND.
144	CLVLI	O	For FBC(feed-back clamping). Connect 0.47 μ F capacitor between this pin and GND.

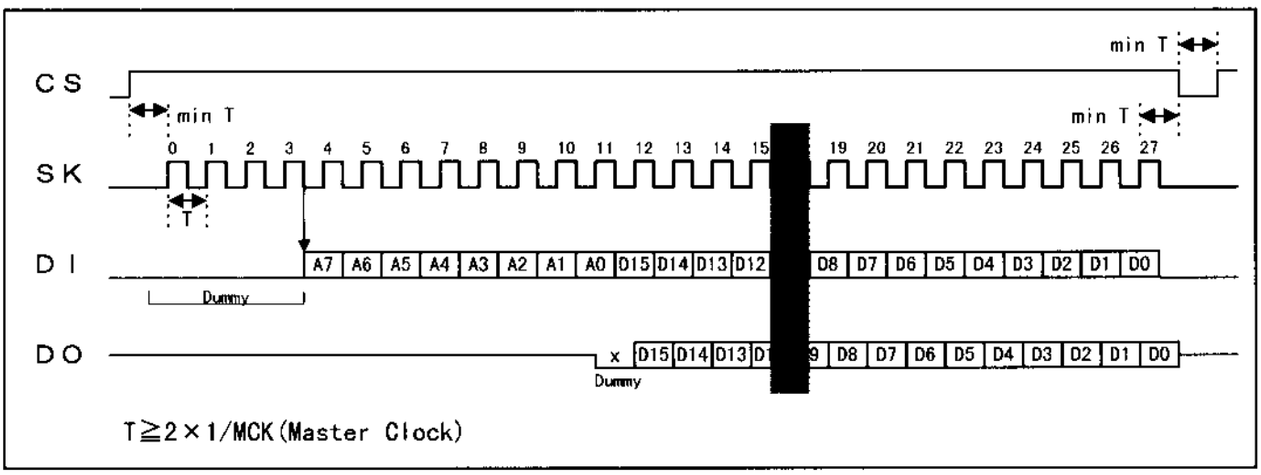
FUNCTIONS SPECIFICATION

Control Mode

TC90A50F is controled by setteing internal resisters. The SCCS,SCSK,SCDI and SCDO(pins 21 to 24) are used for serial interface for setting.
Set PCC/EEPROM=high to select EEPROM automatic read mode,in which the internal settings data can be read once from external EEPROM after a system reset release.

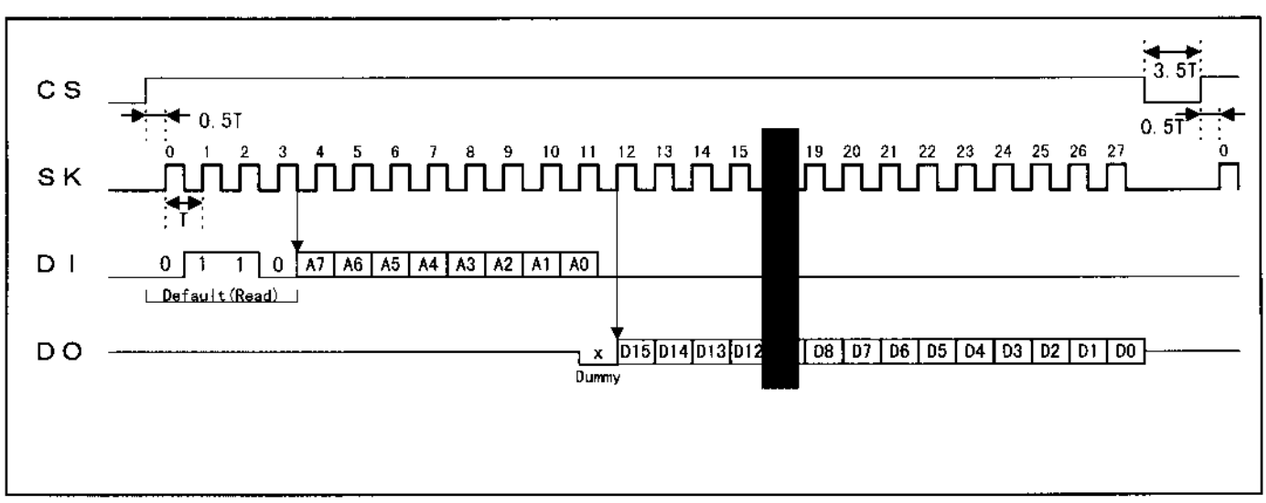
SERIAL I/F SPECIFICATIONS

·Serial Data Input/Output



MCK = 3.375MHz (OSC = 27MHz)

·EEPROM automatic read



T = 1/52.734 kHz (OSC = 27MHz)

CONTENS OF INTERNAL RESISTERS

Operating mode setting (sleep mode,stand-bymode,continue mode,still mode,with/without frame memory)

Intermittent frame mode setting (continue, 1/2 ,1/3,1/5/1/9 intermittent frame)

Electronic shutter speed setting

Flicker of fluorescent lamp reduction mode setting

ALC(Automtic luminounce Level Control) ON/OFF

ALC level setting,area setting

GCA gain setting

Color white balance mode setting (Automatic/Manual)

White balnce gain setting

Chrominance signal adjustment(masking,phase adjustment)

Edge enhance gain setting (Horizontal,Vertical)

Select digital output signal (RGB888,RGB666,YUV422-8,YUV422-16,YUV444)

Color bar signal generator setting

Revesible output (Positive/Negative)

Color/Monochrome switching

RGB pedestal adjustment

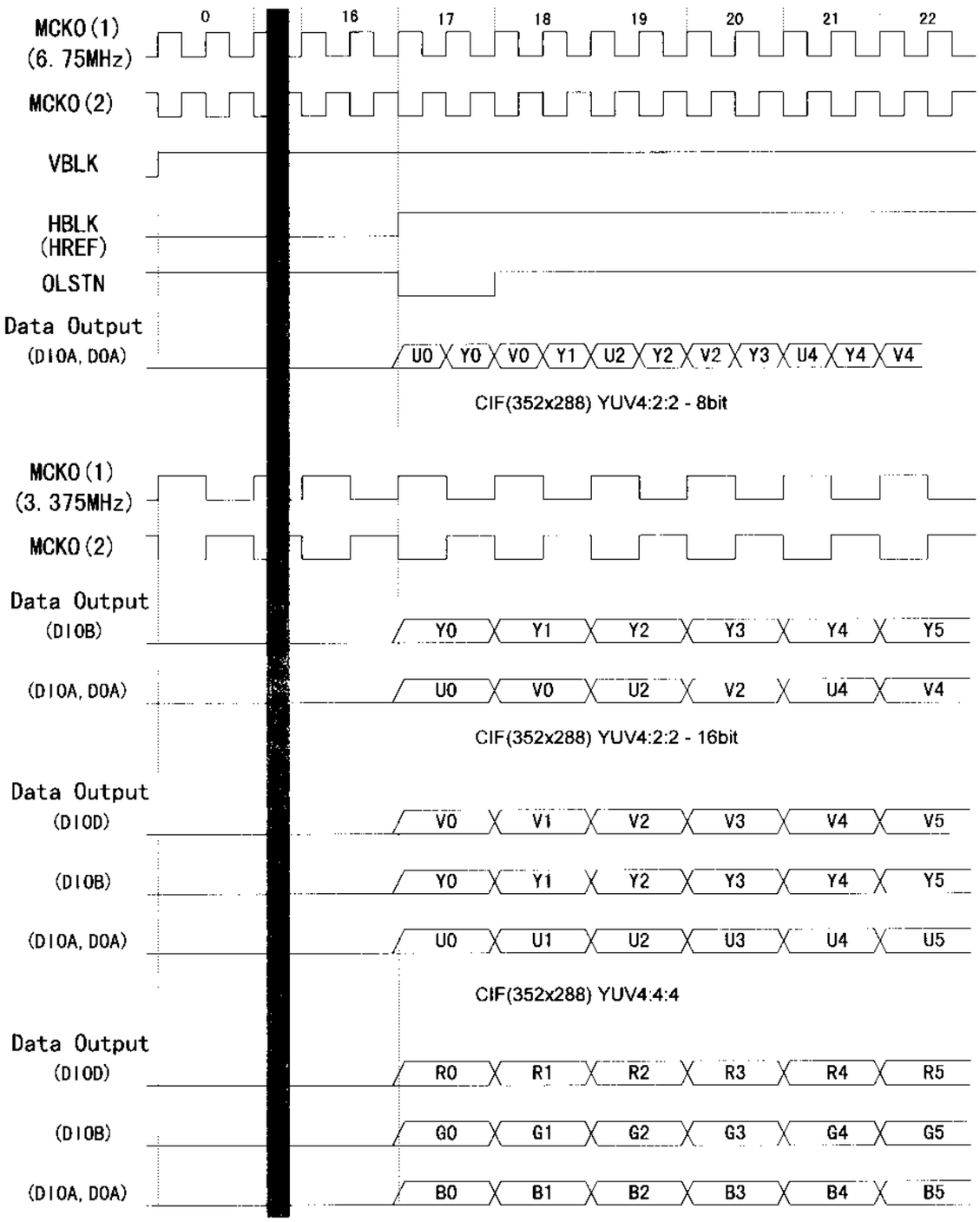
Invert image output setting (Upsidedown,Mirror)

CONTENS OF OUTPUT DATA FOR EXTERNAL CONTROL

Luminaunce data integral value

R-Y/B-Y data integral value

FORMAT OF DIGITAL OUTPUT DATA

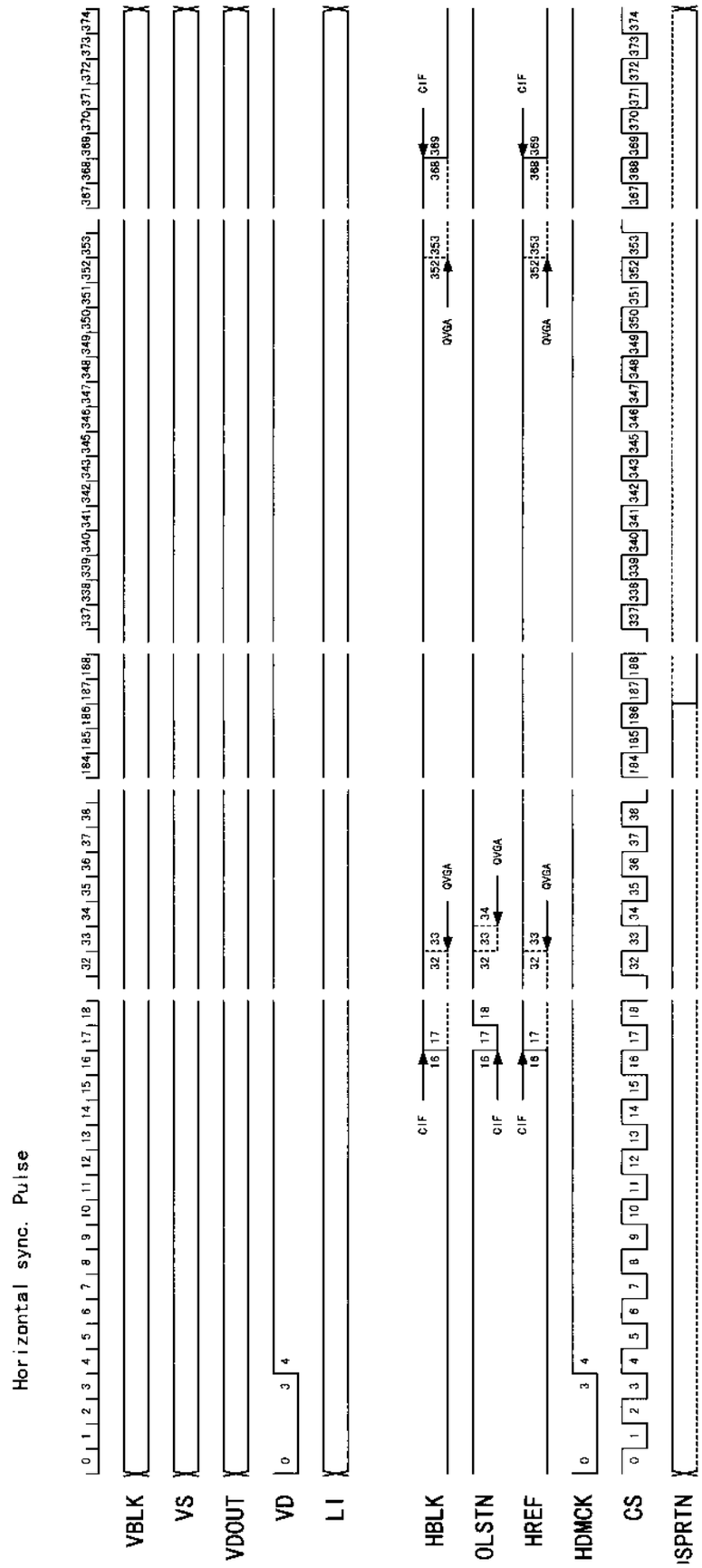


Digital output mode

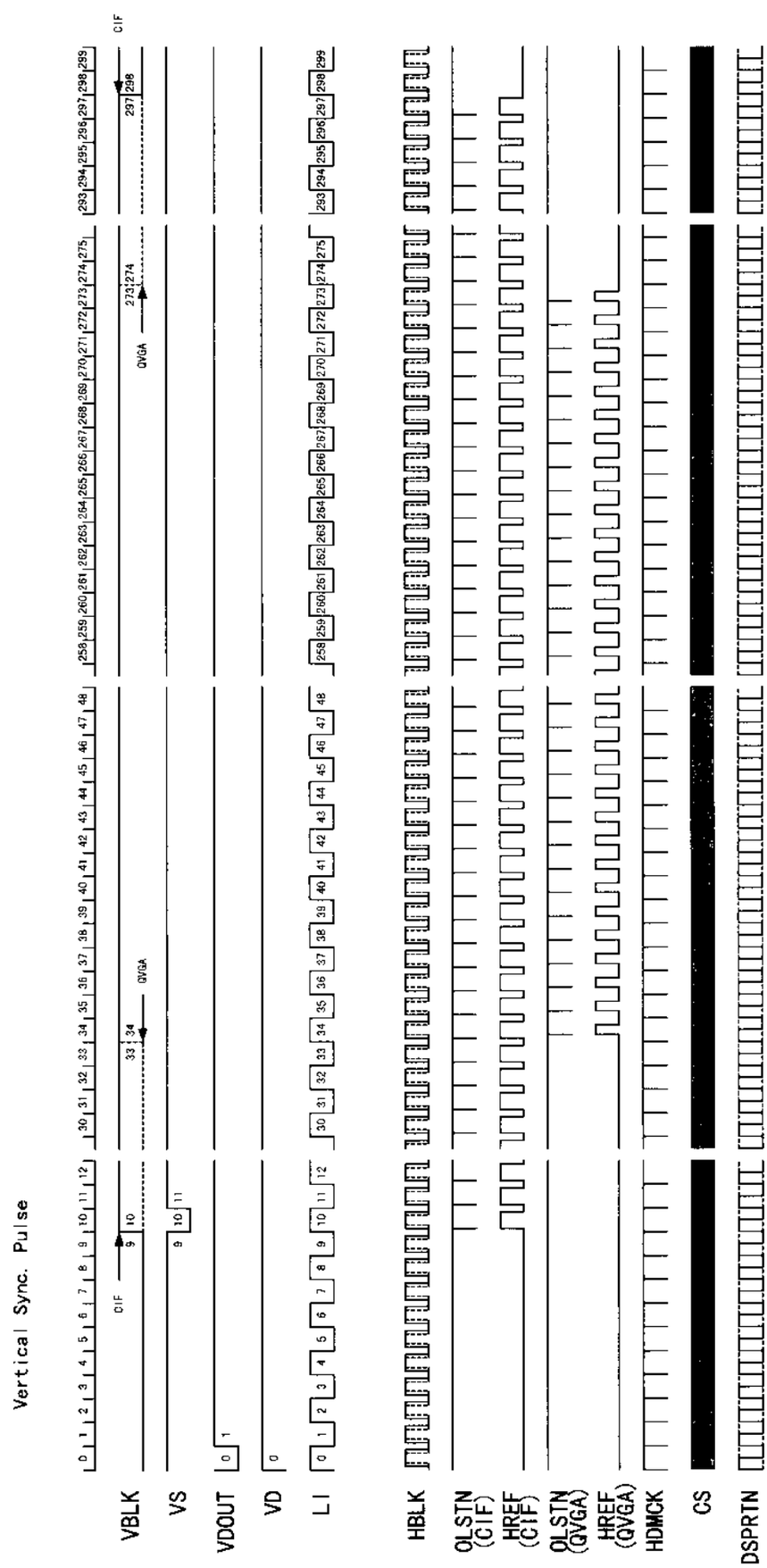
Format	DIOA[7:4]	DOA[3:0]	DIOB[7:0]	DIOD[7:0]	MCKO
YUV422-8	UYVY[7:4]	UYVY[3:0]	-	-	BMCK
YUV422-16	UV[7:4]	UV[3:0]	Y[7:0]	-	MCK
YUV444	U[7:4]	U[3:0]	Y[7:0]	V[7:0]	MCK
RGB666	G[1:0]/B[5:4]	B[3:0]	R[3:0]/G[5:2]	R[5:4] (Note)	MCK
RGB888	B[7:4]	B[3:0]	G[7:0]	R[7:0]	MCK

(Note) R[5:4] is output from DIOC[1:0](pin45,46).

TIMING CHART

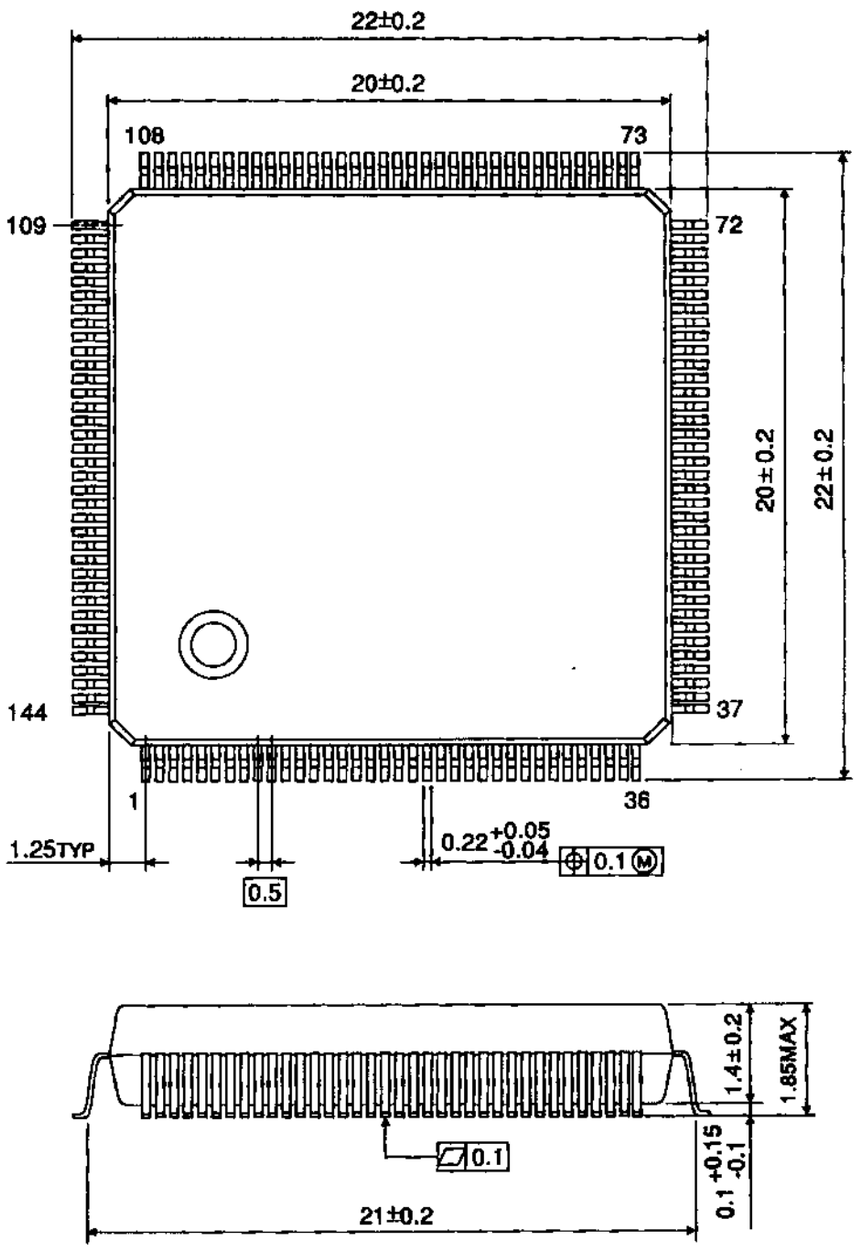


TIMING CHART



OUTLINE DRAWING

LQFP144-P-2020-0.50A Unit : mm



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