RECEIVING SYSTEM

PART 5 - UNIT TECHNICAL INFORMATION

CHAPTER 5 - VLF - LF ADAPTOR TRC1802

PATT NO 0625-18-891884

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CHAPTER 5 - VLF - LF ADAPTOR TRC1802

PATT NO 0625-18-891884

PUPROSE

1. The VLF - LF Adaptor Type TRC1802 is designed to convert the antenna input signal to a fixed frequency, suitable for use with Receiver Type TRC1800. The input frequency range, and reception modes covered by the VLF - LF Adaptor TRC1802 is as follows:

   (a) Range, 10 kHz to 535 kHz.
   (b) Reception modes, A1, A2, F1 and F6.

2. After conversion, the output frequency from the adaptor is 2,5 MHz. This is the same frequency as the 2nd IF of the Receiver Type TRC1800. By means of channelling diodes, the output is applied to the third mixer of the receiver Type TRC1800, in lieu of the 2nd IF from the receiver itself.

IDENTITY

3. VLF - LF Adaptor Type TRC1802 Pattern Number 0625-18-891884. (A general view of the sub-assembly is given in Fig (5)5.1).

SERVICE INFORMATION

4. The VLF - LF Adaptor TRC1802 is designed for use in conjunction with the following sub-assemblies:

   (a) Receiver Type TRC1800.
   (b) Synthesizer Type TRC2111.
   (c) Power Supply Type TRC1801.
   (d) Antenna Pre-selector Type TRC1806.

   Optional sub-assembly to complete the GP Receiver System:

   (e) ISB Adaptor Type TRC1805.

SPECIFICATIONS

5. Frequency range. The overall frequency range of 10kHz - 535kHz is divided into five sub-ranges, as follows:

(a) 10 - 70kHz.
(b) 70 - 150kHz.
(c) 150 - 285kHz.
(d) 285 - 410kHz.
(e) 410 - 535kHz.

6. Attenuation. The input signal can be attenuated by either 0dB, 6dB, 10dB or 20dB, by operation of a control on the front panel.

7. Gain. An input signal of 0,3μV amplitude, will produce an output signal of 2,5MHz at an amplitude not less than 100μV, into 50ohms impedance.

8. Sensitivity. Using an A1 narrow-band signal, of 0,3μV amplitude into 50ohms, the signal plus noise divided by noise ratio, measured over the entire band, will be greater than 10dB.

9. Protection against high induced voltages. The performance of the VLF - LF Adaptor Type TRC 1802, is unimpaired, after being subjected to a direct antenna input signal of 30V rms amplitude into 50ohms.

10. Protection against jamming. For any chosen frequency F, the cross modulation caused by an interfering signal F1, having the following characteristics is not more than 3%.

(i) Within 10kHz of the chosen frequency.
(ii) 30% modulation at 400Hz.
(iii) Amplitude 300mV.

This is measured using A3 mode, and with a broad-band filter fitted to the associated Receiver Type TRC 1800. The Ant. Atten switch on the front panel of the VLF - LF Adaptor must be to the 0dB position.

11. Image frequency rejection. The rejection of the image frequency is greater than 80dB.

12. Selectivity. This is to a large extent dependent upon the associated Receiver Type TRC 1800.

MASS AND DIMENSIONS

13. The VLF - LF Adaptor Type TRC 1802 has the following weight and dimensions:

(a) Weight 6kg (approximately).
(b) Height 250mm.
(c) Width 94mm.
(d) Depth 415mm.

SERVICES REQUIRED

14. The VLF - LF Adaptor Type TRC 1802 is intended for use with the associated power supply sub-assembly Type TRC 1801. This sub-assembly provides the requisite supplies. The sub-assembly TRC 1802, may, however, be operated on a test bench, or in a test jig, provided that the necessary power requirements are met. The supplies required are:

(a) +12V.
(b) +5V.
(c) -12V.

SAFETY PRECAUTIONS

15. No high voltages exist in the unit, however it is always best to observe standard safety precautions, whilst servicing or maintaining electrical equipment.

MANNING REQUIREMENTS

16. The unit can be carried, operated and maintained by one man.

OPERATING INFORMATION

Introduction

17. The VLF - LF Adaptor Type TRC 1802 is normally operated with the other sub-assemblies forming part of the Receiver Type R10 system. Therefore for complete operating instructions, reference should be made to SABR 266(2C).

Front Panel Controls

Fig (5)5.2

18. ANT. ATTEN switch. This switch provides attenuation of the antenna signal by 0, 6, 10 or 20dB. The attenuation level is annotated at the appropriate positions of the switch.

19. Range switch. This switch is used for selection of one of the five sub-ranges within the VLF - LF bands. The ranges themselves are annotated at the appropriate switch positions.

TECHNICAL DESCRIPTION

Introduction

20. The VLF - LF Adaptor TRC 1802 is a plug-in type sub-assembly, which forms part of the Receiver Type R10 system. It receives antenna signals in the VLF and LF bands.

21. The chassis of the TRC 1802 is formed by top and bottom front and rear panels. Two removable side panels, secured by Dzus fasteners, complete the enclosure. The input filter and attenuator assembly is accommodated in the front part of the chassis. The printed circuit boards (PCBs) are located in slides across the remaining part of the chassis. See Fig (5)5.3.

22. The input filters and attenuator circuits are contained on two PCB's which are fitted back-to-back (circuit track innermost) on a small sub-chassis. The attenuator circuits are housed within a metal cover at the top of the right-hand PCB.

23. The ANT. ATTEN switch, S1, is attached to a U-shaped frame, which is secured to the sub-chassis supporting the input filter and attenuator boards. A shaft enables the different switch positions to be selected from the front panel.

24. The range switch, S2 consists of two wafers, one of which directs the input to the appropriate filter, the other wafer selects the output from the same filter. The input wafer is just below switch S1, at the front the sub-chassis supporting the filter and attenuator boards. The output wafer is at the rear of the sub-chassis. A shaft connects the input and output switch wafers to the front panel control knob.

25. PCB's are located in the slides, and mounted vertically across the width of the TRC 1802 chassis. The PCB connectors are located on a fixed side panel. A dowel pin, fitted to the plug end of the PCB, ensures that only the correct PCB engages with the appropriate socket.

26. Removal of the PCB's should be carried out using the extractor tool. This is stowed in a clip located on the top panel.

27. When it is required to test or adjust one of the PCB's, an extension board can be used. This board is stowed between the sub-chassis of the filter and attenuator boards and the PCB's. (See Fig (5)5.3). The PCB is removed from its connector, with the extractor tool provided, and the extension board inserted in its place. The PCB is then inserted into the extension board.

28. The input protection circuit comprises two Zener diodes connected back-to-back and in series. The diodes are located inside a small metal compartment, which is secured to the inner side of the rear panel. Access is gained to the diodes by unscrewing two securing screws and removing a U-shaped cover plate.

29. A block diagram of the five main circuits of the TRC 1802 is shown in Fig (5)5.5. The main circuits are as follows:

(a) Input filters and attenuator boards 26-044080 and 26-044081.
(b) Mixer PCB (A01).
(c) IF PCB (A02).
(d) 7,75MHz oscillator PCB (A03).
(e) Divide by ten PCB (A04).

30. The antenna signal is fed to socket P503, on the rear of the VLF - LF Adaptor (Fig (5)5.4), when TRC 1802 is selected by switch S02 on the front panel of Preselector TRC 1806.

31. From this point it is fed to an antenna protection sub-unit consisting of two Zener diodes. These are connected back to back between the signal line and earth. (See paragraph 28).

ANTENNA PROTECTION SUB-UNIT — Fig (5)5.16

Brief Functional Description — Fig (5)5.3

32. The function of this sub-unit is to afford protection from high induced voltages in the antenna. It limits all input signals to 3V peak to peak.

Detailed Description

33. This is a separate small sub-unit, secured to the inside of the rear panel. It contains two Zener diodes, CR501 and CR502, each having a Zener break-down of 1,5V. If the signal rises positively, to greater than +1,5V, diode CR501 will be forward biased and CR502 reverse biased. If the signal falls below 1,5V, CR501 will be reverse biased and CR502 will be forward biased. The result will be that the signal is limited to the Zener voltage in both directions, ie 3V peak to peak.

INPUT FILTERS AND ATTENUATORS 26-044080 AND 26-044081 — Fig (5)5.7

Brief Functional Description

34. The input filters provide a degree of selectivity, in that each filter passes a small band of frequencies to the attenuators. The attenuators provide 0dB, 6dB, 10dB or 20dB attenuation.

Detailed Description

35. The limited input signals are fed from the protection sub-unit to plug/socket P501/J7, of the input filters and attenuator boards. Choke L46 tends to attenuate the higher frequencies, and the lower frequencies are fed to the range switch S2. This switch has five positions, each one introduces a different band-pass filter, to cover the following ranges:

(a) 10 - 70kHz.
(b) 70 - 150kHz.
(c) 150 - 285kHz.
(d) 285 - 410kHz.
(e) 410 - 535kHz.

36. Except for the values of components, the five band-pass filters are identical and require no explanation. It should be noted however that the band of frequencies passed by the filters centre on approximately 250kHz.

37. Ranges are selected by means of the range switch S2 on the front panel. This switch has two wafers. S2a routes the antenna signals to the appropriate filter. Wafer S2b selects the output from the same filter. The wiper of switch wafer S2b is connected to the wiper of the ANT. ATTEN switch S1.

38. The ANT. ATTEN switch S1 has two wafers. The antenna signals from the filters arrive at the wiper of switch wafer S1a, and are routed either directly to the output wafer S1b, (0dB attenuation), or via one of three resistor pi filters, providing 6dB, 10dB or 20dB attenuation. The output from the wiper of S1b is fed to the output socket J8. Plug P502 and a coaxial cable connect this point to the mixer PCB A01, terminal 10 of J501.

DIVIDE BY 10 PCB A04 — Fig (5)5.9

Brief Functional Description

39. The variable heterodyne frequency from the Synthesizer Type TRC 2111 is fed to the input of the divide by 10 circuit. The actual frequency from the Synthesizer depends upon

the setting of the manual tuning control R09 on the front panel of the Synthesizer, but will be 102,5MHz PLUS ten times the frequency to which the Synthesizer is tuned.

40. The output from the divide by 10 circuit will therefore be 10,25MHz plus the frequency to which the Synthesizer TRC 2111 is tuned.

Detailed Description

41. The variable heterodyne signal from the Synthesizer Type TRC 2111, is fed to the divide by 10 PCB at terminal 2 of connector J502. This frequency will be 102,6 to 107,8MHz in order to cover the complete VLF/LF band.

42. The variable heterodyne frequency is applied to the base of transistor Q401, via R409 and C401. The two transistors, Q401 and Q402 form an amplifying stage to raise the level of the variable heterodyne frequency, to approximately 3V peak to peak, in order to drive the divide by 10 circuit.

43. Decoupling of the +12V supply is provided by C402, C408, R403 and R408. +5V is fed to terminal 5 of connector J502, and after decoupling by C422, C406 and L403, supplies the integrated circuits forming the divider, and additionally is fed to a voltage divider comprising R405 and R406. The voltage developed across R406 (approximately 3V), will be the voltage existing at inputs 6 and 8 of the divide by two IC, Z1, in the absence of a heterodyne input signal. The output of Q402 will drive this voltage between 0 and 3V.

44. Integrated circuits Z2, Z3 and Z4 are connected as a divide by 5 circuit, so that the total division ratio will be 10. The actual frequency to be expected at the output of Z4, test point E403, depends upon the frequency to which the Synthesizer TRC 2111 is tuned, but, providing that the digi-switches on the front panel of the Synthesizer are only used to select between 10 and 530kHz (ie 0 0 1 up to 0 5 3), these frequencies will range from 10,26 to 10,78MHz. The manual tuning control R09 must be at the low frequency end of its range.

45. The output of the divider is fed to the base of transistor Q403, via link E406 and capacitor C407. This transistor and its associated circuitry, shape the final output of the divider. It is then filtered by the parallel tuned circuits L406/C415 and L407/C417/C421. The output is taken from the junction of C417/C421 and routed to the Mixer, PCB A01, via terminal 17 of connector J502.

MIXER PCB A01 Fig (5)5.11

Brief Functional Description

46. The Mixer board comprises four distinct, but inter-related circuits. These are as follows:

(a) The heterodyne amplifier.
(b) The Mixer.
(c) The 10,25MHz ±700Hz filter.
(d) The 10,25MHz amplifier.

47. The heterodyne amplifier is fed with the variable heterodyne from the divide by 10 circuit. The output of this push-pull amplifier provides a balanced input to the Mixer.

48. The Mixer is composed of four JUGFET's, which receive the variable heterodyne frequency on the source electrodes and the antenna signals from the selected filter and attenuator on the gate electrodes. Normal mixing action ensures that the sum and the difference frequencies are available at the output.

49. The 10,25MHz filter has a pass-band of 1 400Hz, ie ±700Hz. It is a quartz crystal filter.

50. The output of the crystal filter is fed to a 10,25MHz amplifier, to compensate for the losses in the filter. AGC from the Receiver Type TRC 1800 is applied to this amplifier.

Detailed Description

51. The heterodyne amplifier. Terminal 17 of connector J501, is connected to terminal 4 of the heterodyne amplifier. The variable heterodyne frequency from the divide

by 10 circuit is fed to this point, and thence to transformer T110. The heterodyne frequency will be induced into the secondary of the transformer, and applied in balanced form, to the bases of transistor Q110 and Q111. These transistors are connected as a push-pull amplifier, R113 providing control of the gain. The balanced output is available at terminals 1 and 2, from the secondary winding of transformer T111.

52. <u>The Mixer</u>. The balanced variable heterodyne input from the heterodyne amplifier, is fed to terminals 3 and 4 of the mixer, and thence to the primary winding of transformer T120. The secondary of this transformer is centre tapped, one half being connected in the source circuit of transistors Q120 and Q121. The other half is connected in the source circuit of transistors Q122 and Q123. This means that the current flow through the transistors will be modified by the heterodyne signal induced into the secondary of T120.

53. The antenna signals from the input filter and attenuator PCB, are fed to terminals 9 and 10, (9 being earthed). From this point the antenna signals are fed to transformer T101, which performs the function of converting the unbalanced input to a balanced one. The output of the transformer T101 is applied to terminals 1 and 2 of the mixer PCB, and thence to the gate electrodes of the mixer JUGFET's Q120 to Q123.

54. The current flow through the mixer transistors is further modified by the antenna signals appearing on the gate electrodes. This is in addition to the effects of the heterodyne frequency being injected into the source electrodes. The sum and difference frequencies will be developed across the secondary of the output transformer T100. This transformer is fed via terminals 5 and 7 of the mixer PCB.

55. The mixer functions in a similar manner to a push-pull amplifier. The heterodyne signal at the source electrodes of A120/Q121, will be in anti-phase to that at the source electrodes of Q122/Q123. The source electrodes which are being driven negatively by the heterodyne signal, will cause the associated pair of transistors, to conduct more heavily than the pair whose source electrodes are being driven positively. At the same time, the antenna signals are driving the gate electrodes of Q120/Q122 in antiphase to the gate electrodes of Q121/Q123. The result is that one transistor of the four will be driven into conduction by both the heterodyne and the antenna signals. As the heterodyne frequency is much higher than the

antenna frequency, it will pass through many complete cycles whilst the antenna frequency completes only one cycle. Suppose therefore that the antenna signal is driving the gate electrodes of Q120/Q122 positively, the heterodyne signal would be causing Q120 to conduct more heavily than Q122 during one half cycle, and then reverse the state during the next half cycle.

56. Transformer T100 is shunted by R100 in order to flatten the response curve, allowing for a reasonably linear response to a signal of 10,25MHz ±750Hz.

57. Filter FL100. Filter FL100 is a quartz crystal filter with a band-pass of 10,25MHz ±750Hz. It is fed with the IF signal from the secondary of transformer T100. Its output is connected to terminal 4 of the 10,25MHz amplifier.

58. 10,25MHz amplifier. Amplification of the IF signal is performed by a MOSFET, Q130. This is followed by an emitter follower, transistor Q131. The IF is fed to the g1 electrode of transistor Q130 via a tuned circuit formed by C136, C137 and L132. AGC originating in the Receiver Type TRC 1800 is applied to the g2 electrode via terminals 4, 3 and resistor R137.

59. R134 and C134 decouple the AGC line. R133 is the source resistor and is decoupled by C133. L131 constitutes the drain load, and the output is taken from the drain electrodes via C132 to the base of Q131. Base bias for this transistor is provided by resistors R131 and R132, the output being developed across R130. The output is then fed via C138, terminal 2 of the 10,25 amplifier and terminal 2 of the Mixer PCB to the intermediate frequency board A02.

7,75MHz OSCILLATOR — Fig (5)5.13

Brief Functional Description

60. The function of this PCB is to produce a stable frequency of 7,75MHz, which can be mixed with the 10,25MHz IF to produce an IF of 2,5MHz. It consists of a quartz crystal oscillator, which is phase locked to the 5MHz master oscillator in the associated frequency Synthesizer.

61. Phase comparison takes place at a frequency of 250kHz. This means that in order to produce 250kHz from the 7,75MHz oscillator frequency, it must be divided by 31. In order to produce 250kHz from the 5MHz supplied by the Synthesizer this latter frequency must be divided by 20.

62. The output from the phase comparator is fed to an integrator, which produces a DC voltage proportional to the phase difference between the two frequencies. This DC voltage is amplified and applied to a varactor in the 7,75MHz oscillator tuned circuit, which corrects the phase accordingly.

<u>Detailed Description</u>

63. Transistor Q301 and crystal Y301 with the associated circuitry including L301 and varactor diode CR301, form an oscillator whose fundamental frequency is 7,75MHz. The output is taken from the collector of Q301, and fed to the base of the emitter follower Q303. From this point the oscillations are fed to terminal 17, and thence to PCB A02.

64. Additionally, the output from the oscillator at the junction of R314 and C306, is fed to the base of the buffer amplifier Q304, via R315 and C307. This buffer supplies a signal of the necessary amplitude to drive the inverter Z307/8. The output from the inverter is fed to each of the clock inputs of the integrated circuits Z301/12, Z301/9, Z302/12, Z302/9 and Z303/9. These five flip-flops comprise a five bit shift register. For convenience of reference in the following description, these are lettered A to E respectively.

65. Z306 is connected as an "exclusive OR" gate. As the inputs to this gate are the Q outputs of flip-flops C and E, it performs the function $\overline{C}E + C\overline{E}$. The output from Z306/11 will therefore be at logic level 0 if these two Q outputs are at level 00 OR 11, and will be at level 1 if they are at level 01 OR 10. The output of Z306/11 is fed direct to the K input of Z301/12, and inverted to the J input of the same flip-flop. Therefore if $\overline{C}E + C\overline{E}$ is presented to the input of the exclusive OR gate, input J of Z301/12 will be at level 0, and input K will be at level 1. Alternatively, if $\overline{C}E + C\overline{E}$ is presented to the inputs of Z306, input J of Z301/12 will be at level 1, and input K will be at level 0.

66. The input to the shift register is therefore decided by the Q outputs C and E in conjunction with the exclusive OR gate Z306. Assuming therefore that all the five flip-flops of the shift register are reset, all the Q outputs will be at level 0, which means that a 1 will be present at input J of Z301/12 and 0 at input K. A clock pulse arriving will clock the 1 at input J through to output Q, and the contents of the shift register will now be 1 0 0 0 0. Because the Q outputs of C and E are still at level 0, input J of Z301/12 will still be at level 1, so that the next clock pulse will clock another 1 into the register, making the contents 1 1 0 0 0. Input J is still at level 1 and thus the third clock pulse will clock a further 1 into the register, making the contents 1 1 1 0 0. The Q outputs C and E are now 1 and 0 respectively, causing input J to change to level 0. The next clock pulse will therefore insert a 0 into the shift register, making the contents 0 1 1 1 0. The following table shows the complete cycle of events.

Table 5.1 — Shift register logic states

Clock Pulse	Inputs J	Inputs K	Outputs C	Outputs E	Contents of register A	B	C	D	E
1	1	0	0	0	0	0	0	0	0
2	1	0	0	0	1	1	0	0	0
3	1	0	0	0	1	1	1	0	0
4	0	1	1	0	0	1	1	1	0
5	0	1	1	0	0	0	1	1	1
6	0	0	1	1	1	0	0	1	1
7	0	1	0	1	0	1	0	0	1
8	0	1	0	1	0	0	1	0	0
9	0	1	1	0	0	0	0	1	0
10	1	0	0	0	1	0	0	0	1
11	0	1	0	1	0	1	0	0	0
12	1	0	0	0	1	0	1	0	0
13	0	1	1	0	0	1	0	1	0
14	1	0	0	0	1	0	1	0	1
15	1	0	1	1	1	1	0	1	0
16	1	0	0	0	1	1	1	0	1
17	1	0	1	1	1	1	1	1	0
18	0	1	1	0	0	1	1	1	1
19	1	0	1	1	1	0	1	1	1
20	1	0	1	1	1	1	0	1	1
21	0	1	0	1	0	1	1	0	1
22	1	0	1	1	1	0	1	1	0
23	0	1	1	0	0	1	0	1	1
24	0	1	0	1	0	0	1	0	1
25	1	0	1	1	1	0	0	1	0
26	1	0	0	0	1	1	0	0	1
27	0	1	0	1	0	1	1	0	0
28	0	1	1	0	0	0	1	1	0
29	0	1	1	0	0	0	0	1	1
30	0	1	0	1	0	0	0	0	1
31	0	1	0	1	0	0	0	0	0

The cycle of events will then be repeated. The shift register and the exclusive OR gate therefore act as a divider by 31.

67. The state 0 0 0 0 0 of the Q outputs corresponds to 1 1 1 1 1 state of the $\overline{Q}$ outputs. These latter outputs enable Z305 whose output will therefore be level 0 pulses at a repetition frequency of 250kHz.

68. Z312 is the resetting device, but is only included in case the Q outputs ever get to the state 1 1 1 1 1, such as at the instant of switching on. If Z312 were not present and the Q outputs were at 1 1 1 1 1, this state would never change, as a 1 would always be present at the J input of Z301/12.

69. 5MHz from the Synthesizer Type TRC 2111 is supplied to terminal 2, and thence to the driving amplifier comprising transistors Q305 and Q306. The output from the amplifier is fed via C325 to the clock input of Z304. It is clamped above earth by the diode CR302. Z304 and Z303/12 divide the 5MHz input by 20. The input to Z311 is therefore 250kHz.

70. The circuits formed by Z307/3, Z307/6, R326, C312 and Z311/3, Z311/6, R327, C313 are identical differentiating circuits, producing very short duration square pulses of 250kHz. The output of each of these circuits is applied to the phase comparator consisting of Z311/8 and Z311/11. The output from the latter gate will be 250kHz square waves, whose width will be proportional to the phase difference between the oscillator and the reference frequency.

71. The output from Z311/11 is applied to an integrating circuit, composed of R313 and C304. The DC voltage thus produced is proportional to the phase difference, and is applied to the base of the DC amplifier Q302. The output from the collector of Q302 is applied to the varactor CR301 via the inductances L302 and L301.

72. L301 and CR301 form a variable reactance, which can be capacitive or inductive, depending upon the control voltage delivered to the varactor. This allows control of the tuning of the crystal around its nominal frequency by approximately 1kHz. This amount of control is sufficient to ensure that the crystal oscillator is slaved to the master oscillator.

INTERMEDIATE FREQUENCY BOARD PCB A02 — Fig (5)5.15

Brief Functional Description

73. This PCB receives the IF of 10,25MHz from the mixer, and 7,75MHz from the crystal oscillator. These two frequencies are mixed, to produce a difference frequency of 2,5MHz, which is then fed to the Receiver Type TRC 1800.

74. A separate circuit on the same board, is supplied with the AGC voltage obtained from the associated Receiver Type TRC 1800. The AGC voltage is amplified and inverted and then applied to the 10,25MHz amplifier in PCB A01.

Detailed Description

75. The IF input of 10,25MHz is received from PCB A01 connector J501/2, at terminal 2 of connector J503. From this point it is applied to the emitter of Q201 via C215 and R224. The amplified IF signal at the collector of Q201, is coupled to the g2 electrode of the field effect transistor Q202.

76. The 7,75MHz input from the crystal oscillator, is fed to terminal 10 of connector J503, and thence via R226 and C216, to the g1 electrode of Q202. This input is filtered by the paralled tuned circuit L204/C217. Both the IF and the oscillator frequencies modulate the current flow through the FET. The output will therefore contain the sum and difference frequencies. The drain load of Q202 is tuned to the difference frequency of 2,5MHz, and thus the other frequencies present will be drastically attenuated. The output of Q202 is further filtered by a parallel tuned circuit, whose resonant frequency is 2,5MHz, ie L203, C226 and C228.

77. The amplitude of the 2,5MHz IF is adjusted by R236. It is then applied to the base of the emitter follower Q203. The output is fed via connector J503 terminal 17 and connector P504 terminal A7 to the Receiver Type TRC 1800. See the interconnecting diagram Fig (5)5.16.

78. The AGC voltage from the associated Receiver Type TRC 1800, is applied to terminal 4 of connector P504. From this point it is fed via terminal 5 of connector J503 and R207, to the inverting input of the operational amplifier Z201.

79. The threshold level for the AGC is set by R215. The inverted output is taken from Z201 pin 6, and fed via R202, R201 and terminal 4 of connector J503, to terminal 4 of connector J501. The Zener diode CR201 in conjunction with diode CR202 limits the AGC output of the operational amplifier to a maximum of +6V.

TEST INFORMATION

80. Test equipment. The test equipment required is listed in Table 5.2:

Table 5.2 — Test Equipment

Item	Qty	CRETE	Manufacturer
Multimeter	1	CT471	Avo Model 8
Oscilloscope	1	CT536A	Tektronix 545A
RF voltmeter	1		
Signal generator (VLF to HF)	1		

81. DC voltage measurements. To carry out voltage measurements, the VLF - LF Adaptor TRC 1802 should be removed from the rack assembly (see paragraph 92), and either installed in a test rig, or the necessary extension leads used to connect the TRC 1802 to the rack assembly supply.

82. Switch on the power supply to the TRC 1802 under test. Using the multimeter, carry out the following voltage measurements. Unless otherwise stated, voltages are always measured with respect to earth.

Table 5.3 — DC Voltages

Connector	Pin			
	4	7	9	11
P504	+2V	+5V	+12V	-12V

Note — The voltage on pin 4 is measured with the Receiver TRC 1800 RF gain control at maximum gain.

83. Mixer PCB A01 Voltage checks. Before making the voltage measurements listed in Table 5.4, the following conditions must be met:

(1) Remove the plug from socket P503 on the rear panel. ie no signal condition.

(2) Remove the oscillator board A03.

(3) Remove the divide by ten board A04.

(4) Remove the mixer board A01.

(5) Remove the individual screening covers from the mixer, the heterodyne amplifier, and the 10,25MHz amplifier.

(6) Insert the extension board into connector J501.

(7) Insert PCB A01 into the extension board connector, taking care that the locating pin is on the same side as the locating hole.

Table 5.4 DC Voltages Mixer PCB A01

Transistor	Base/Gate	Collector/Drain	Emitter/Source
Q110	+0,65V	+11,4V	0V
Q111	+0,65V	+11,4V	0V
Q120	0V	+11,4V	+1,42V
Q121	0V	+11,4V	+1,42V
Q122	0V	+11,4V	+1,42V
Q123	0V	+11,4V	+1,42V
Q130	g1 +2,1V	+11,5V	+5,7V
	g2 +5,7V		
Q131	+6,0V	+11,5V	+5,7V

84. IF PCB A02 Voltage checks. Before making the voltage measurements listed in Table 5.5 and Table 5.6, the following conditions must be met:

(1) Perform tasks laid down in paragraph 83 (1), (2) and (3).

(2) Remove the intermediate frequency PCB A02.

(3) Remove the screening cover from PCB A02.

(4) Insert the extension board into connector J503.

(5) Insert the intermediate frequency PCB A01 into the connector of the extension board.

Table 5.5 — DC Voltages IF PCB A02

Transistor	Base/Gate	Collector/Drain	Emitter/Source
Q201	+5,6V	+11,2V	+4,95V
Q202	g1 0V	+11,5V	+0,56V
	g2+0,56V		
Q203	+5,5V	+9,5V	+4,85V

Table 5.6 — DC Voltages AGC amplifier

Pin	1	2	3	4	5	6	7	8
Z201	+8,2V	+1,96V	+2,0V	-11,7V	-11,7V	+10,8V	+11,6V	+7,8V

85. 7,75MHz oscillator PCB A03 Voltage checks. Before performing the voltage checks listed in Table 5.7, the following conditions must be met:

(1) Remove PCB A03.
(2) Insert the extension board into connector J504.
(3) Remove top and bottom screening covers from PCB A03.
(4) Insert PCB A03 into the connector of the extension board.
(5) Apply a 5MHz signal to connector P504 pin A3.

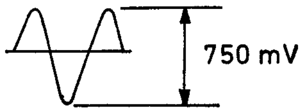
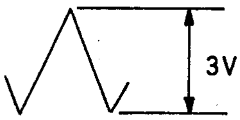
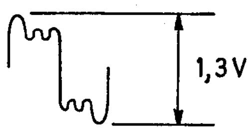
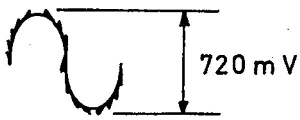
Table 5.7		DC Voltages 7,75MHz oscillator	
Transistor	Base	Collector	Emitter
Q301	+3,4V	+6,0V	+2,9V
Q302	+10,95V	+4,3V	+0,36V
Q303	+4,9V	+11,2V	+4,6V
Q304	+3,6V	+7,8V	+3,8V
Q305	+3,7V	+8,8V	+3,1V
Q306	+3,7V	+8,1V	+3,6V
Z312/8	+3,0V		

86. Divide by 10 PCB A04 Voltage checks. Before performing the voltage checks listed in Table 5.8, the following conditions must be met:

(1) Remove PCB A04.
(2) Remove screening cover from PCB A04.
(3) Insert the extension board into connector J502.
(4) Insert PCB A04 into the connector of the extension board.
(5) Inject 100MHz into pin A3 of connector P504.

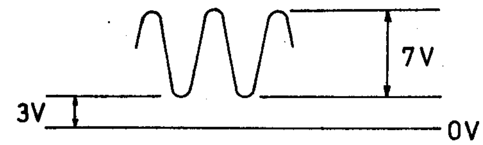
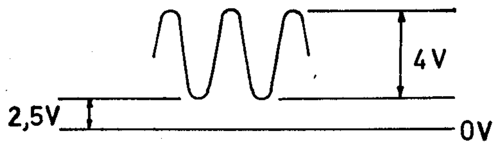
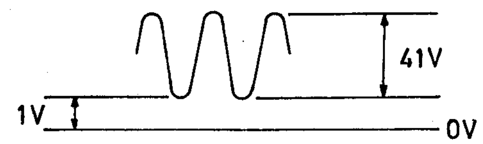
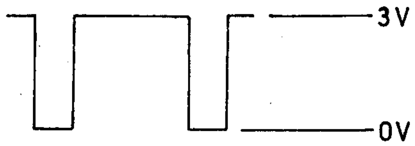
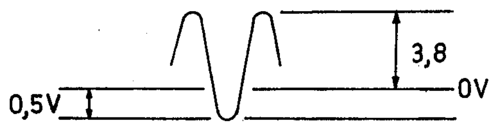
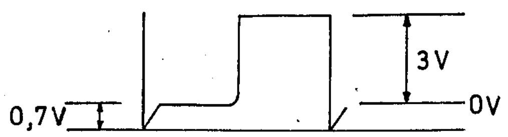
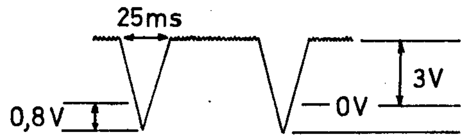
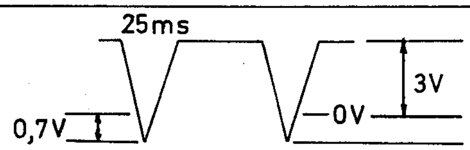
Table 5.8		DC Voltages Divider by 10 PCB A04	
Transistor	Base	Collector	Emitter
Q401	+0,78V	+2,8V	0V
Q402	+2,8V	+8,5V	+2,1V
Q403	+2,3V	+4,8V	+1,6V

87. AC voltage measurements. The oscillograms listed in the following tables, should be displayed on an appropriate oscilloscope, in the sequence given in the tables.

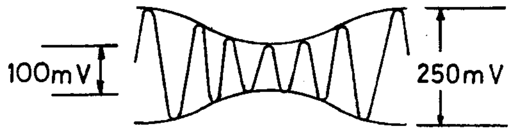
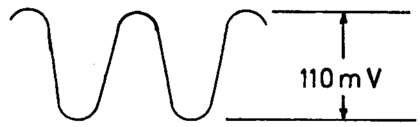
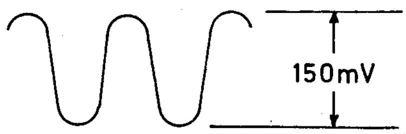
Table 5.9		AC waveforms Divider by 10 PCB A04
Test point	Frequency	Oscillogram
E401	102,6 - 107,8MHz	
E402	51,3 - 53,9MHz	
E404	10,26 - 10,78MHz	
E407	10,26 - 10,78MHz	
E405	10,26 - 10,78MHz	

88. 7,75MHz oscillator PCB A03.

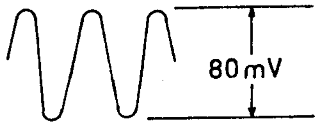
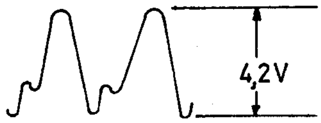
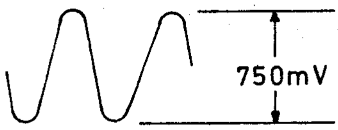
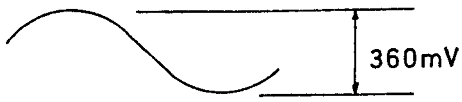
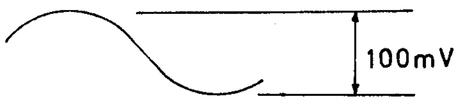
Table 5.10 — **AC waveforms 7,75 oscillator**

Test point	Frequency	Oscillograms
Q301 base	7,75MHz	
Q301 collector	7,75MHz	
E302	7,75MHz	
E303	7,75MHz	
E305	250kHz	
E307	5MHz	
E306	250kHz	
E304	250kHz	
Z311/6	250kHz	

89. Mixer PCB A01.

Table 5.11		AC waveforms Mixer
Test point	Frequency	Oscillograms
Filter FL100 input		
Filter FL100 output	10,25MHz	
Terminal 2	10,25MHz	

90. Intermediate frequency PCB A02 AC waveforms.

Table 5.12		AC waveforms IF
Test point	Frequency	Oscillograms
E203	10,25MHz	
Terminal 10	7,75MHz	
E204	7,75MHz	
E205	2,5MHz	
E206	2,5MHz	
E207	2,5MHz	

MAINTENANCE INFORMATION

Removal and Replacement Procedures

91. TRC 1802 Removal. To remove the VLF - LF Adaptor TRC 1802 from the rack assembly, for test or maintenance purposes, the following procedures should be adopted:

(1) Switch off the associated power supply type TRC 1801.

(2) Unscrew the three captive screws which secure the TRC 1802 to the rack assembly.

(3) Grip the flange surrounding the front panel, and ease the sub-assembly forward approximately 2cm, in order to disengage the rear plugs.

(4) Remove the sub-assembly by pulling forward with one hand whilst supporting it underneath with the other hand.

92. TRC 1802 Replacement. To replace the TRC 1802 in the rack assembly, the following procedure should be adopted:

(1) Ensure that the associated power supply TRC 1801 is switched off.

(2) Check that the guide pins at the rear of the sub-assembly are not bent or broken.

(3) Ensure that the connector P504 is slightly loose in its mounting, on the rear panel.

(4) Insert the replacement sub-assembly, rear first into the appropriate slides on the rack assembly. Ease the sub-assembly carefully forward, until the plug and socket are correctly mated.

(5) Tighten the three captive screws securing the TRC 1802 to the rack assembly frame.

93. Attenuator and filter board removal and replacement. The attenuators and filters, are assembled on two PCB's, positioned back to back at the front of the sub-assembly TRC 1802. The PCB on the right hand side contains the attenuators, and the removal of this PCB will be described. The removal of the other PCB is similar, but entails the unsoldering of 6 connecting leads only.

94. Removal. Having previously removed the complete sub-assembly TRC 1802, as described in Paragraph 92, proceed as follows:

(1) Remove the two side covers. The right hand one is secured by three Dzus fasteners, the left hand one by two Dzus fasteners.

(2) Lay the sub-assembly TRC 1802 on the work bench, with the right side uppermost.

(3) Locate the cover over the attenuators. Fig (5)5.3.

(4) Remove the two screws securing the cover, and remove the cover.

(5) Unsolder the 6 white connecting leads disclosed.

(6) Unsolder the other four white connecting leads to the PCB.

(7) Remove the six screws securing the PCB to the chassis.

(8) Carefully lift out the PCB.

95. Replacement. A replacement PCB can be fitted by reversing the tasks listed in paragraph 95.

96. Boards A02, A03 and A04 should be removed with the special tool provided for this purpose. Board A01 has no holes to accommodate the special tool, and should therefore be extracted carefully by pulling on the covers of mixer and the filter.

Setting-up Procedures

97. AGC amplifier. This adjustment entails the setting-up of the threshold level of the AGC voltage. It depends upon the requisite level of AGC being available from the Receiver Type TRC 1800, or alternatively that the requisite DC levels can be obtained from a variable DC power supply, injected at the appropriate input terminal. (P504/4).

98. Proceed as follows:

(1) Remove the right hand side cover, (3 dzus fasteners).

(2) Using the special tool provided, remove PCB A02.

(3) Remove the four screws securing the cover, and remove the cover.

(4) Insert the extension board into connector J503.

(5) Insert PCB A02 into the connnector of the extension board.

(6) Connect the multimeter between test point E201 and earth.

(7) Adjust the RF gain control on the Receiver Type TRC 1800 to obtain a reading of +0.9V on the multimeter.

(8) Connect the multimeter between test point E202 and earth.

(9) Adjust R215 to obtain a reading of -1,5V on the multimeter.

(10) Connect the multimeter between test point E201 and earth.

(11) Adjust the RF gain control on the Receiver Type TRC 1800 until the multimeter reads +2,0V.

(12) Connect the multimeter between test point E202 and earth.

(13) Check that the multimeter reads between +5,8V and +6,0V.

99. <u>Divide by 10 PCB A04</u>. The only adjustment to be made to this PCB, is to the output filter, which should be set up in the following manner:

(1) Remove the link E406.

(2) Connect the output of a swept-frequency generator to point E404. The frequency must be swept between 10,2 and 10,8MHz.

(3) Connect an oscilloscope via a 0,5pf capacitor, to test point E407.

(4) Connect test point E410 to earth.

(5) Adjust L405 until the response curve peaks at 10,25MHz.

(6) Remove the earth from test point E410.

(7) Connect test point E412 to earth.

(8) Adjust L406 to obtain a trough on the response curve at 10,25MHz.

(9) Remove the earth from test point E412.

(10) Adjust L407 to obtain a maximum on the response curve at 10,25MHz.

(11) Disconnect the oscilloscope from test point E407, and connect it to test point E405.

(12) Check that the response curve is reasonably square, between the limits of 10,2 to 10,8MHz.

(13) Replace the link E406.

100. <u>7,75MHz oscillator PCB A03</u>. The only check to be performed on this PCB is that the oscillator is phase locked to the master oscillator in the Synthesizer Type TRC 2111. In order to perform this check, proceed as follows:

(1) Connect the oscilloscope to test point E302.

(2) Connect the frequency counter to test point E302.

(3) Connect the VTVM, set to approximately 12V DC, between test point E301 to earth.

(4) Inject a frequency of 5MHz at terminal P504/2, using the signal generator.

(5) Vary the frequency injected at terminal P504/2, a few hundred Hz either side of 5MHz. There should be a slight shift of the differentiated phase comparator pipe displayed on the oscilloscope.

(6) Ascertain the limit of movement in each direction.

(7) Record, for each direction limit:

(a) The frequency of the oscillator, as read on the frequency counter.

(b) The level of the DC tuning voltage, as read on the VTVM.

101. It should be found that the oscillator frequency varies above and below 7,75MHz by approximately 1 200Hz and 700Hz respectively.

102. <u>Intermediate frequency PCB A02</u>. Having ascertained that 7,75MHz is available at terminal J503/10, the inductors may be tuned as follows:

(1) Connect a 50ohms resistor between test point E207 and earth.

(2) Connect the oscilloscope to test point E207.

(3) Adjust the swept-frequency generator to sweep between the frequencies 10,23 - 10,27MHz (ie 10,25MHz $\pm$20kHz).

(4) Inject the output of the swept frequency generator at terminal J503/2.

(5) Adjust L201 and L204 to obtain the maximum output level.

(6) Adjust L202 and L203 to obtain a flat response curve, centred on 2,5MHz. The bandwidth should be 23kHz, measured between the 3dB points.

103. Gain adjustment. The gain is adjusted by means of R236. It should be adjusted with reference to the 10,25MHz input from the mixer PCB A01. The maximum gain from the 10,25MHz input to the 2,5MHz output is 32dB ±2dB.

104. Mixer PCB A01.

(a) Heterodyne amplifier adjustments. Proceed as follows:

(1) Select 250kHz on the associated Synthesizer Type TRC 2111.

(2) Connect the RF voltmeter to test point E120.

(3) Adjust T110 and T111 to obtain maximum reading on the voltmeter.

(4) Finally, adjust R113 until a reading of between 1,75V and 1,8V is obtained.

(b) Crystal filter checking. Proceed as follows:

(1) Set R121 and R122 of the mixer to mid-travel.

(2) Select 250kHz on the associated Synthesizer Type TRC 2111.

(3) Select the sub-band 150 - 285kHz, by means of the range switch S2, on the front panel of the LF - VLF Adaptor Type TRC 1802.

(4) Adjust the swept-frequency generator to sweep between 249 and 251kHz.

(5) Inject the output of the swept-frequency generator at socket P503.

(6) Connect the oscilloscope to P504/A7.

(7) Connect a 50ohm resistor between P504/A7 and earth.

(8) Observe the response curve on the oscilloscope, and adjust T100 and L132 to obtain minimum ripple over the entire pass-band.

105. Gain adjustment. For this adjustment, the output of the intermediate amplifier is observed. Proceed as follows:

(1) Inject a frequency of 250kHz, amplitude 1µV, at the antenna input socket of the Antenna Preselector Type TRC 1806.

(2) Connect the oscilloscope to P504/A7.

(3) Connect a 50ohm resistor between P504/A7 and earth.

(4) Adjust R236 in the intermediate frequency PCB A02, to obtain an amplitude of 300µV ±1dB.

NOTE It is preferable to use a selective voltmeter instead of the oscilloscope in (2). The readings obtained in this manner will not then be affected by any remaining and interfering heterodyne frequencies.

106. Balancing the mixer. This adjustment is conducted in conjunction with the associated Receiver Type TRC 1800. The procecure adopted should be as follows:

(1) Select 10kHz on the associated Synthesizer Type TRC 2111.

(2) Disconnect the antenna input at the Antenna Preselector Type TRC 1806.

(3) Connect the VTVM to the AF line. The reading obtained will be due to noise only.

(4) Re-adjust the resistors R121 and R122 which were set to mid-travel, until minimum reading is obtained.

(5) Check the signal to noise ratio, by injecting an antenna signal of ±90kHz. The results obtained should approximate: S + N/N is not less than 10dB for an input signal of 0,3µV.

107. Input filters adjustment. Adjustment of the input filters should not be attempted, unless a fault has occurred which entails replacing a component.

108. A rapid check of the input filters may be performed in the following manner:

(1) Set the attenuator switch S1 to 0dB.

(2) Select the desired sub-band, by means of switch S2 on the front panel.

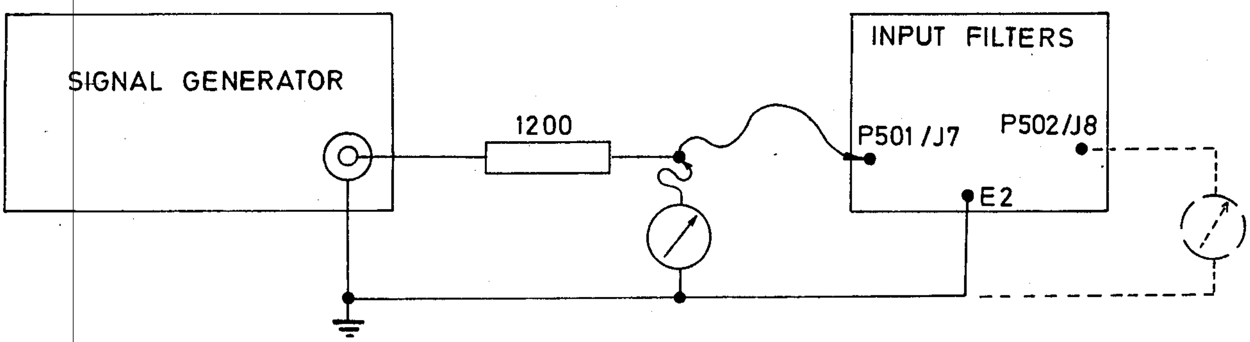
(3) Apply the output of the swept-frequency generator, (adjusted to sweep through the sub-band selected in (2)), to the antenna input terminal of the Preselector Type TRC 1806.

(4) Connect the oscilloscope to P504/A7 on the LF - VLF Adaptor Type TRC 1802.

(5) Observe the response curve on the oscilloscope. The ripple over the entire sub-band should be less than 1dB.

109. If circumstances necessitate re-aligning the input filters, the following procedure should be adopted:

(1) Connect the signal generator as shown in the sketch below. The instrument must be capable of delivering frequencies from 10 to 535kHz.



(2) Select the 10 - 70kHz range, by means of the range switch S2.

(3) Earth test point E2.

(4) Adjust the signal generator to 26,5kHz.

(5) Tune L2 for minimum reading on the voltmeter.

(6) Disconnect the signal generator from the input socket P501/J7.

(7) Connect the signal generator to the output socket P502/J8.

(8) Tune L4 for minimum reading on the voltmeter.

(9) Disconnect the signal generator from the output socket P502/J8.

(10) Reconnect the signal generator to the input socket P501/J7.

(11) Connect the voltmeter to the output socket P502/J8.

(12) Remove the earth from test point E2.

(13) Tune L3 to obtain maximum reading on the voltmeter.

(14) Do not adjust L1 and L5 as these are set up in the factory to their nominal value.

110. <u>70 - 150kHz filter adjustment</u>. The adjustment of this filter is, in the first instance, the same as the 10 - 70kHz filter already described. The only difference is the frequency to be injected, and the inductors to be tuned.

(1) As for paragraph 104 (1).

(2) Select the 70 - 150kHz range by means of the range switch S2.

(3) Earth test point E12.

(4) Adjust the signal generator to 103kHz.

(5) Tune L12 for minimum reading on the voltmeter.

(6) Proceed as for paragraph 104 steps (6) to (13), but adjusting L14 for step (8), and L13 in step (13).

(7) Earth test point E11. This connects L11 and L12 in parallel.

(8) Adjust the signal generator to 122kHz. (The corrected frequency allows for the fact that L11 and L12 have been connected in parallel).

(9) Tune L11 for maximum reading on the voltmeter.

(10) Disconnect the signal generator from the input socket P501/J7.

(11) Reconnect the signal generator to the output socket P502/J8.

(12) Earth test point E13.

(13) Tune L15 for maximum reading on the voltmeter.

(14) Remove the earth from test point E13.

(15) Disconnect the signal generator from the output socket P502/J8, and reconnect it to the input socket P501/J7.

(16) Adjust the signal generator to 103kHz.

(17) Connect the voltmeter between P502/J8 and earth.

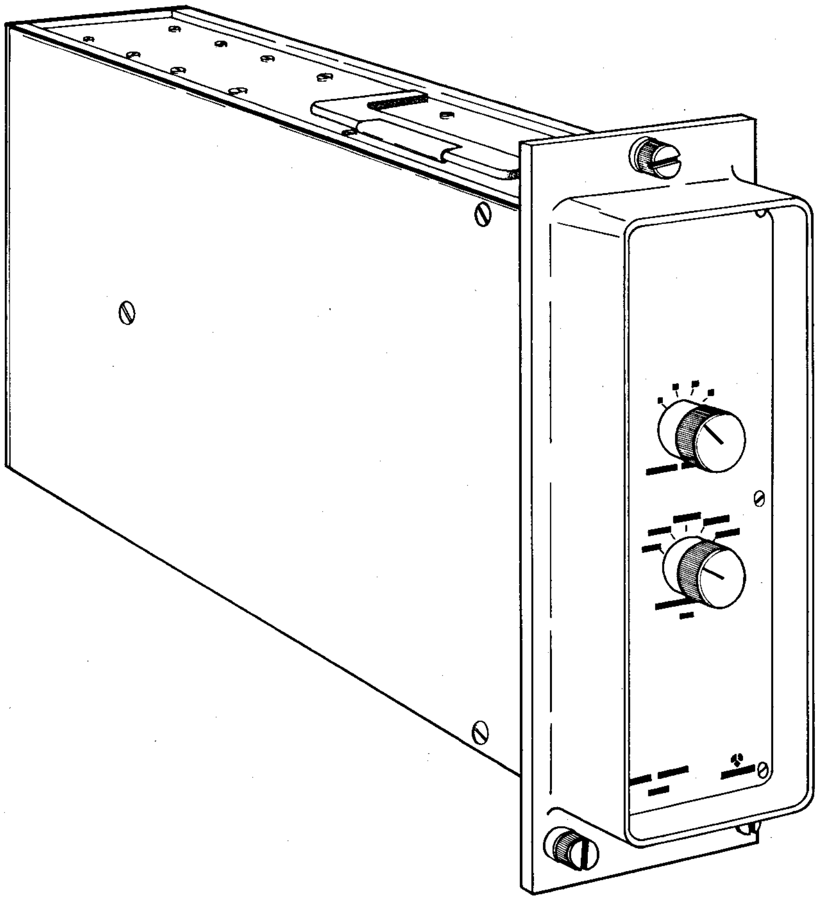
(18) Tune L13 for maximum reading on the voltmeter.

111. Adjustment of the other filters is performed in a similar manner to that described in paragraph 105. The differences being the frequencies injected, the test points earthed, and the inductors adjusted. These differences are listed in Table 5.12.

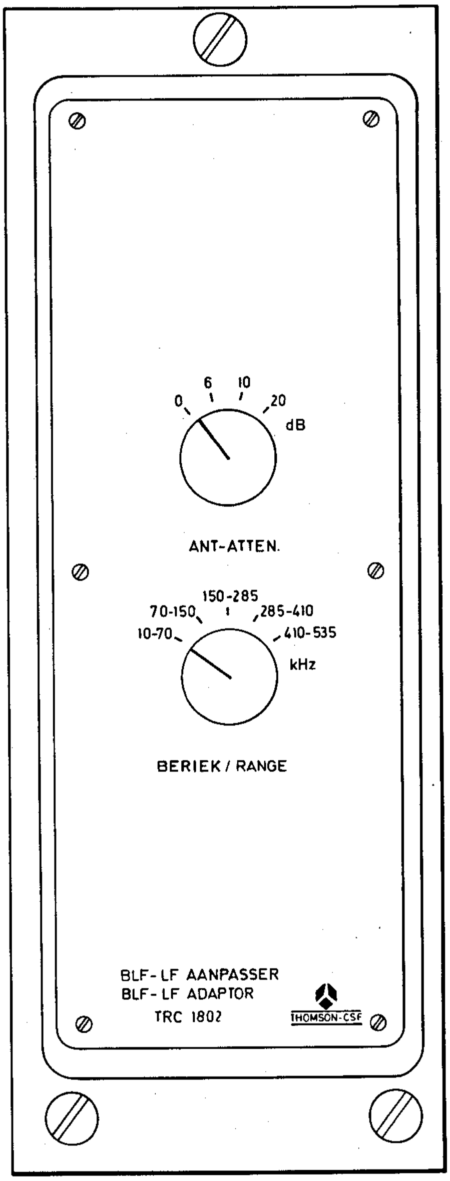
Table 5.12 — Adjustment of filters

Filter	Frequency	Test point	Inductor
150 - 285kHz	207kHz	E22	L22 and L24
150 - 285kHz	234kHz	E21/E23	L21 and L25
150 - 285kHz	207kHz	None	L23
285 - 410kHz	342kHz	E32	L32 and L34
285 - 410kHz	357kHz	E31/E33	L31 and L35
285 - 410kHz	342kHz	None	L33
410 - 535kHz	468kHz	E42	L42 and L44
410 - 535kHz	480kHz	E41/E43	L41 and L45
410 - 535kHz	468kHz	None	L43

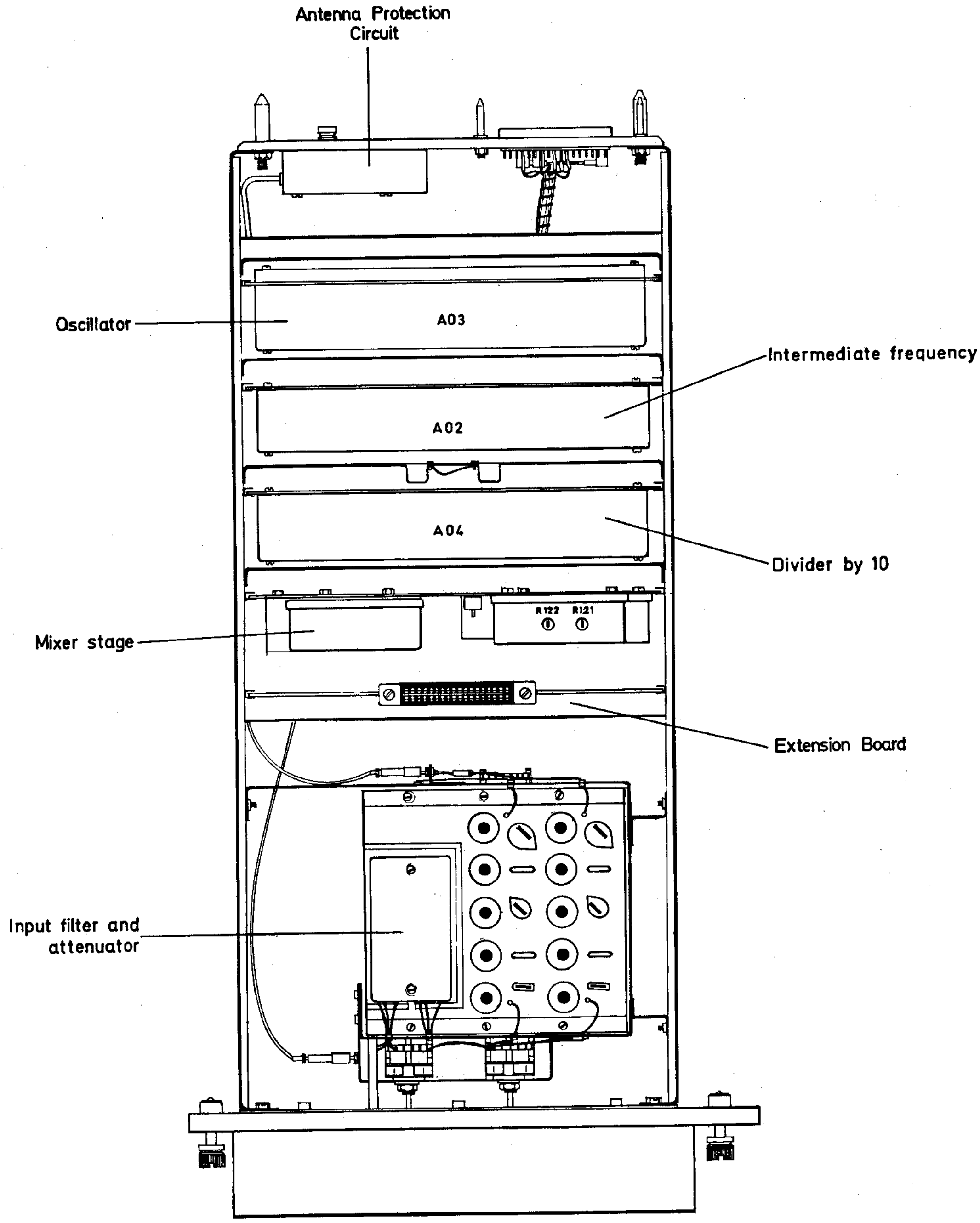
NOTE In case of difficulty, it should be remembered that each filter must be tuned to the centre geometrical frequency of its pass-band. These frequencies are, in ascending order of frequency: 26,5kHz, 103kHz, 207kHz, 342kHz and 450kHz.



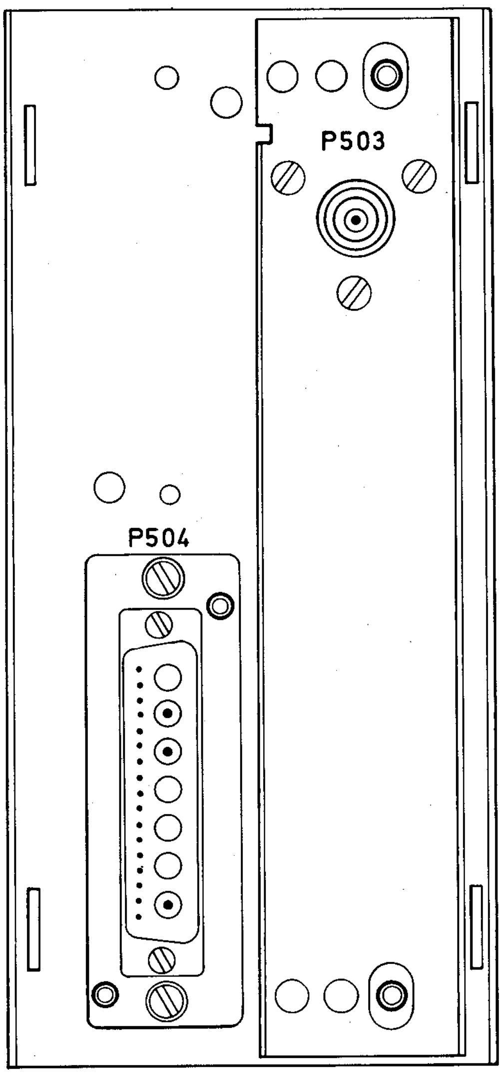
TRC 1802 VLF-LF ADAPTOR-GENERAL VIEW



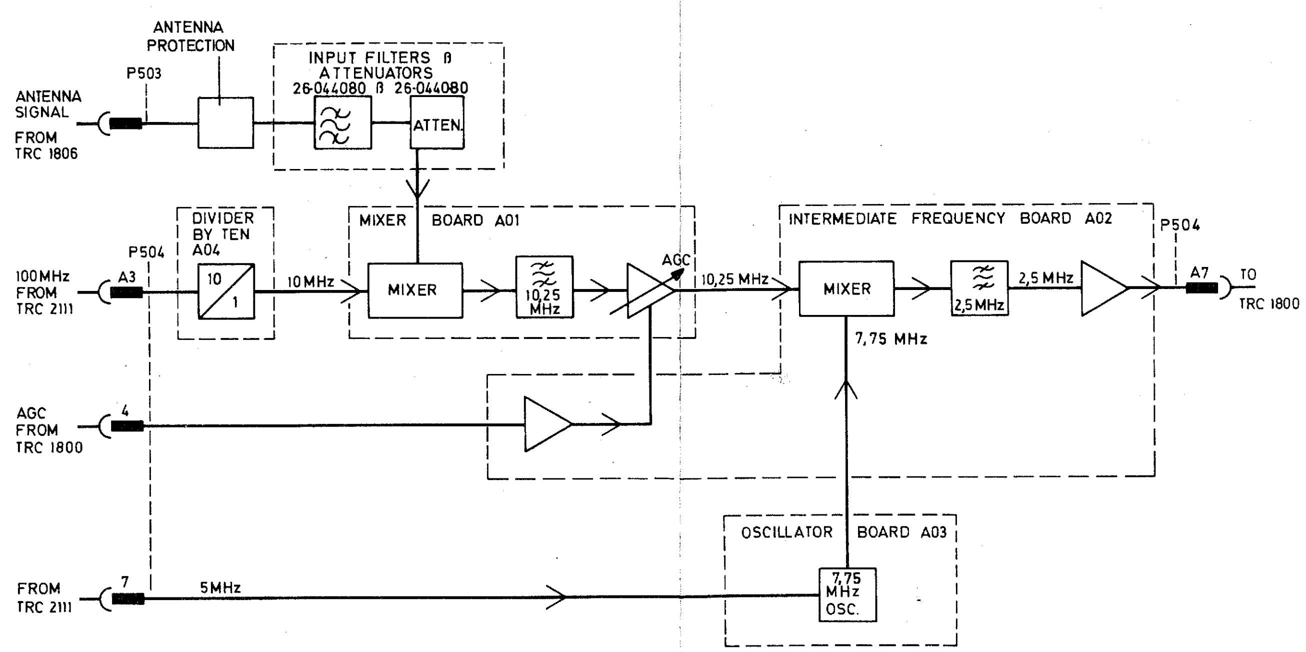
TRC 1802 VLF-LF ADAPTOR-FRONT PANEL CONTROLS



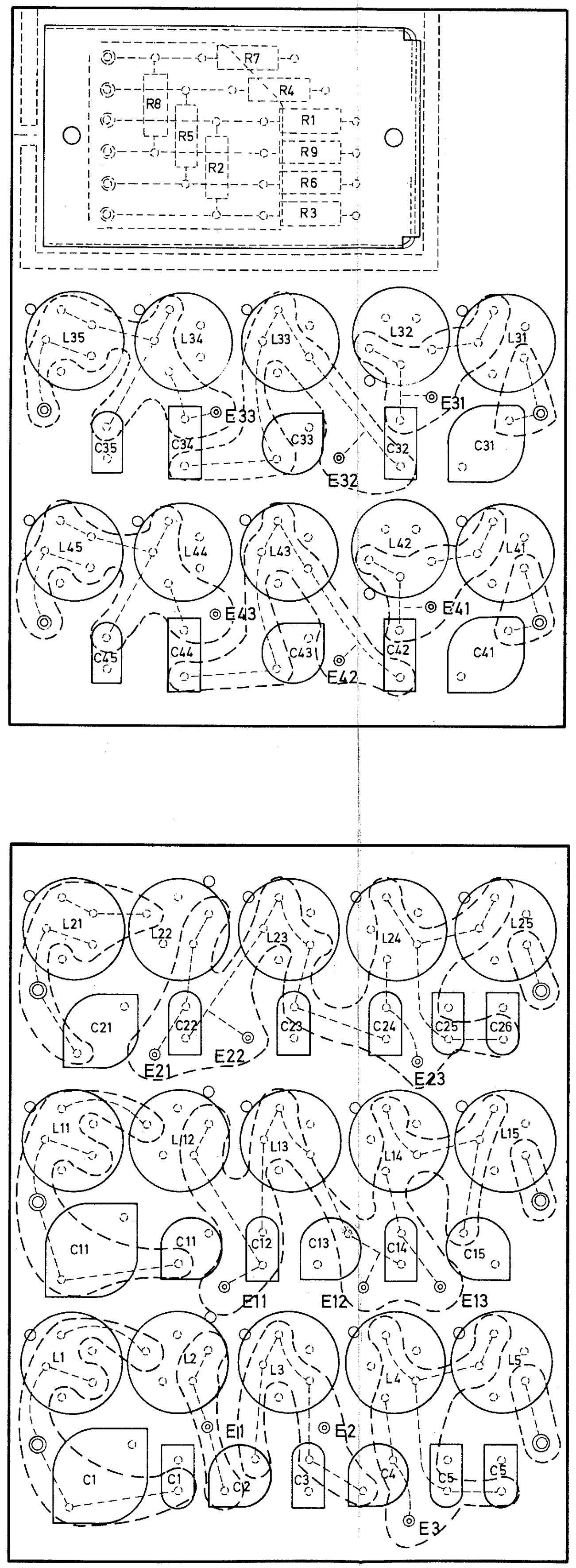
TRC 1802 VLF-LF ADAPTOR - LOCATION OF SUB-UNITS



TRC 1802 VLF-LF ADAPTOR - REAR PANEL

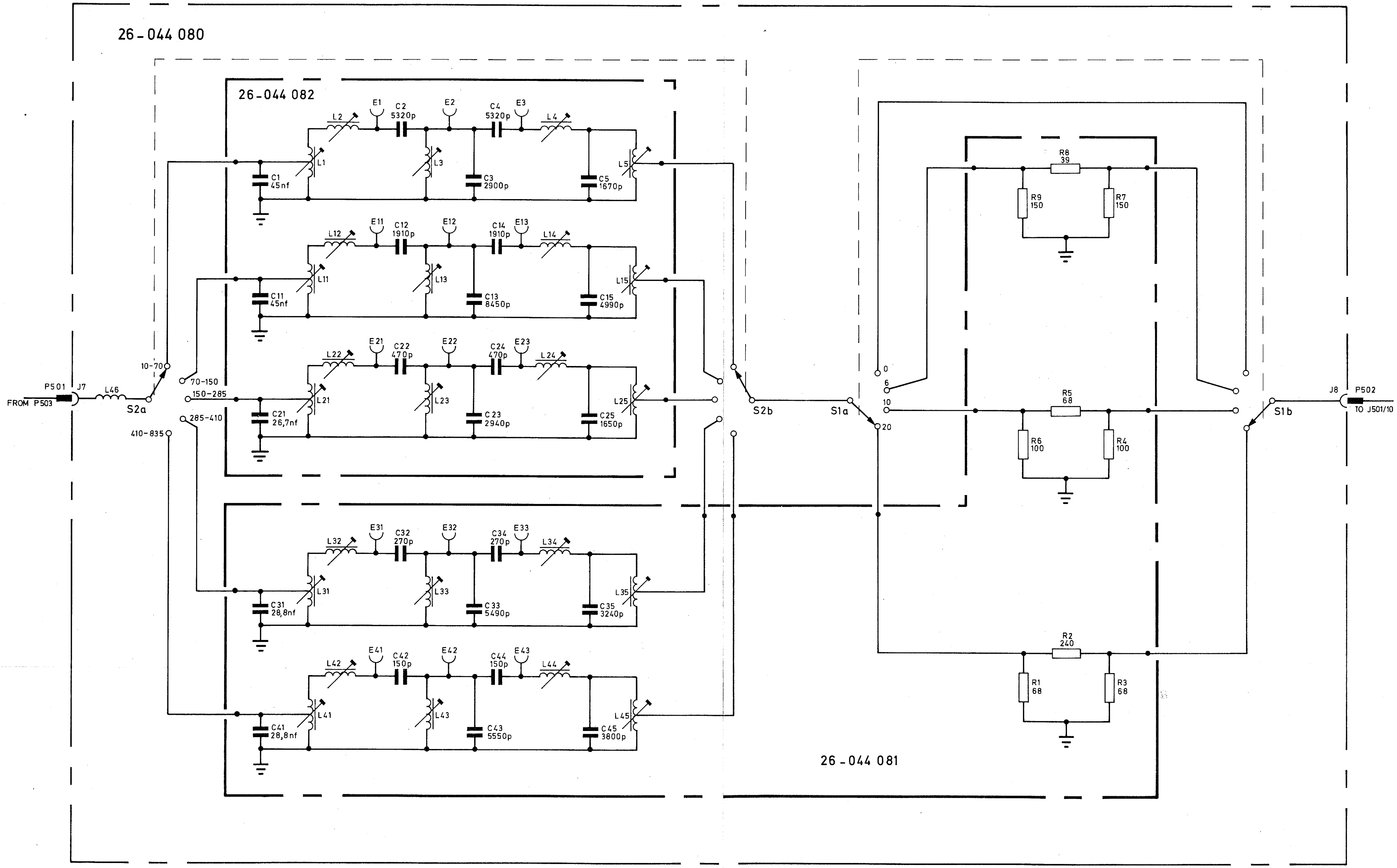


TRC 1802 VLF-LF ADAPTOR - BLOCK DIAGRAM



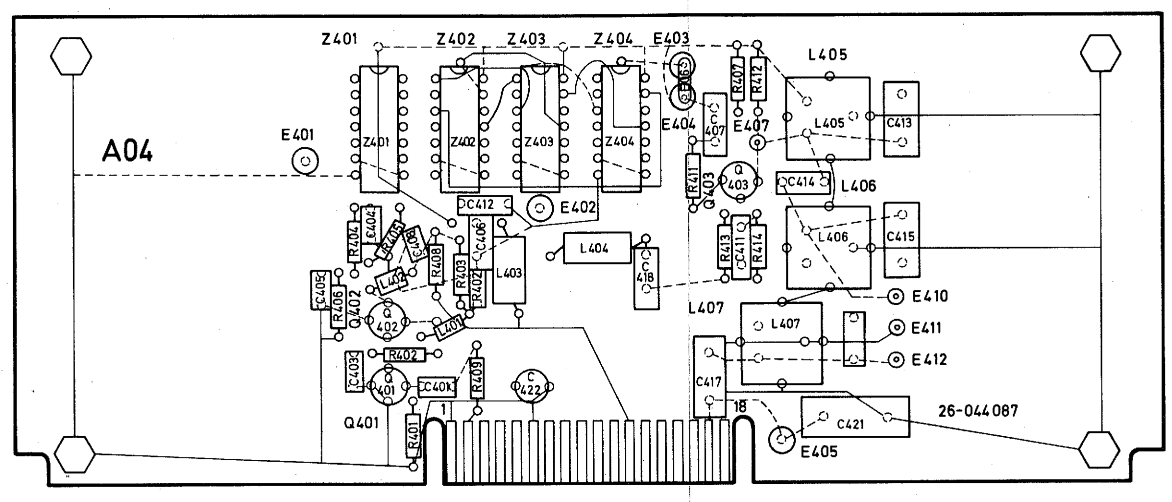
TRC 1802 VLF LF ADAPTOR - INPUT FILTERS & ATTENUATOR

COMPONENT LOCATION DIAGRAM



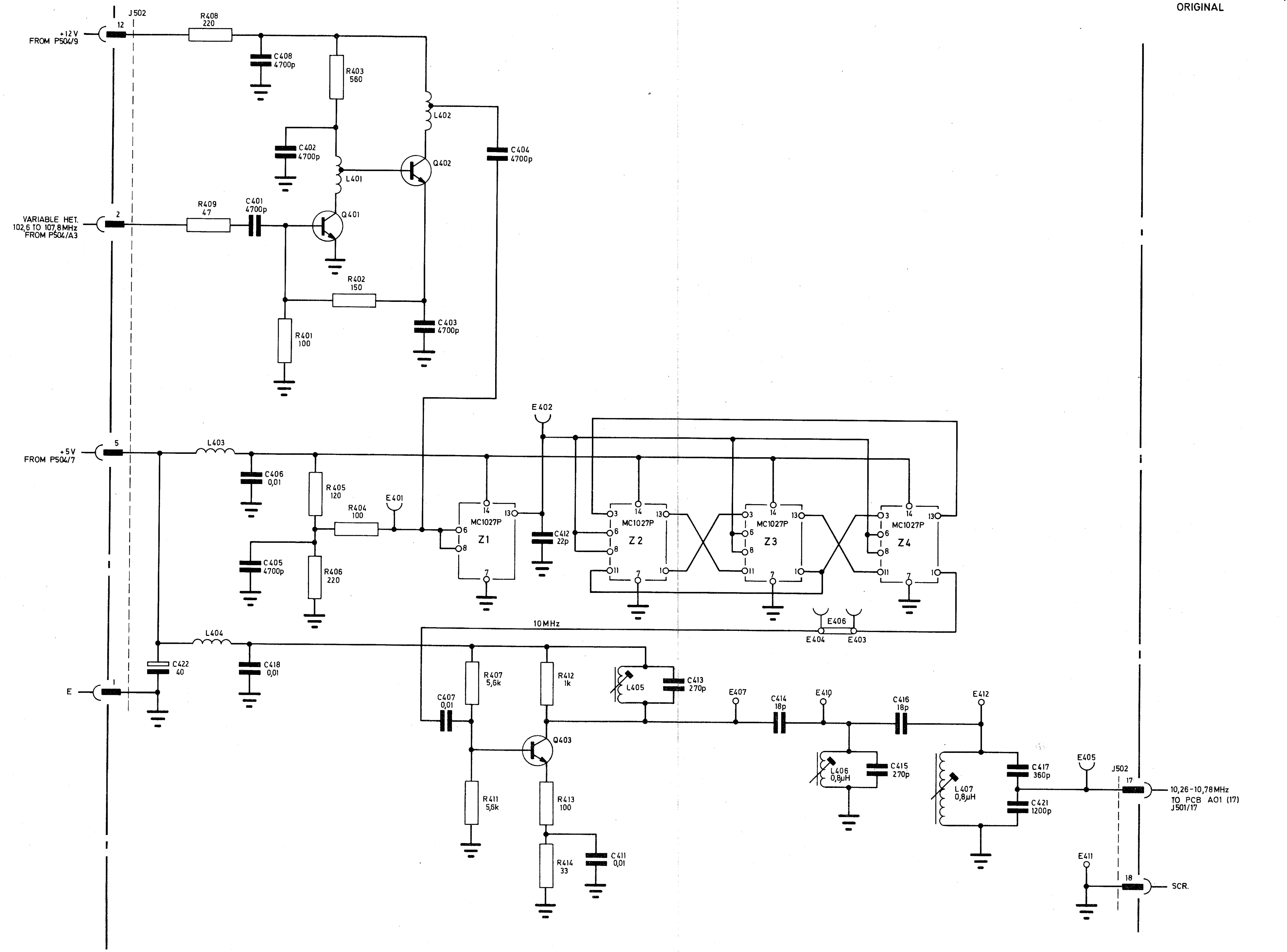
TRC 1802 VLF-LF ADAPTOR - INPUT FILTERS & ATTENUATOR BOARD

CIRCUIT DIAGRAM



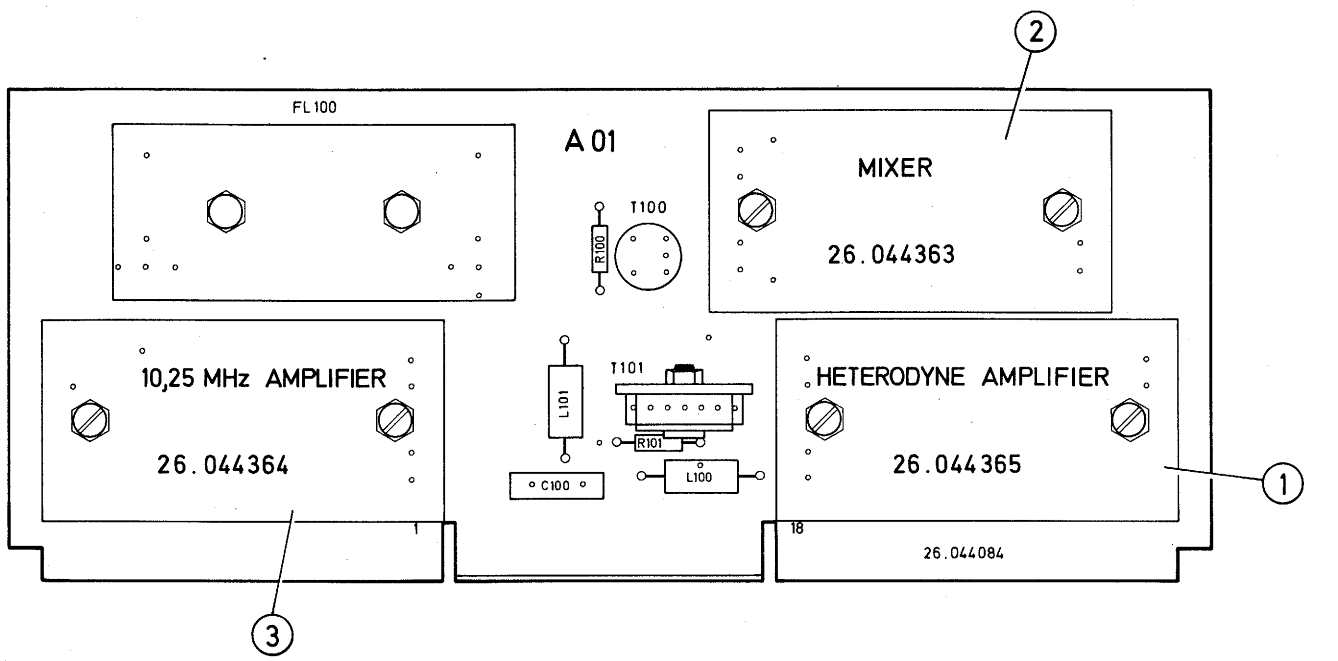
TRC 1802 VLF-LF ADAPTOR-DIVIDER BY 10 BOARD A04

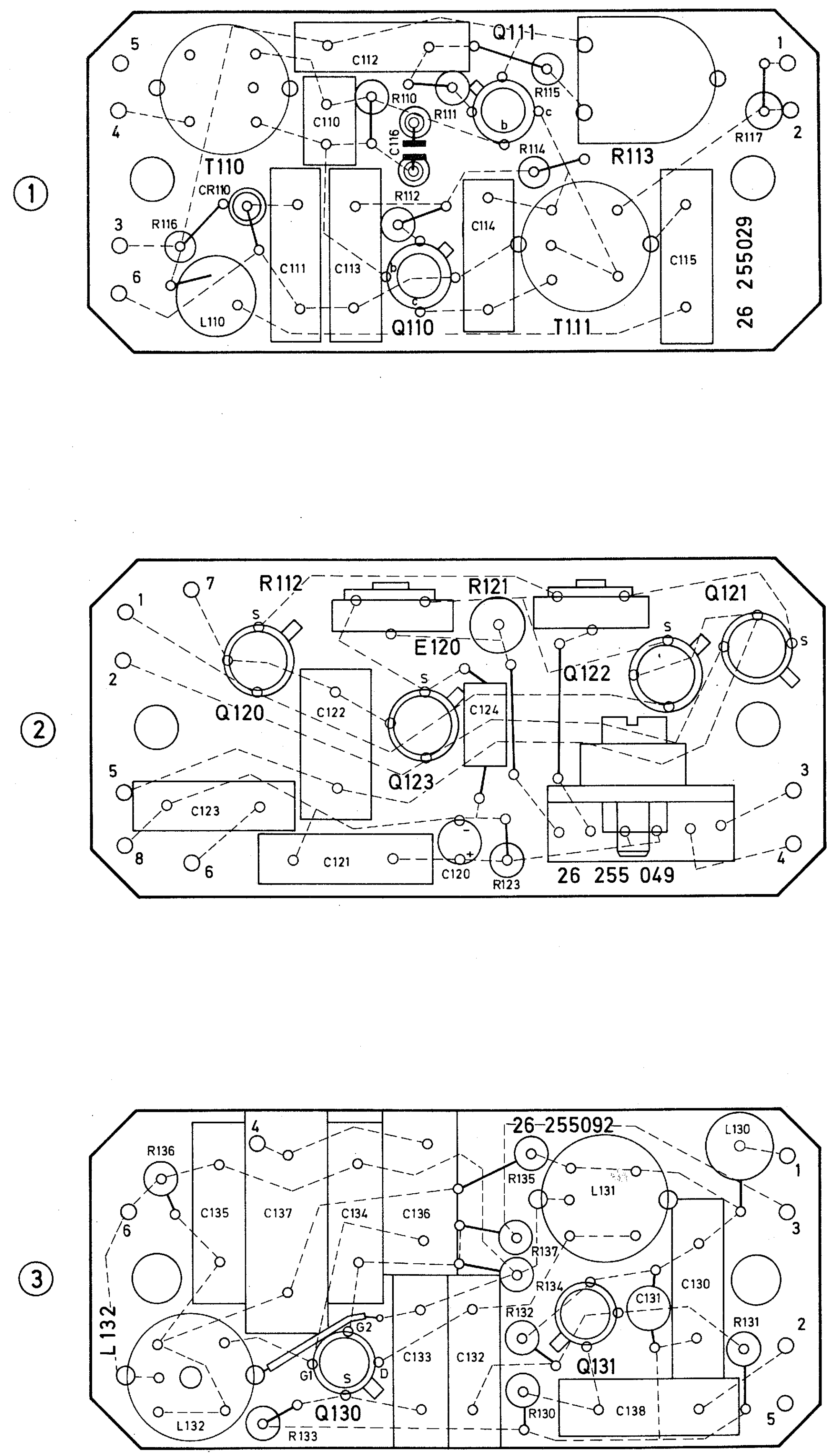
COMPONENT LOCATION DIAGRAM



TRC 1802 VLF-LF ADAPTOR - DIVIDER BY 10 BOARD A04

CIRCUIT DIAGRAM

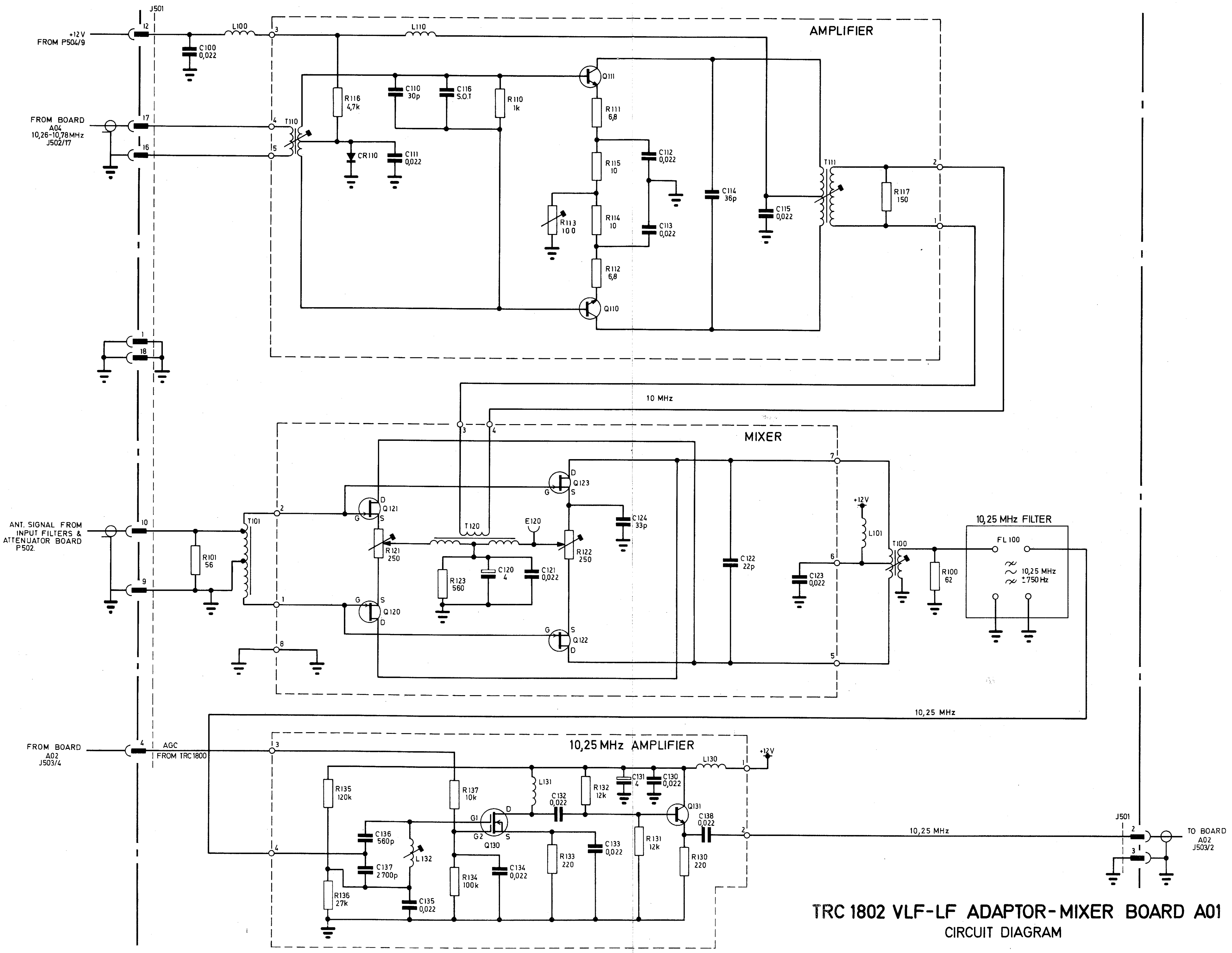




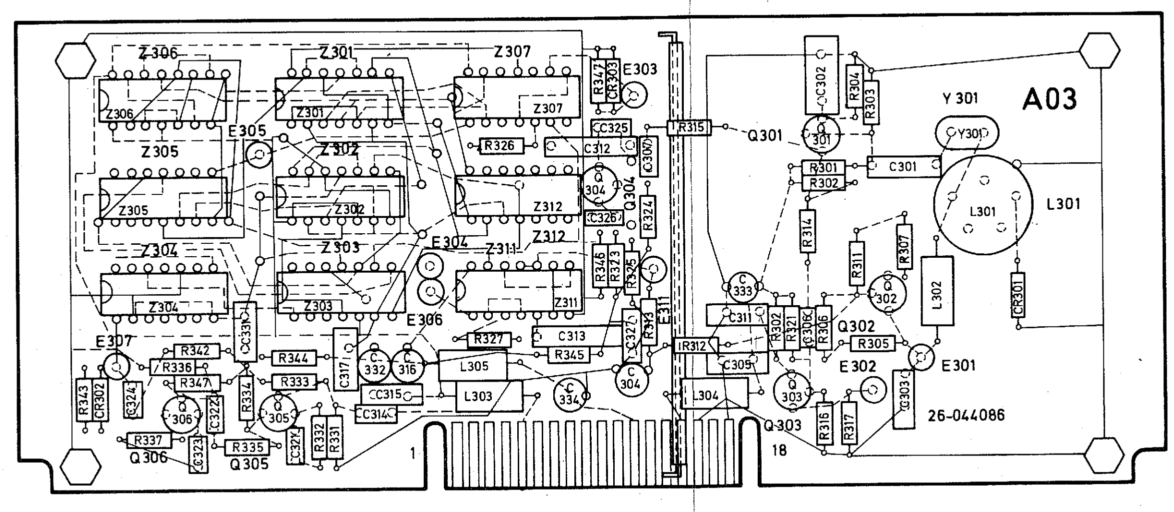
TRC 1802 VLF-LF ADAPTOR-MIXER BOARD A01

COMPONENT LOCATION DIAGRAM

FIG(5)5.10

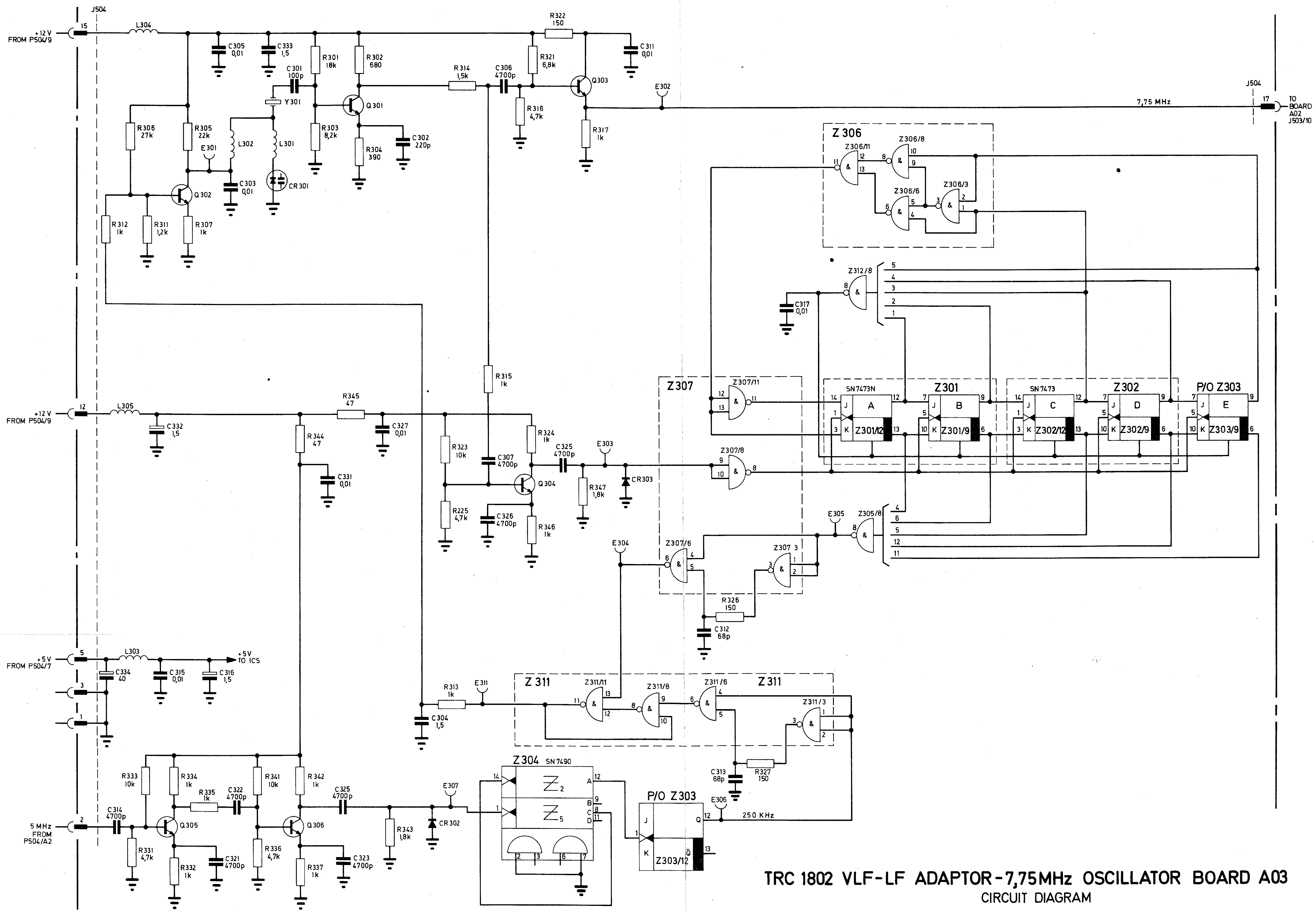


TRC 1802 VLF-LF ADAPTOR-MIXER BOARD A01
CIRCUIT DIAGRAM



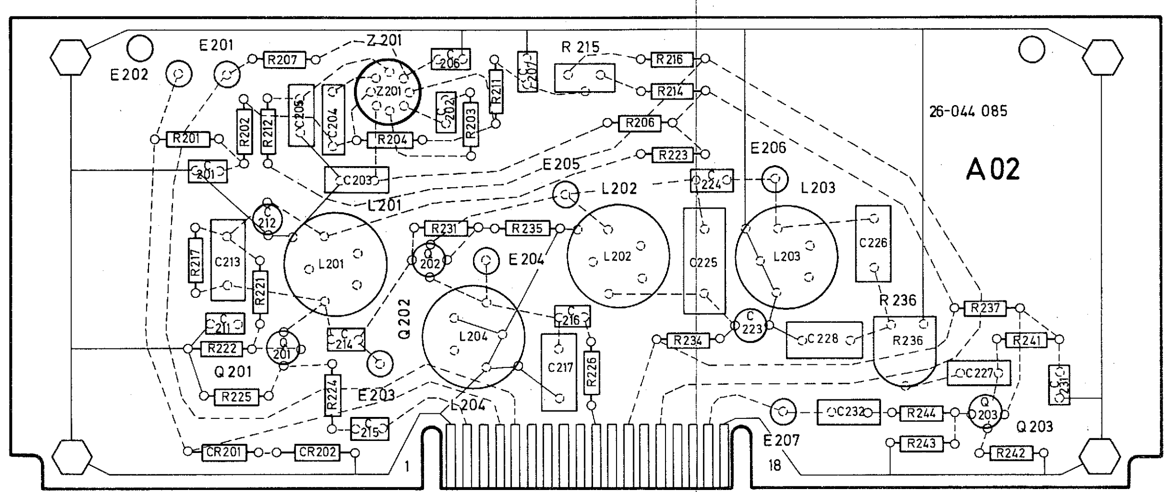
TRC 1802 VLF-LF ADAPTOR - 7,75 MHz OSCILLATOR BOARD A03

COMPONENT LOCATION DIAGRAM



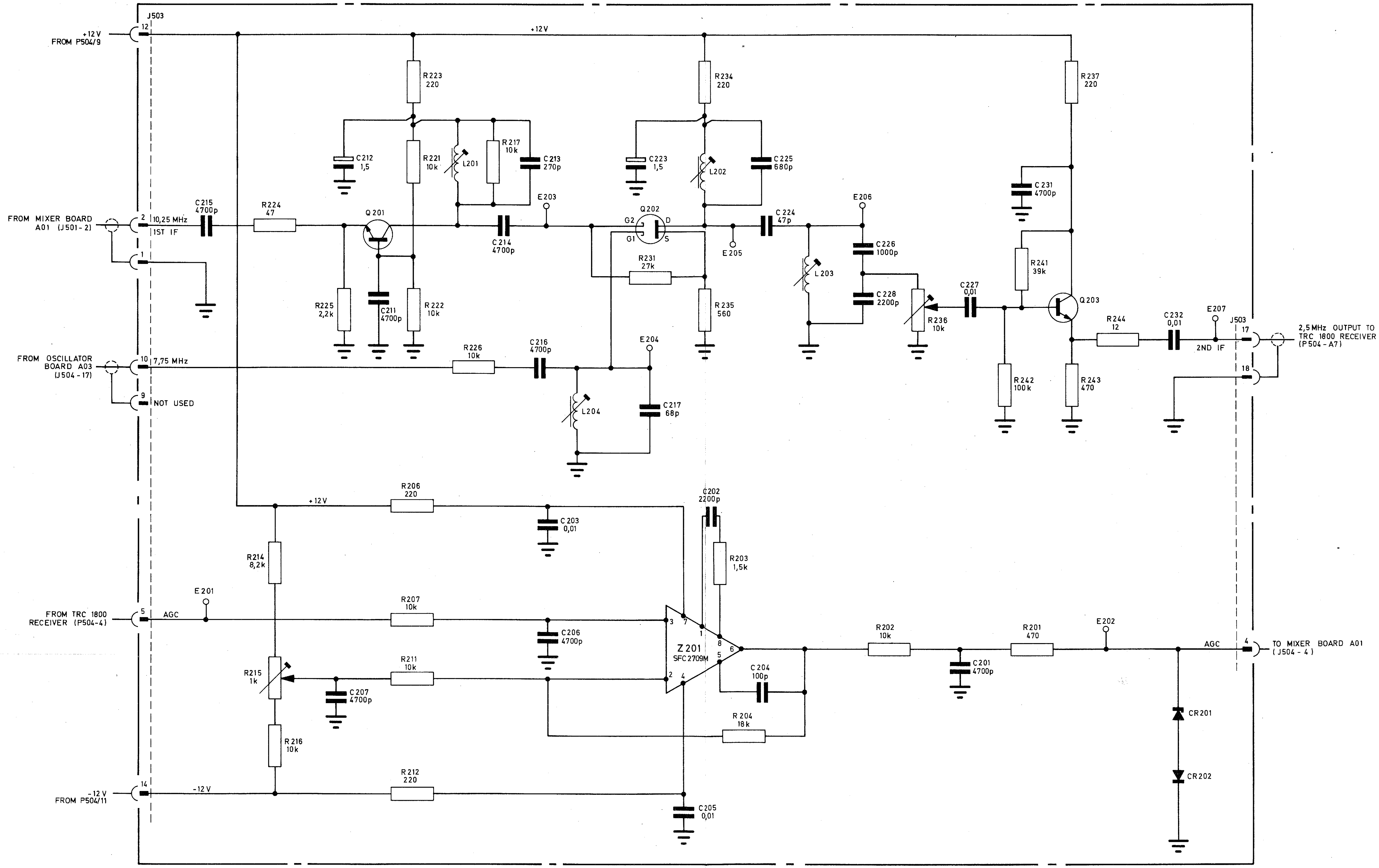
TRC 1802 VLF-LF ADAPTOR-7,75MHz OSCILLATOR BOARD A03

CIRCUIT DIAGRAM



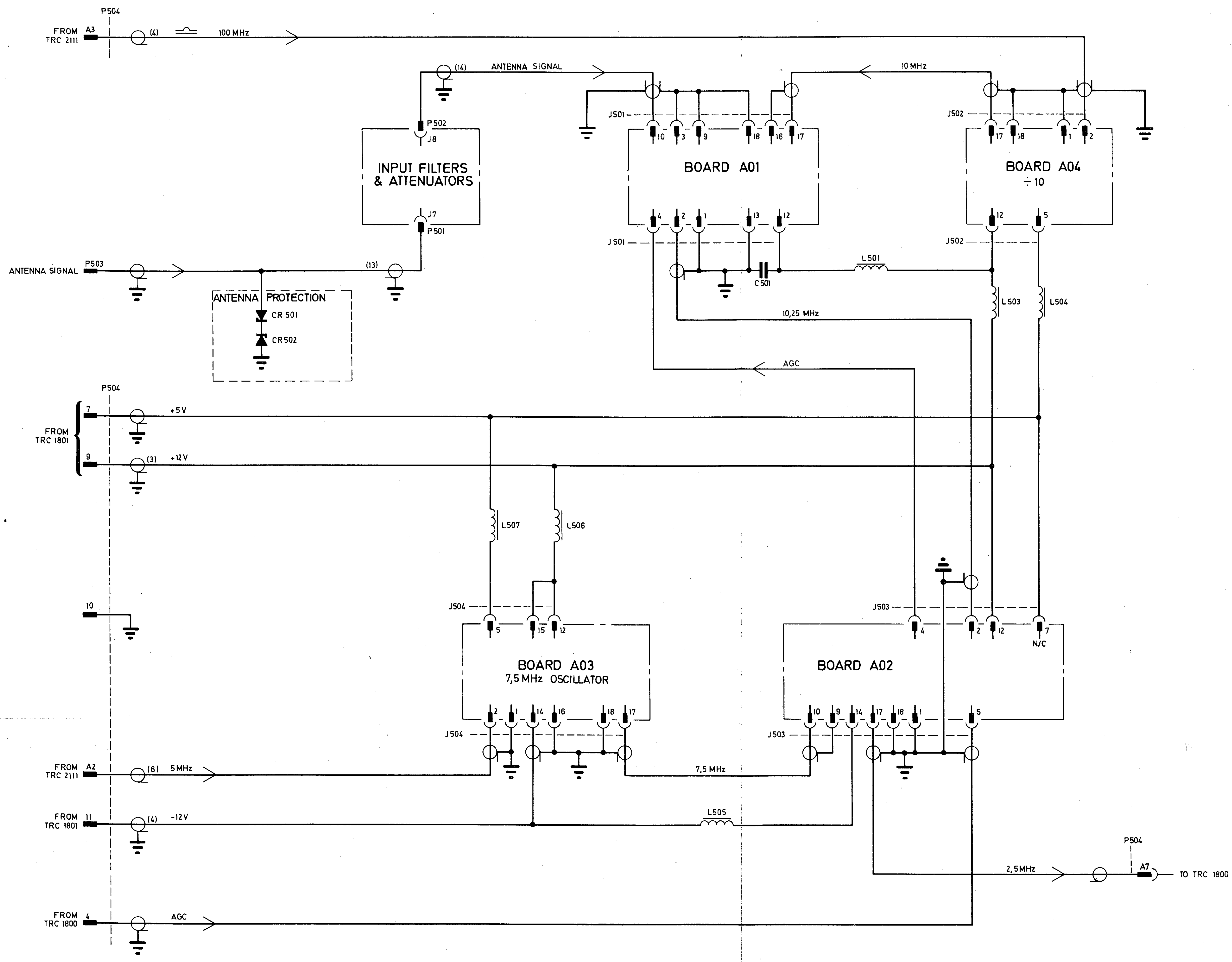
TRC1802 VLF-LF ADAPTOR - INTERMEDIATE FREQUENCY & AGC AMPLIFIER BOARD

COMPONENT LOCATION DIAGRAM



TRC1802 VLF-LF ADAPTOR-INTERMEDIATE FREQUENCY & AGC AMPLIFIER BOARD A02

CIRCUIT DIAGRAM



TRC 1802 VLF-LF ADAPTOR - INTERCONNECTIONS DIAGRAM