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An MC68030 32-bit High Performance Minimum System

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INTRODUCTION

This application note describes the design of a 32-bit High Performance Minimum System based on Motorola's 32-bit MC68030 microprocessor. It makes use of the new fast synchronous interface available on this device to access RAM memory with a two clock cycle read and write bus cycle. The system is designed to operate at 20MHz using available Fast Static RAM memories with future upgrades to 25MHz and 30MHz using faster memory devices.

An MC68681 DUART (Dual-channel Universal Asynchronous Receiver Transmitter) and associated circuitry provides two serial RS232 ports for connection to terminals or host computer links. An MC68230 PI/T (Parallel Interface/Timer) is also included to provide a Centronics-type parallel portorto be used asgeneral I/O. The MC68681 also includes a 16-bit timer and the MC68230 has a 24-bit timer which are available for timing functions.

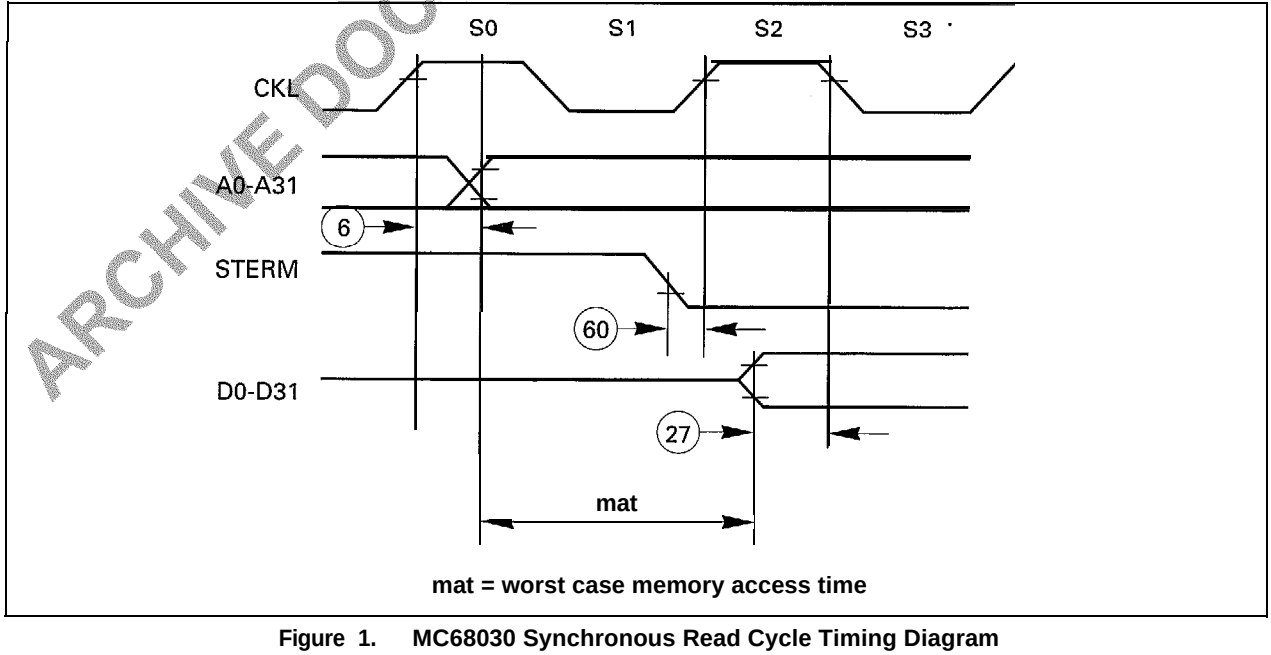
The memory system is implemented by a bank of 8 MCM6164 64k bit fast static RAMs and two 27512 512k bit EPROMs used to contain debug monitor firmware or other system software. The RAM memory is implemented on a 32-bit wide data bus to allow high performance operation and the EPROM is configured on an 8-bit wide data bus making use of the dynamic bus sizing capabilities of the MC68030 microprocessor.

DESCRIPTION OF OPERATION

The most critical timing path in this design is the interface to the RAM memory. The design has been optimised to meet the timing parameters of this interface to allow for zero wait state operation. This has influenced the design of the address decode section since the synchronous termination handshake must be returned to the processor before the start of State 2 of a bus cycle to ensure zero wait state operation. The interface to EPROMs and I/O devices includes buffer delays, etc. and does not operate with zero wait states.

ADDRESS DECODE SECTION

Examining the timing parameters of a synchronous read cycle for the MC68030 shown in Figure 1 the following constraints are evident. a) Address lines AO-A31, function code lines FC0-FC2, and SIZ0-SIZ1 become valid at time number 6 after the rising edge of state zero. b) The synchronous handshake STERM requires a set-up time 60 before the rising edge of state two to ensure zero wait state operation. Therefore the time betweenthemaximumvalue of parameter 6 and the minimum of parameter 60 is the timeavailabletocompletetheaddressdecodeandgenerate the STERM signal. An MC68030 operating at 20MHz has a cycle time of 50nS which yields an address decode and handshake generation time of 50 - min60 -max6 = 50-4-25 = 21nS.



mat = worst case memory access time

Figure 1. MC68030 Synchronous Read Cycle Timing Diagram

In this application the decode is achieved by three 74F521 and two 74F138, U14, U15, U16, U12 and U13. Address lines A31-A24 are used to produce a decode signal called BOARD-SEL which allocates the bottom 1MBytes of the MC68030's address space to this application board. Therefore, this board could be interfaced to other boards to add extra memory, etc. in the address space above the bottom megabyte. U15 and U16 produce two select signals based on the state of address lines A23-A19. These being I/O.ROM_SEL for the bottom 500KBytes of the memory map and RAM-SEL for the next 500KBytes. These two selects are further decoded by U12 and U13 to produce individual selects for 4 x 128K RAM banks, 2 separate 128K Byte ROM selects and 2 separate 128K Byte I/O selects used for the MC68681 and MC68230. The memory map for the board is shown in Figure 2.

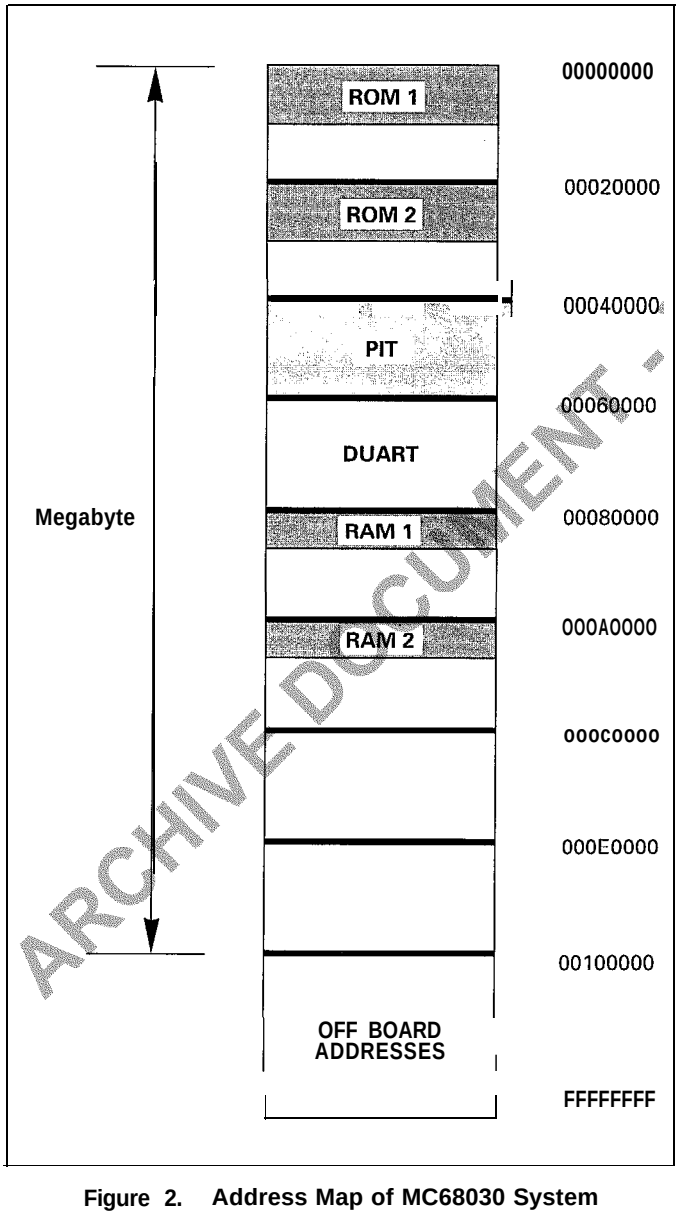


Figure 2. Address Map of MC68030 System

The Synchronous Termination signal STERM is generated by ORing BOARD-SEL and RAM-SEL in U8c. Jumper J6 allows the output of this gate to be fed directly to the processor or to allow a system STERM signal to come from some other off board source via U7b.

A wait state generator is implemented by U35 and allows for O-4 wait states to be selected by jumper J1. This decode and handshake generation logic meets the timing constraints discussed above since for zero wait states the signal path consists of a 74F521 followed by a 74F32 which induces a maximum delay of 11+6.3ns. which is within the 21ns constraint.

PROGRAM ROM

Two sockets are available on the board to accept EPROMs and these are configured for 27512 type devices. The two EPROMs U25 and U26 are both attached to bits D31-D24 of the processors data bus and therefore form an 8-bitwidedata port to the processor. This has the advantage that the processor can be bootstrapped from a single EPROM and, the dynamic bus sizing capability of the MC68030 will automatically handle all sizes of access to the program ROM.

The chip select signals ROM1CS and ROM2CS from the address decode section are used to select the appropriate device. Since the interface port is 8-bits wide the required handshake to the processor is DSACKO = 0 and DSACK1 = 1. Most benchmarkcode will be run from RAM on the board therefore the ROM access time is not critical and no attempt has been made to minimise the number of wait states for each ROM access. The two rom chip selects are ANDed by U7c and then this combined signal is ORed with a delay signal to produce the required DSACKO signal to the processor. The delay signal comes from a second wait state generator implemented by U4. This induces a delay of two cycles of a clock which is one eighth of the processor clock. This guarantees enough access time to the EPROMs even if the clock frequency of the processor is increased beyond the design speed of 20MHz.

The wait state generator implemented by U4 is also used to implement a bus errortime-out for faulty accesses. If the processor does not receive either a STERM or the DSACKx handshake within 4 clock cycles of the slowest clock available on the board then U4 will generate a BERR signal to the MC68030 and force exception processing.

READ/WRITE MEMORY

As discussed previously the address decode logic produces four separate RAM chip select signals each covering a 128KByte address range. Due to the capacitive loading of the RAM chips only two banks have been incorporated on the board. These two RAM banks are currently implemented with MCM6164 45nS type devices but these will be replaced with 32K x 8 type devices once faster versions become available. 'The decode and access time to these RAMs are part of the critical timing path in the design and as such this has been optimised to operate with zero wait-states. The RAM is organised as a 32-bit wide port and uses the new synchronous interface on the MC68030

which yields a two clock cycle read and write bus cycle. To improvetheaccesstime,theRAMchipsusedhaveseparate chip enable and output enable inputs. The chip enable inputs are tied to a "logiczero" to enable them permanently and the output enables are connected to the chip select signals generated by the address decode logic. On a read operation all four chips of one bank are always enabled which drives the full 32 bits of the data bus. The processor will then latch the appropriate sections of the data bus depending on the size of the access. A processor write operation is more complex since only the relevant sections of the data bus contain valid data. The PAL U38 uses the AO, Al, SIZ0 and SIZ1 lines from the MC68030 to generate four separate byte select signals, UUD*, UMD*, LMD* and LLD*. These signals are gated with the RAM1 write select and RAM2 write select signals and address strobe in U39, U40, U41 and U42 to produce the individual RAM chipwrite enable signals. The equations use to code the PAL of U38 are those given in the "Applications" section of the MC68030 User's Manual. There is no data bus buffering between the RAM chips and the processor so no extra delay is introduced into the system. The address decode section generates additional RAM selects for banks three and four and these can be used to select additional RAM which could be added to the board using buffered address and data buses.

SERIAL COMMUNICATIONS

The MC68681 DUART U28 provides two independent serial communication ports. They are normally connected to local terminals or to provide links to host computers. The driver chips U36 and U37 provide the TTL-to-RS232 voltage level conversions between the DUART and the serial ports. These ports are brought out to standard DB25 way connectors J4 and J5. The MC68681 DUART also contains a 16-bit timer which can be used by the system for general counting or timing applications.

PARALLEL PRINTER PORT

A Centronics-type parallel printer port has been implemented using a MC68230 PI/T U27. The output of this device is buffered by a 74LS244 octal driver U29 and brought out to a standard 50-way connector J3. The MC68230 also contains a general purpose 24-bit timer which may be used by an operating system scheduler to generate periodic hardware interrupts.

BUS BUFFERING

The time critical paths to the RAM are unbuffered to allow full zero wait state operation. Two 74F244 devices U30 and U31 are used to buffer address lines AO-A15. These buffered address lines are then connected to the EPROMS and I/O devices in the system and could also be used for additional RAM banks. The basic system contains no data bus buffers due to need for high performance zero wait state operation. Four 74F245 bidirectional buffers could be added to the data bus if extra RAM is required.

This application note has described a design of a high performance 32-bit system using the fast synchronous bus interface of the MC68030 Advanced 32 bit Microprocessor. The system was initially designed and built to operate at 20MHz with a future upgrade to 25MHz with faster memories. The stability of the design has been tested by operating the board at 30MHz using one wait state in the RAM interface with the existing 45ns memory devices. It has also demonstrated the use of the synchronous interface while still using commericially available memory devices and standard FAST TTL interface logic for the address decode section on the design.

REFERENCES

MC68030 Enhanced 32-Bit Microprocessor User's Manual Second Edition MC68030UM/AD REV 1.

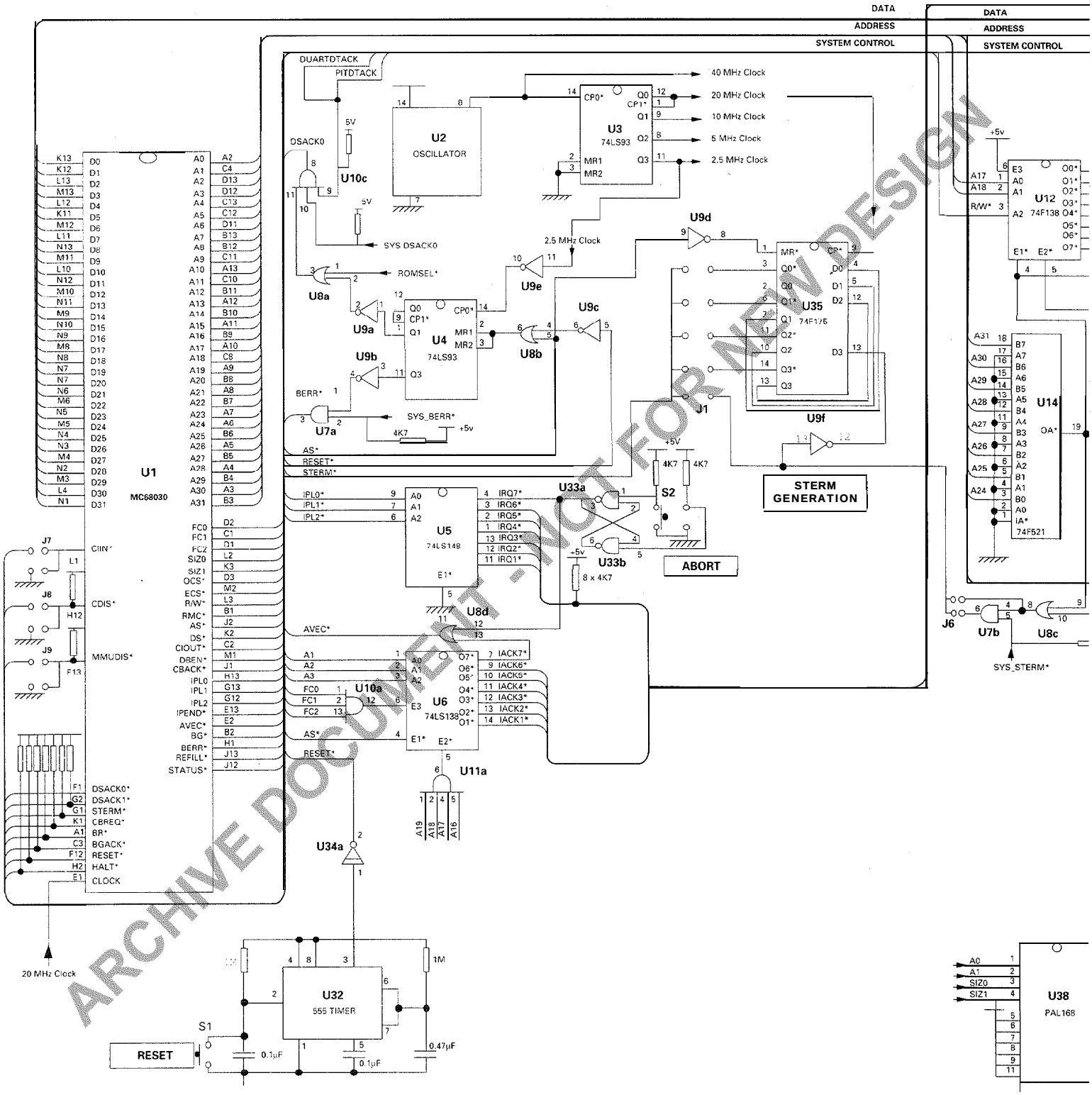
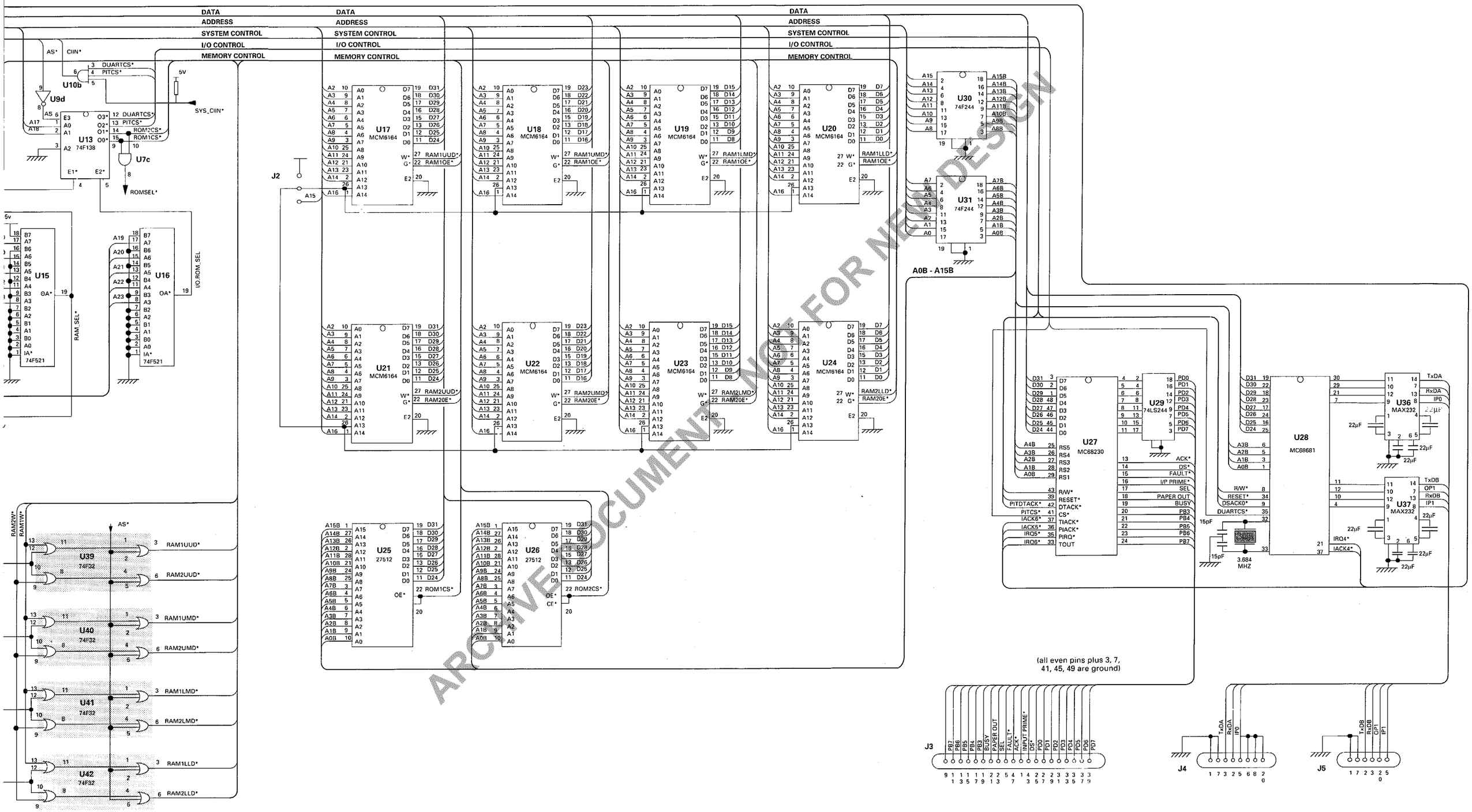


Fig. 3 Full circuit schematics



U1	MC68030	32 bit CPU
u2	40 MHz xtal osc. mod.	
U3 - U4	74LS93	4 bit Counter
u5	74LS148	8 - 3 bit priority Encoder
U6	74LS138	3 - 8 Decoder
u7	74F08	Quad 2 input AND gate
U8	74F32	Quad 2 input OR gate
U9	74F04	Hex Inverter
U10	74FII	Triple 3 input AND gate
U11	74F20	Dual 4 input NAND gate
u12 - u13	74F138	3 - 8 Decoder
U14 - U16	74F521	8 bit Identity Comparator
U17 - U24	MCM6164	8K x 8 Static RAM 45ns
U25 - U26	27512	64K x 8 EPROM
U27	MC68230	Parallel Interface Timer (PI/T)
U28	MC68681	Dual UART (DUART)
u29	74LS244	Octal Buffer
U30 - u31	74F244	Octal Buffer
U32	NE555	Universal Timer
u33	74LS00	Quad 2 input NAND gate
u34	74LS05	Hex Inverter (Open Collector)
u35	74F175	Quad D type Flip Flop
U36 - U37	MAX232	+5v powered Dual RS232 Trans./Rec.
U38	PAL1 6L8	Programmable Logic Array
U39 - U42	74F32	Quad 2 input OR gate
J1		5 way jumper
J2		2 way jumper
J3		50 pin IDC connector
J4 - J5		DB - 25 connectors
J6 - J9		2 way jumper
S1 - S2		SPST Pushbutton

Figure 4. Device List

Literature Distribution Centres:
USA: Motorola Literature Distribution; P.O. Box 20912; Pheonix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands Milton Keynes, MK14 5BP, England.
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