MOTOROLA
SEMICONDUCTOR
ENGINEERING BULLETIN

Order this document
by EB116/D

EB116

Chip-Select Generation for a 33.33-MHz MC68030 Microprocessor and a 33.33-MHz MC68882 Floating-Point Coprocessor

The purpose of this engineering bulletin is to provide an interface recommended for systems that use both the MC68030 second-generation microprocessor and a floating-point coprocessor (FPCP) at 33.33 MHz. Interfacing the MC68030 and an MC68882 is simple. The only part of the interface that requires external logic is the generation of chip select ($\overline{CS}$). The $\overline{CS}$ generation circuit discussed in this document also operates correctly for 25 MHz speed MC68030s, MC68020s, MC68882s, and MC68881s.

The major concern of a system designer is to design a $\overline{CS}$ interface that meets the AC Electrical Specifications for both the MC68030 (MPU) and the MC68882 (FPCP) without adding unnecessary wait states to FPCP accesses. The following maximum specifications (relative to CLK low) meet these objectives:

$$t_{CLK} \text{ low to } \overline{AS} \text{ low} \leq (\text{MPU Spec 1} - \text{MPU Spec 47A} - \text{FPCP Spec 19}) \quad (1)$$

$$t_{CLK} \text{ low to } \overline{CS} \text{ low} \leq (\text{MPU Spec 1} - \text{MPU Spec 47A} - \text{FPCP Spec 19}) \quad (2)$$

Even though requirement (1) is not met under worst-case conditions, if the MPU address strobe ($\overline{AS}$) is loaded within specifications and the $\overline{AS}$ input to the FPCP is unbuffered, the requirement is met under typical conditions. Designing the $\overline{CS}$ generation circuit to meet requirement (2) provides the highest probability that accesses to the FPCP occur without unnecessary wait states. A PAL 16L8 (Figure 1) with a maximum propagation delay of 7.5 ns, programmed according to the equations in Figure 2, can be used to generate $\overline{CS}$. For a 33.33-MHz system, t_{CLK} low to $\overline{CS}$ low $\leq$ 8 ns when this design is used. Should worst-case conditions cause t_{CLK} low to $\overline{AS}$ low to exceed requirement (1), one wait state is inserted in the access to the FPCP; no other adverse effect occurs. Figure 3 shows the bus cycle timing for this interface. Refer to *MC68881/MC68882 Floating-Point Coprocessor User's Manual* for FPCP specifications.

In conclusion, the suggested interface considers the results of characterization data of the MC68030 and MC68882. This interface meets all the MC68030/MC68882 specifications and assures the most efficient accesses to the MC68882.

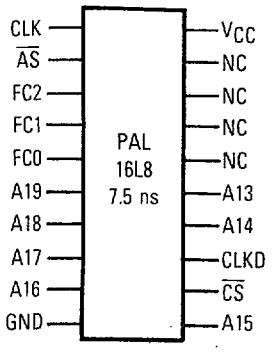
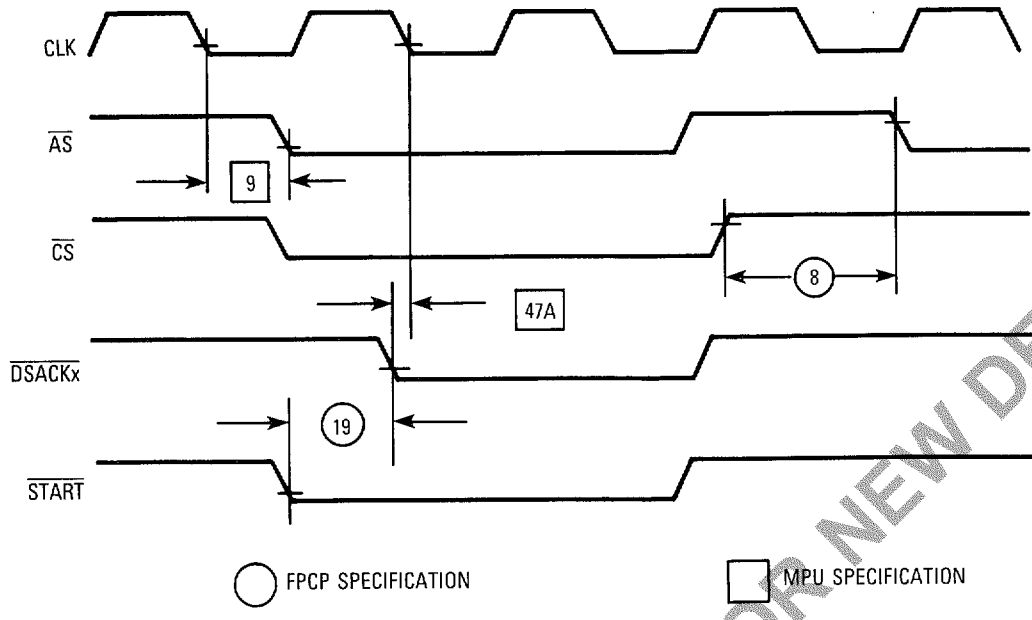


Figure 1. Chip-Select Generation PAL

```
PAL16L8
FPCP CS GENERATION CIRCUITRY FOR 33.33 MHz OPERATION
MOTOROLA INC., AUSTIN, TEXAS
CLK   /AS   FC2   FC1   FC0   A19   A18   A17   A16   GND
A15   /CS   /CLKD   A14   A13   NC1   NC2   NC3   NC4   VCC

CS  = FC2   * FC1   * FC0                   ;cpu space = $7
    * /A19  * /A18  * A17   * /A16          ;coprocessor access = $2
    * /A15  * /A14  * A13                   ;coprocessor id = $1
    * /CLK                                  ;qualified by MPU clock low

    + FC2   * FC1   * FC0                   ;cpu space = $7
    * /A19  * /A18  * A17   * /A16          ;coprocessor access = $2
    * /A15  * /A14  * A13                   ;coprocessor id = $1
    * AS                                    ;qualified by address strobe low

    + FC2   * FC1   * FC0                   ;cpu space = $7
    * /A19  * /A18  * A17   * /A16          ;coprocessor access = $2
    * /A15  * /A14  * A13                   ;coprocessor id = $1
    * /CLKD                                 ;qualified by CLKD (delayed CLK) low

/CLKD = /CLK
```

Description: There are three terms to the $\overline{CS}$ generation. The first term denotes the earliest time $\overline{CS}$ can be asserted. The second term is used to assert $\overline{CS}$ until the end of the FPCP access. The third term is applicable only when using a 33.33 MHz MC68020. This is to ensure that no race condition occurs in case of a late $\overline{AS}$.

Figure 2. PAL Equations



NOTE: For the most recent electrical specifications for the MC68030, refer to technical summary BR508/D Rev. 1; for the MC68881, refer to technical summary BR265/D Rev. 3; and for the MC68882, refer to technical summary BR509/D Rev. 2.

Figure 3. Bus Cycle Timing Diagram

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Center; 88 Tanners Drive, Blakelands Milton Keynes, MK145BP, England.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; P.O. Box 80300; Cheung Sha Wan Post Office; Kowloon Hong Kong.

MOTOROLA

Printed in Great Britain by Tavistock Press (Bedford) Ltd. 3000 1/89