Control system simulator

It is a common practice to test the dynamic performance of any control system with certain known and standard inputs and then evaluate the error pattern to determine the health of the system. A simulator capable of generating very low-frequency simple harmonic motion (SHM), constant-velocity ramps and step functions is used for this, but the equipment has draw backs because of its gear trains, cams, friction drives and governor controls. Even though these are time tested, they tend to drift from their initial settings, resulting in poor accuracy and non-repeatability.

Featured here is a simple electronic simulator configured around the popular 8085 CPU and some of its supporting ICs. The SHM test is considered the toughest test for most of the control systems as it contains acceleration, deceleration, change of sign and constant velocity. To synthesise SHM, a complete cycle of a sine function is sampled into 16K words with 16bit resolution. However, you can see that, with the data of the first quarter (0 to 90°), the entire waveform can be constructed by appropriately manipulating the sign and amplitude at the sampling instants. Thus, 4K × 16 samples of the first quarter of the sine wave only need to be stored, addressed at certain rate and then scaled up or down corresponding to the period and pitch selections.

The 8155's 14bit timer generates the terminal count indicating the rate at which the samples are latched out. Two eight bit ports are programmed to output the 16bit sampled data and the six-bit port to input the pitch and period. The 256byte ram in the 8155 forms a scratch pad.

The step function can be created by selectively inverting one of the output bits according to the bit weight. Bit weight can be decided in conjunction with its interface to the digital-to-synchro or resolver converters. An hardware HALT can also be of some use where the output waveform needs to be stopped at any desired phase (position) before applying the step function. In addition, a simple program to count up and count down can generate the constant speed slow or fast ramps.

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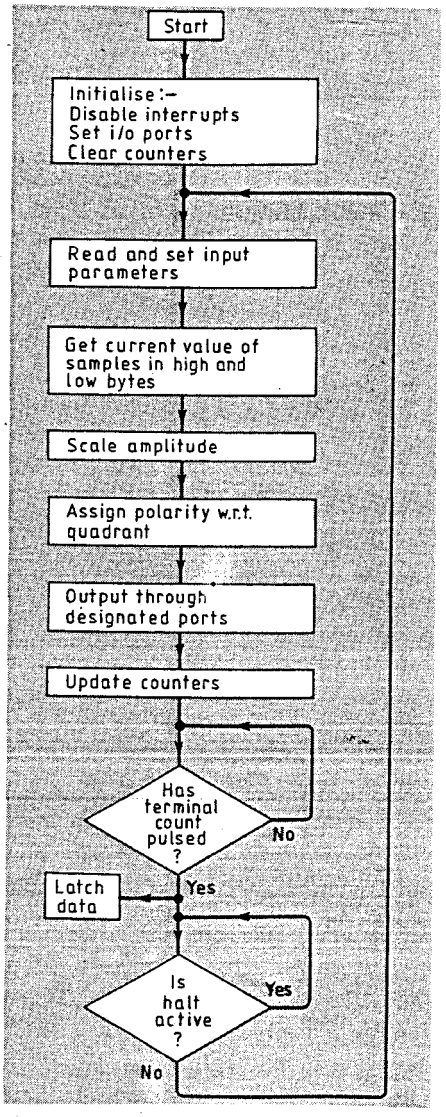

Wide-band VCO for UHF

My main considerations when designing this circuit were wide tuning band-width, low phase noise and low cost.

Decoupling of the base of Tr_2 should be made as close to the package of the device as possible preferably using a chip capacitor.

Capacitor C_6 is selected to give the widest tuning band width and highest power output and will vary according to PCB layout. Again, this should be a chip capacitor and should be connected as close to the transistor terminals as possible.

Transistor Tr_1 forms the basis of an active bias circuit to provide the oscillator with good frequency stability with temperature.

With the right PCB layout and a ground plane the circuit is capable of a tuning range of 310 to 680MHz, a minimum power output of 50mW into 50Ω and a phase noise better than 85dBc/Hz at 10kHz.

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